AIP Applied Physics Letters

# Ultrathin graphene and graphene oxide layers as a diffusion barrier for advanced Cu metallization

Jae Hoon Bong, Seong Jun Yoon, Alexander Yoon, Wan Sik Hwang, and Byung Jin Cho

Citation: Applied Physics Letters **106**, 063112 (2015); doi: 10.1063/1.4908559
View online: http://dx.doi.org/10.1063/1.4908559
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/106/6?ver=pdfcov
Published by the AIP Publishing

**Articles you may be interested in**

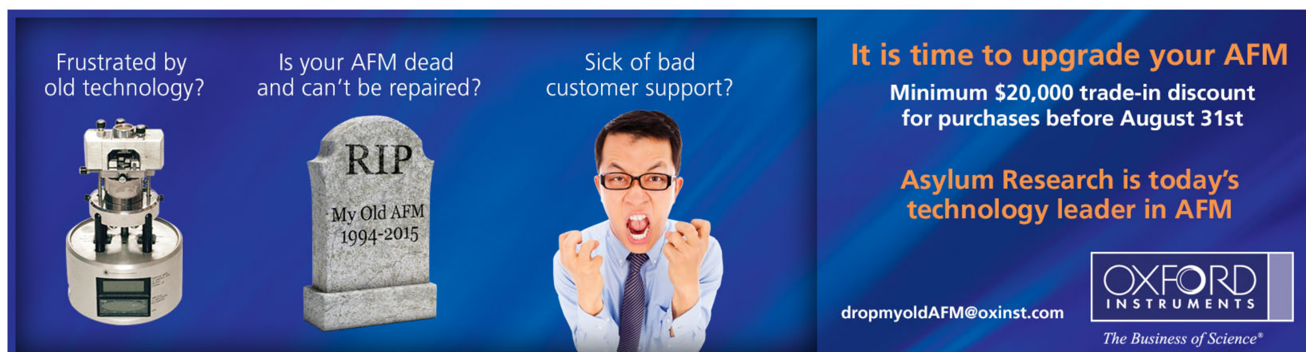
Evaluation of integrity and barrier performance of atomic layer deposited W N x C y films on plasma enhanced chemical vapor deposited Si O 2 for Cu metallization
Appl. Phys. Lett. **89**, 081913 (2006); 10.1063/1.2338768

Real-time spectroscopic ellipsometry study of ultrathin diffusion barriers for integrated circuits
J. Appl. Phys. **96**, 3949 (2004); 10.1063/1.1784621

Ti, TiN, and Ti/TiN thin films prepared by ion beam assisted deposition as diffusion barriers between Cu and Si
J. Vac. Sci. Technol. A **18**, 2312 (2000); 10.1116/1.1288942

Polymerized C-Si films on metal substrates: Cu adhesion/diffusion barriers for ultralarge scale integration?
J. Vac. Sci. Technol. A **17**, 1968 (1999); 10.1116/1.581712

Performance of MOCVD transition metal nitrides as diffusion barriers for Cu metallization
AIP Conf. Proc. **418**, 451 (1998); 10.1063/1.54666




This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 143.248.103.62 On: Wed, 08 Jul 2015 07:26:28

APPLIED PHYSICS LETTERS **106**, 063112 (2015)

# Ultrathin graphene and graphene oxide layers as a diffusion barrier for advanced Cu metallization

Jae Hoon Bong,[1] Seong Jun Yoon,[1] Alexander Yoon,[2] Wan Sik Hwang,[3] and Byung Jin Cho[1,a)]

[1]*Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, South Korea*
[2]*Lam Research Corporation, San Jose, California 95134, USA*
[3]*Department of Materials Engineering, Korea Aerospace University, Goyang 412-791, South Korea*

(Received 9 January 2015; accepted 4 February 2015; published online 13 February 2015)

We report on the diffusion barrier properties of chemical-vapor-deposition grown graphene, graphene oxide, and reduced graphene oxide (rGO) for copper metallization in integrated circuits. Single-layer graphene shows the best diffusion barrier performance among the three but it has poor integration compatibility, displaying weak adhesion and poor nucleation for Cu deposition on top of it. Within the allowable thermal budget in the back-end-of-line process, rGO in a range of 1 nm thickness shows excellent thermal stability with suitable integration compatibility at 400 °C for 30 min. The diffusion barrier property was verified through optical, physical, and chemical analyses. The use of an extremely thin rGO layer as a Cu barrier material is expected to provide an alternative route for further scaling of copper interconnect technology. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4908559]

The continual scaling of integrated circuits (ICs) has led to significant issues of resistance-capacitance (RC) time delay and electromigration (EM) in metal interconnect lines. Copper is widely used as an interconnect in modern ICs because of its low electrical resistivity and good electromigration reliability. However, Cu atoms readily diffuse into Si and $SiO_2$ even at temperature as low as 200 °C, resulting in degradation of the device performance and reliability by forming resistive Cu-Si compounds and generating deep trap levels in the silicon. It is therefore necessary to use a barrier material between Cu and underlying dielectrics to prevent the diffusion of copper.

Refractory metal nitrides are widely used as diffusion barriers because of their low solubility in Cu, high thermal stability, and high conductivity. However, as the dimensions of Cu interconnectors are further scaled down, the thickness of the barrier materials also should be reduced. According to the International Technology Roadmap for Semiconductors (ITRS), barrier materials thinner than 2 nm will be required in 22 nm line-width interconnect technology.[1] While many researchers have studied various barrier materials deposited by chemical-vapor-deposition (CVD) or atomic-layer-deposition (ALD),[2–4] the formation of an ultra-thin barrier material with satisfactory barrier properties remains a significant challenge.

Graphene, a monolayer of carbon atoms densely packed in a hexagonal lattice, recently has been explored as an ultra-thin barrier material because of its outstanding scalability and chemical/thermal stability.[5,6] In general, the interconnect barrier employs a multilayer system that consists of not only a barrier layer but also an adhesive layer, liner, and seed layer for Cu deposition. Recent research has focused on graphene's outstanding thermal stability as a Cu diffusion barrier,[7,8] but other properties related to its performance as a barrier layer such as its adhesion and seed layer properties have been overlooked. Although graphene is advantageous for application as a Cu diffusion barrier due to its superior thermal stability, it accompanies device integration issues due to its $sp^2$ hybridization bonding nature.[9] It is therefore imperative to consider other alternatives having carbon covalent bonds such as graphene oxide. The realization of superior barrier properties against molecular penetration has been achieved by implementing graphene as well as reduced graphene oxide (rGO), which, similar to graphene, possesses carbon covalent bonds and, unlike graphene, various functional groups as well.[10–14] The use of graphene oxide (GO) and rGO provides opportunities to promote adhesion and provide a Cu seed layer by engineering the functional groups. Moreover, they afford advantages over graphene because they are mass-production friendly and offer solution process capability.[15–17] Nonetheless, the barrier properties of GO and rGO with respect to Cu diffusion have not been investigated thus far. In this work, we present a comparative study on the Cu diffusion barrier properties of four different stacked structures: Cu/CVD-grown mono-layer graphene/Si, Cu/GO/Si, Cu/rGO/Si, and Cu/Si. It was demonstrated that the Cu diffusion barrier properties of GO and rGO are comparable to those of CVD-grown graphene at moderate temperature and they offer superior integration compatibility.

Large-area monolayer graphene was synthesized by an inductively coupled-plasma enhanced CVD process. In the growth step, $C_2H_2$ gas, employed as a precursor, was flowed onto a 4-in. Cu/$SiO_2$/Si wafer with 50 W RF plasma at 750 °C. The synthesized graphene was then transferred onto a Si substrate by a wet transfer method using poly(methyl methacrylate) (PMMA), followed by the removal of PMMA by forming gas annealing at 400 °C for 2 h. In this experiment, a

a)Author to whom correspondence should be addressed. Electronic mail: bjcho@kaist.edu

 © 2015 AIP Publishing LLC

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 143.248.103.62 On: Wed, 08 Jul 2015 07:26:28

heavily p-doped Si wafer (100) was used, and sulfuric peroxide mixture (SPM) treatment was performed to obtain a hydrophilic surface before the formation of barrier layers on the silicon substrate. A commercially available GO solution was used, and its flake size and concentration are about 90 nm and 2 g/l, respectively. A thin GO layer was uniformly dispensed on a Si substrate by a spin-coating process, and rGO was obtained through thermal reduction of the GO at 400 °C for 10 min in a $H_2$(10%)/Ar gas ambient. A 30-nm-thick Cu film was then deposited on CVD-grown graphene/Si, GO/Si, rGO/Si, and Si by thermal evaporation. Finally, high vacuum ($\sim 10^{-6}$ Torr) annealing was conducted at various temperatures at and above 400 °C for 30 min to accelerate Cu diffusion into Si.

The properties of the barrier materials were examined through Raman measurement (laser wavelength of 514 nm), atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS) analyses. The copper silicide crystal structure, formed by the reaction between Cu and Si, was observed via an optical microscope (OM), scanning electron microscope (SEM), energy-dispersive X-ray spectroscopy (EDXS), and X-ray diffraction (XRD) spectra. Back-side secondary ion mass spectroscopy (SIMS) was used to directly observe the concentration of Cu atoms diffused into Si.

Fig. 1(a) shows the Raman spectra of CVD-grown graphene, GO, and rGO. The negligible D peak and the intensity ratio of the 2D over G peaks of CVD-grown graphene indicate that single-layer graphene (SLG) with a small amount of defects was synthesized. In contrast to SLG, the 2D peak became weak and the D peak was prominent in the GO and rGO samples due to structural disorders and defects. There was no significant change in the intensity ratio of the D over G peaks from GO to rGO, indicating that additional defects were not introduced in the rGO layer after thermal reduction in the forming gas ambient. A noticeable difference from GO to rGO is the downshift of the G peak from 1604 $cm^{-1}$ to 1591 $cm^{-1}$ after reduction, which reflects restoration of the $sp^2$ hybridized carbon network in the rGO.[18] The presence of the D peak in GO and rGO, respectively, might promote adhesion and nucleation sites in the barrier stacks. The thickness of the GO layer coated on Si varied depending on the specifications of the GO solution, the spin-coating process, and the surface energy of the target substrate. We optimized those process parameters and finally obtained a continuously distributed thin GO layer on the hydrophilic Si substrate after SPM treatment. In Fig. 1(b), the thickness of the GO layer coated on the Si substrate was determined to be approximately 1.2 nm by AFM and that of rGO was slightly decreased to about 1 nm after thermal reduction due to removal of the functional groups. Figs. 1(c) and 1(d) exhibit C 1s XPS spectra of the GO and rGO layers. As shown in Fig. 1(c), the C 1s spectrum of the GO layer revealed the $sp^2$ C=C and $sp^3$ C-C bonding peaks at 254.5 eV and 255.4 eV, respectively, and there were three peaks indicating the oxygen functional groups, corresponding to C-O-C (286.5 eV), C=O (287.5 eV), and C-O-OH (288.8 eV).[19] After the reduction of GO, the peak intensities of these functional groups significantly decreased, and some of these functional groups were still observed in the rGO.

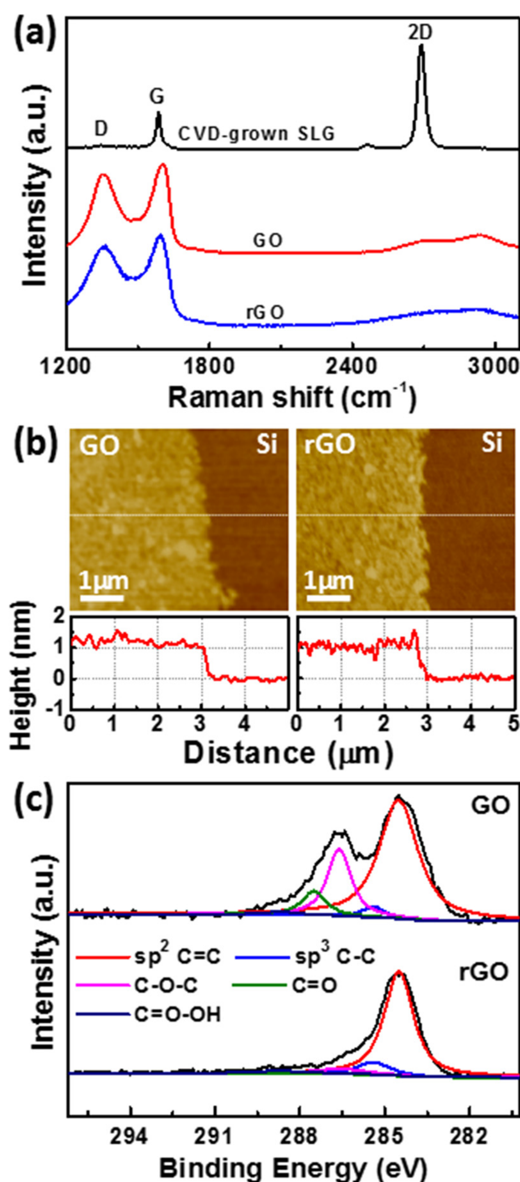



FIG. 1. (a) Raman spectra of CVD-grown graphene, GO, and rGO. (b) AFM images and line profiles of GO and rGO layers coated on Si. (c) XPS spectra (C 1s) of GO and rGO.

Fig. 2(a) shows optical microscope images of a Cu/Si sample after high vacuum annealing for 30 min at various temperatures. Without a barrier layer, rectangular-shaped dark spots were observed after annealing, and both the size and the density of the dark spots increased gradually with the annealing temperature. Fig. 3 shows a cross-sectional SEM image of the dark spots on the Cu/Si sample annealed at 600 °C for 30 min. Without the diffusion barrier, certain compounds emerged at the Cu-Si interface after high vacuum annealing at 600 °C. From the EDXS analysis results, as shown in the inset image of Fig. 3, these compounds were identified as crystallites of copper silicide resulting from reaction between the diffused Cu and Si. The temperature at which copper silicide formation is first observed was around 400 °C in our experiment, which is higher than the reported temperature of a Cu/bare Si system.[20–22] A possible reason for this is the presence of a thin chemical oxide layer on the Si substrate formed during the SPM chemical treatment to

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 143.248.103.62 On: Wed, 08 Jul 2015 07:26:28

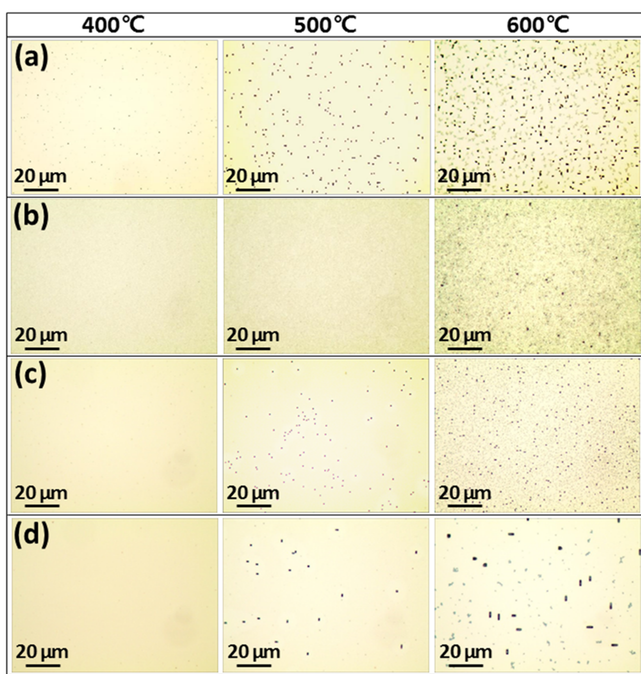



FIG. 2. Optical microscope images of (a) Cu/Si, (b) Cu/SLG/Si, (c) Cu/GO/Si, and (d) Cu/rGO/Si structures after annealing at various temperatures for 30 min in a vacuum ambient.

render the silicon surface hydrophilic. On the other hand, in the Cu/SLG/Si structure, it was found that the copper silicide was first observed at a higher temperature of about 600 °C, indicating that the SLG provides an excellent Cu diffusion barrier. Also, in both the Cu/GO/Si and Cu/rGO/Si structures, crystallites of copper silicide were found after annealing at 500 °C, as shown in Figs. 2(c) and 2(d), but the density of crystallites is lower than that of the control sample with no barrier. Among these two structures, the density of the copper silicide crystallite is lower in the Cu/rGO/Si sample, implying that the rGO layer has a better barrier property than the GO layer.

For further analysis of the thermal stability of SLG, GO, and rGO as Cu diffusion barrier materials, an XRD analysis was performed as well. Fig. 4(a) shows the XRD patterns of as-deposited copper and an annealed Cu/Si sample at 400 °C

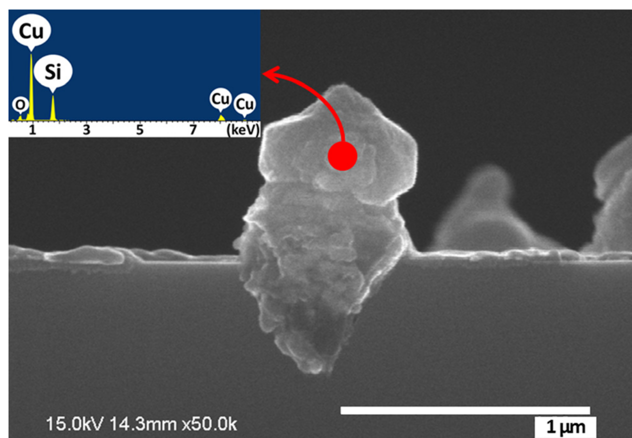



FIG. 3. SEM image of the crystallite of copper silicide formed at the Cu-Si interface. The sample was annealed at 600 °C for 30 min. Inset image indicates EDXS analysis of the crystallite of copper silicide.

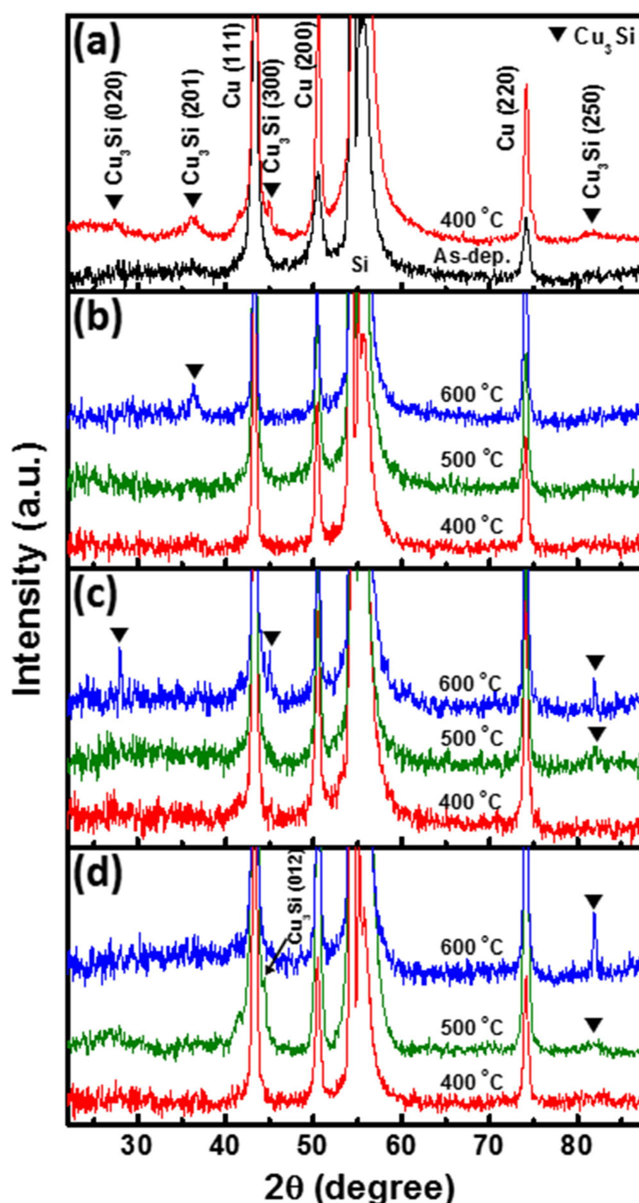



FIG. 4. XRD spectra of (a) Cu/Si, (b) Cu/SLG/Si, (c) Cu/GO/Si, and (d) Cu/rGO/Si structures after annealing at various temperatures for 30 min. The arrows indicate the presence of each Cu-Si compound.

for 30 min. In the case of the as-deposited copper, a Cu (111) peak was clearly seen at 43.3° and relatively small peaks of Cu (200) and Cu (220) were observed at 50.5° and 74.3°, respectively. These results indicate that the as-deposited Cu by a thermal evaporator has a preferential orientation in the (111) direction and the deposited film is a polycrystalline structure. After annealing at 400 °C for 30 min in a vacuum ambient, the intensity of the Cu peaks increased and their full-width-at-half-maximum (FWHM) values became narrower, indicating that crystallization and grain growth of Cu occurred. Additional peaks representing copper silicide were observed at 27.7°, 36.2°, 45°, and 82°, which correspond to $Cu_3Si$ (020), $Cu_3Si$ (201), $Cu_3Si$ (300), and $Cu_3Si$ (250).[23,24] These peaks indicate that Cu reacted with Si due to Cu diffusion after annealing at 400 °C. Contrary to the annealed Cu/Si sample, the Cu/SLG/Si sample shows no noticeable $Cu_3Si$ peaks after 500 °C annealing. The $Cu_3Si$ (201) peak at 36.2° appears only after annealing

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 143.248.103.62 On: Wed, 08 Jul 2015 07:26:28

at 600 °C for 30 min, as shown in Fig. 4(b). This further confirms that the CVD-grown SLG is an excellent barrier material and it effectively blocks the diffusion of Cu atoms up to the annealing temperature of 500 °C. Figs. 4(c) and 4(d) show XRD patterns of Cu/GO/Si and Cu/rGO/Si structures after annealing for 30 min. In both cases, the peaks reflecting copper silicide are not detected until 400 °C; $Cu_3Si$ peaks, however, are observed after annealing at 500 °C and become more pronounced after 600 °C annealing. These results suggest that GO and rGO can also effectively block Cu diffusion during annealing at 400 °C for 30 min. For typical BEOL processes, the process temperature usually does not exceed 400 °C, and therefore ultrathin GO and rGO layers in a thickness range of 1 nm can be applied to Cu interconnects as a diffusion barrier.

The barrier properties of SLG, GO, and rGO also can be examined by a SIMS analysis, which enables direct in-depth profile measurement of atomic concentrations. In this experiment, a back-side SIMS analysis was performed after mechanical polishing of the back-side of the wafers for accurate profiling of the diffused Cu atoms in Si. Ion beam induced Cu diffusion, the so called "knock-on effect," thereby can be excluded. Fig. 5(a) shows the depth profile of Cu in silicon after annealing of the Cu/Si sample at 400 °C for 30 min. The diffused Cu atoms were observed in the entire depth of Si, and their concentration ranges from about $10^{19}\,cm^{-3}$ to about $10^{20}\,cm^{-3}$. In contrast to the Cu/Si sample, from SIMS results of Cu/SLG/Si samples diffused Cu is observed only in the 600 °C annealing sample, as shown in Fig. 5(b). Figs. 5(c) and 5(d) show that the GO and rGO layers both effectively block the Cu diffusion during 400 °C annealing, consistent with the XRD analysis results in Fig. 4. After annealing at 500 °C for 30 min, the concentration of diffused Cu in Si penetrating the rGO layer is about $4 \times 10^{18}\,cm^{-3}$, which is less than that of the Cu/GO/Si structure ($\sim 10^{20}\,cm^{-3}$). It is known that the functional groups of GO can provide diffusion paths accelerating the oxidation of Cu and Fe surfaces.[14] This suggests that the slightly better blocking performance of the rGO layer compared to the GO layer might be due to the removal of the functional groups. Even though rGO was less thermally stable than SLG, one nanometer thick rGO is still sufficient to suppress Cu diffusion under a thermal budget of 400 °C, 30 min annealing. In addition, it is worth mentioning that the patterned Cu lines on SLG suffer from metal drifting because of poor adhesion property of graphene.[9] This requires an additional engineering to improve adhesion between Cu and SLG, which mitigates the advantage of graphene as a Cu barrier material.[25] However, patterned Cu lines can be secured on GO and rGO.

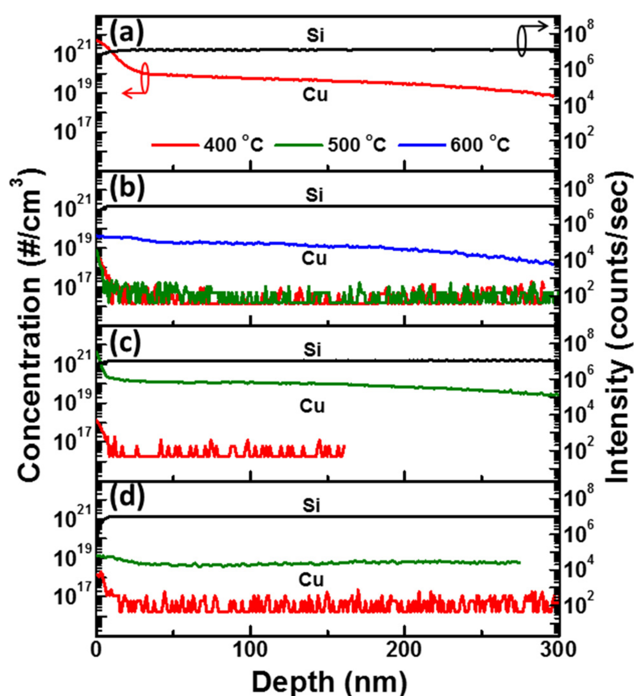



FIG. 5. Back-side SIMS profiles of (a) Cu/Si, (b) Cu/SLG/Si, (c) Cu/GO/Si, and (d) Cu/rGO/Si structures after annealing at various temperatures for 30 min. The measurement was stopped when the concentration of Si started to drastically decrease.

We have investigated the barrier properties of CVD-grown SLG, GO, and rGO layers against Cu diffusion. Although the SLG shows better diffusion barrier performance compared to the GO and rGO layers, the rGO layer effectively suppresses Cu diffusion under a thermal budget of 400 °C, 30 min annealing, which is sufficient for the BEOL process. The ease of preparation of an ultrathin rGO layer and good adhesion with Cu line make rGO a strong candidate for a future barrier material in the Cu metallization process.

This research was supported by Lam Research Corporation research grant.

[1]International Technology Roadmap for Semiconductors—Interconnect, 2007.
[2]K. R. McClain, C. O'Donohue, A. Koley, R. O. Bonsu, K. A. Abboud, J. C. Revelli, T. J. Anderson, and L. McElwee-White, J. Am. Chem. Soc. **136**, 1650 (2014).
[3]A. Lintanf-Salaun, A. Mantoux, E. Djurado, and E. Blanquet, Microelectron. Eng. **87**, 373 (2010).
[4]D. C. Shin, M. R. Kim, J. H. Lee, B. H. Choi, and H. K. Lee, J. Nanosci. Nanotechnol. **12**, 5631 (2012).
[5]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[6]A. K. Geim and K. S. Novoselov, Nat. Mater. **6**, 183 (2007).
[7]B. S. Nguyen, J. F. Lin, and D. C. Perng, Appl. Phys. Lett. **104**, 082105 (2014).
[8]J. Hong, S. Lee, S. Lee, H. Han, C. Mahata, H. W. Yeon, B. Koo, S. I. Kim, T. Nam, K. Byun, B. W. Min, Y. W. Kim, H. Kim, Y. C. Joo, and T. Lee, Nanoscale **6**, 7503 (2014).
[9]Y. J. Shin, Y. Y. Wang, H. Huang, G. Kalon, A. T. S. Wee, Z. X. Shen, C. S. Bhatia, and H. Yang, Langmuir **26**, 3798 (2010).
[10]J. S. Bunch, S. S. Verbridge, J. S. Alden, A. M. van der Zande, J. M. Parpia, H. G. Craighead, and P. L. McEuen, Nano Lett. **8**, 2458 (2008).
[11]H. Y. Kim, C. Lee, J. Kim, F. Ren, and S. J. Pearton, J. Vac. Sci. Technol., B **30**, 030602 (2012).
[12]S. S. Roy and M. S. Arnold, Adv. Funct. Mater. **23**, 3638 (2013).
[13]T. Yoon, J. H. Mun, B. J. Cho, and T. S. Kim, Nanoscale **6**, 151 (2014).
[14]D. Kang, J. Y. Kwon, H. Cho, J. H. Sim, H. S. Hwang, C. S. Kim, Y. J. Kim, R. S. Ruoff, and H. S. Shin, ACS Nano **6**, 7763 (2012).
[15]G. Eda, G. Fanchini, and M. Chhowalla, Nat. Nanotechnol. **3**, 270 (2008).
[16]H. A. Becerril, J. Mao, Z. Liu, R. M. Stoltenberg, Z. Bao, and Y. Chen, ACS Nano **2**, 463 (2008).
[17]J. T. Robinson, M. Zalalutdinov, J. W. Baldwin, E. S. Snow, Z. Q. Wei, P. Sheehan, and B. H. Houston, Nano Lett. **8**, 3441 (2008).
[18]T. V. Cuong, V. H. Pham, Q. T. Tran, S. H. Hahn, J. S. Chung, E. W. Shin, and E. J. Kim, Mater. Lett. **64**, 399 (2010).
[19]J. L. Zhang, H. J. Yang, G. X. Shen, P. Cheng, J. Y. Zhang, and S. W. Guo, Chem. Commun. **46**, 1112 (2010).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 143.248.103.62 On: Wed, 08 Jul 2015 07:26:28

[20]C. A. Chang, J. Appl. Phys. **67**, 566 (1990).
[21]N. Benouattas, A. Mosser, D. Raiser, J. Faerber, and A. Bouabellou, Appl. Surf. Sci. **153**, 79 (2000).
[22]N. Benouattas, A. Mosser, and A. Bouabellou, Appl. Surf. Sci. **252**, 7572 (2006).
[23]S. C. Liang, D. C. Tsai, Z. C. Chang, T. N. Lin, M. H. Shiao, and F. S. Shieu, Electrochem. Solid-State **15**, H5 (2012).
[24]K. H. Min, K. C. Chun, and K. B. Kim, J. Vac. Sci. Technol., B **14**, 3263 (1996).
[25]M. S. Choi, S. H. Lee, and W. J. Yoo, J. Appl. Phys. **110**, 073305 (2011).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 143.248.103.62 On: Wed, 08 Jul 2015 07:26:28