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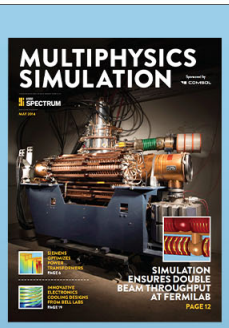

Current density enhancement nano-contact phase-change memory for low writing current

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In this work, a phase-change memory (PCM) with self-assembled nanostructures and an oxidized thin phase-change layer is proposed and intensively investigated for low writing reset current by finite element analysis. Current density is significantly enhanced in our nano-contact memory because of the existence of nanostructures and oxidized phase-change layer. The writing current of our proposed memory is about 1/10-3/10 that of conventional cell, which is in good agreement with our experimental results. The heat efficiency in the nano-contact PCM cell is greatly improved and its power consumption can be as low as about 1/10 that of the conventional cell. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4816080]

Nowadays, nonvolatile memories, which are widely used in our daily lives, are growing demanded. In recent years, the current mainstream flash memory meets serious problems such as its fair scalability and low speed so many prospective memories are proposed and attract much attention worldwide.[1–10] In these memories, phase-change memory (PCM)[11–17] is widely regarded as the best candidate for next-generation non-volatile memories. It is a type of nonvolatile random access memory that stores data by changing the state of the material used between amorphous and crystalline states on a microscopic level. PCM is 500 to 1000 times faster than normal flash memory.[3,10] It exhibits many merits such as nonvolatile operation,[3] high speed,[10] low cost,[1] multilevel storage,[6,9] excellent endurance to cycling,[1,3] great scalability,[5] and good compatibility with silicon fabrication processes.[16,17]

The high writing reset current of PCM is one of the biggest obstacles for its mass production.[18–22] For instance, it is 1.2 mA for PCM cell with a conventional bottom contact electrode, which was fabricated at the 180 nm technology node.[3] How to reduce the operation current, therefore, becomes a critical issue in the worldwide. One of most important solutions is to adopt some phase change materials with a relatively high resistivity in order to improve the heat efficiency in PCM cell via self Joule heating. For example, the resistivity of phase change materials can greatly increased by doping N,[18] C,[19] O,[20] and other elements or co-sputtering[21,22] with insulator such as SiO_2. The other effective solution is to optimize the cell structure. In recent years, researchers proposed some cell structures such as the edge contact, μ-trench cell, and confined chalcogenide cells to reduce the reset current.[23,24] However, compared with the conventional PCM cell,[3] two additional steps of lithography for the formation the oxide in the heater for the μ-trench, and the contact area between $Ge_2Sb_2Te_5$ (GST) and the heater are necessary for the μ-trench cell. As a result, the fabrication of these memory cells is much more complicated than that of the corresponding conventional PCM cell with a normal bottom/top contact.[3,16,23,24] Recently, we experimentally demonstrated the effect of reducing reset current by incorporating the block-copolymer self-assembled nanostructures into the contact hole.[16] However, there is a lack of intensive analysis to explain its mechanism.

In this letter, we intensively analyze the simple PCM cell structure with the block-copolymer self-assembled nanostructures incorporated into the contact hole using finite element method. The nano-contact PCM cell exhibits its ultralow reset current compared with the conventional one due to the great enhancement of current density.

Cross section of our PCM cell for finite element analysis is schematically shown in Fig. 1(a). There is a layer of W on SiO_2/Si substrate as the bottom electrode. A phase-change layer of GST is then formed on the W layer. The SiO_2 hole is fabricated by wet etching which was followed by the formation of nanostructures in the contact hole. The TiN heater is then formed in the contact hole. Finally, a layer of W is deposited as a top electrode.

The difference between our nano-contact and a conventional PCM cell structures is whether there exist nanostructures at the interface between TiN heater and GST layer and a very thin layer of high-resistance O-doped GST (O-GST). The nanostructures can be fabricated by block-copolymer such as Si-containing poly(styrene-b-dimethylsiloxane) (PS-PDMS). It was demonstrated by X-ray photoelectron spectroscopy that the self-assembled PDMS nanostructures can be easily converted into thermally stable and insulating SiO_x nanostructures[25] after reactive ion etching (RIE) with O_2 plasma, and a thin layer of O-GST is certainly formed at the top of GST layer. As shown in Fig. 1(b), a variety of nanostructure shapes are obtained simply by changing the

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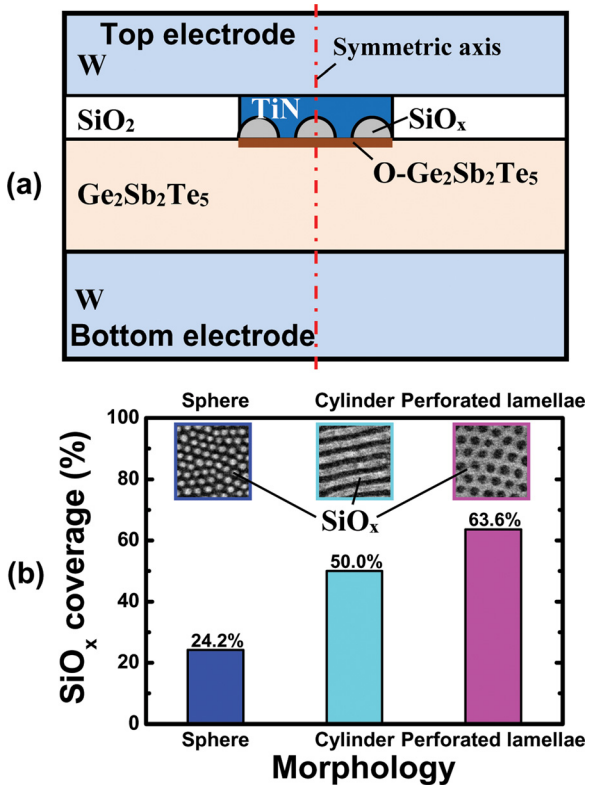

FIG. 1. (a) Cross-sectional diagram of our proposed nano-contact PCM cell with nanostructures introduced into the interface between the TiN heater and the phase-change GST layer. (b) A wide range of SiOx coverage controlled by molecular weight and treatment method.

molecular weight and adopting solvent-vapor treatment and the SiO_x coverage could be controlled over a wide range typically from 24.2% to 50.0%, further to 63.6%.[25,26]

The mathematical model for heat transfer by conduction in the PCM cell is the heat equation:

$$\rho C\frac{\partial T}{\partial t} - \nabla \cdot (k\nabla T) = Q, \tag{1}$$

where ρ is the density, T is the temperature, C is the heat capacity, k is the thermal conductivity, t is the time, and Q is the heat flux. The heat generated by Joule heating Q is given by

$$Q = \frac{1}{\sigma}|J|^2, \tag{2}$$

where σ is the electric conductivity, and J is the electric current density. Equation (1) is solved by finite element method in this study.

The current density, electrical potential, and temperature distributions of nano-contact PCM cell with a contact hole radius of 45 nm at its reset pulse (10 ns, 105 μA) are shown in Figs. 2(a)–2(c), respectively. The nanostructure with a 50.0% SiO_x coverage is typically adopted for the finite element analysis of our proposed PCM cell here. As can be seen from Fig. 2(a), current density in the area of TiN heater between the two adjoining insulated SiO_x nanostructures is highly enhanced. Furthermore, enhancement of current density in the thin O-GST layer can also be clearly observed beneath the gaps between nanostructures. From Eq. (2), the Joule heating should mainly occur in the areas with high current density for the same material. The high temperature regions are certainly expected to be gaps between the two adjoining insulated SiO_x nanostructures and those in O-GST layer beneath the gaps between

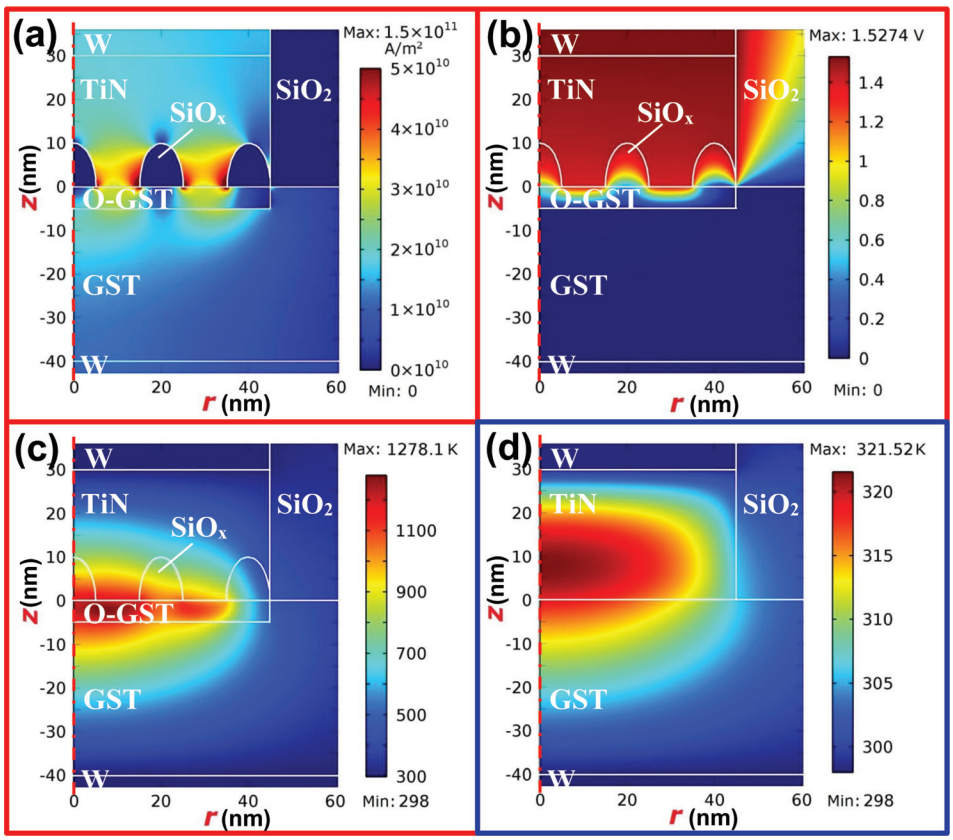

FIG. 2. (a)-(c) Current density, electric potential, and temperature distributions of the nano-contact PCM cell with a contact hole radius of 45 nm at its reset pulse (10 ns, 105 μA), respectively. (d) Temperature distribution of the conventional PCM cell at 105 μA for reference.

nanostructures. Besides, the side effect, that the current density in the regions close to the edges of nanostructures is much higher than that in the middle of gaps of nano structures, was also reasonably observed from Fig. 2(a). The current density usually concentrates at the corners or joints.[27] As shown in Fig. 2(b), along the perpendicular bisector of adjoining insulated SiO_x nanostructures, the electric potential mainly drops in the O-GST layer. The heat generated by Joule heating can be also described as follows:

$$Q = \sigma|\nabla V|^2, \tag{3}$$

where V is the electric potential. Joule heating, therefore, mainly occurs in the regions beneath the gaps between the two adjoining insulated SiO_x nanostructures, which results in the high temperature in these regions in the nano-contact PCM cell. The prediction of high-temperature regions is proved true from Fig. 2(c). The regions of O-GST beneath the gaps between the two adjoining insulated SiO_x nanostructures have a high temperature, which is above the melting point of O-GST, 905 K.[16] It was reported that the doping N into GeTe up to 10 at. % does not change the melting point based on the differential thermal analysis.[28] Here, we reasonably assume that the doping O into GST in a small amount has not great effect on its melting point, and O-GST has the same melting point as the undoped GST. Consequently, application of a 10 ns, 105 μA pulse is enough to raise the temperature in GST to amorphize it and make the cell enter a high-resistance state to complete so-called reset operation of a PCM. On the contrary, the current density in the conventional PCM cell cannot be enhanced due to the lack of insulated SiO_x nanostructures and the electric potential mainly drops in TiN heater. The temperature distribution of the conventional PCM cell is shown in Fig. 2(d). As can be seen, the high temperature region is located in the TiN heater and the highest temperature is as low as 321.5 K at a 10 ns, 105 μA pulse.

Fig. 3(a) shows the detailed profiles of current density at different z's of 0, −2.5, and −5 nm of the nano-contact and conventional PCM cells at a 10 ns, 105 μA pulse. The current density of the nano-contact PCM cell in the phase change layer beneath the gap between adjacent nanostructures can be as large as 2.8×10^{10} A/m^2, which is much larger than that of the conventional PCM cell, around 1.5×10^{10} A/m^2. The heat generated by Joule heating in the nano-contact PCM cell can be 3.5 times that in the conventional PCM cell based on Eq. (2) even if the low electronic conductivity of O-GST is not taken into account. The enhancement of current density in the phase change layer reasonably results in high temperature in the phase change layer beneath the gap between adjacent nano-structures at the end of the current-on of 10 ns, 105 μA pulse, as shown in Fig. 3(b). For instance, the temperature in the nano-contact PCM cell can be 1275 K at the position of $z = -2.5$ nm and $r = 7$ nm, much higher than that of the conventional cell, 319 K.

The highest temperature in phase change layer T_{high} as a function of the programming current I_p is shown in Fig. 4(a). The highest temperature of each PCM cell with a

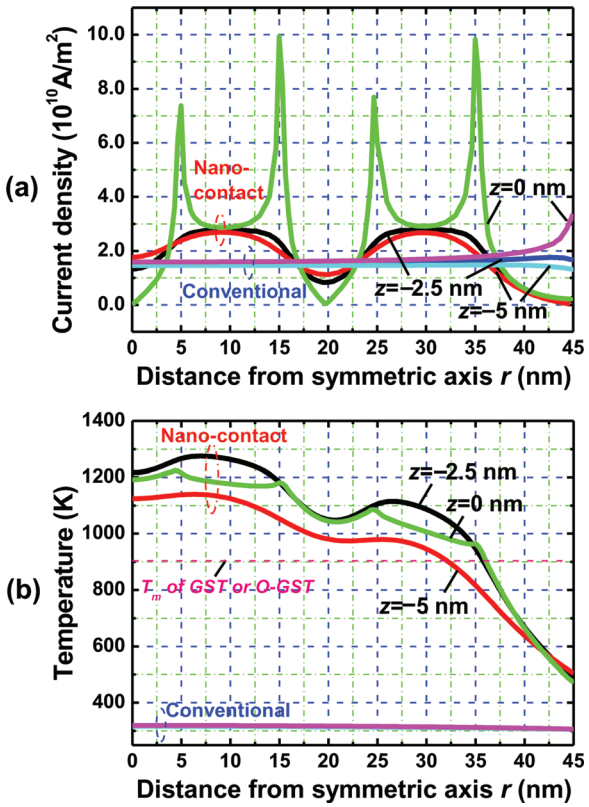

FIG. 3. (a) Current density profiles in the radius direction of the nano-contact and conventional PCM cells at 105 μA. (b) Temperature profiles in the radius direction of the nano-contact and conventional PCM cells at the end of current-on of the 10 ns, 105 μA pulse.

contact hole radius of 45 nm increases with the programming current. It is very clear from the trends of the curves that T_{high} of nano-contact PCM cell should be much higher than that of the conventional cell at the same programming currents. The huge difference of the highest temperatures between the two cells results from the concentration of Joule heating due to the above-described enhancement of current density and low electric conductivity of O-GST based on Eq. (2). The cell resistance as a function of the programming current for cells with a contact hole radius of 45 nm is shown in Fig. 4(b). The resistance of nano-contact PCM cell is initially as low as $1.5 \times 10^4\Omega$, increases to $3.3 \times 10^5\Omega$ at 100 μA, and further up to $4.8 \times 10^7\Omega$ at 105 μA. The reset current I_{reset} of the nano-contact PCM cell, at which the PCM cell enters the high-resistance state, is 105 μA. Similar increase in cell resistance can be observed in the conventional PCM cell but its reset current is 1000 μA, about 10 times that of the nano-contact PCM cell. Fig. 4(c) shows the writing reset current change with the contact hole radius scaling from 1000 nm down to 22.5 nm of both nano-contact and conventional cells. The reset current significantly decreases with scaling down. For instance, the reset current $I_{reset\text{-}nc}$ of the nano-contact PCM cell drops from 3.6×10^4 μA to 105 μA, and further to 55 μA with contact hole radius scaling from 1000 nm down to 45 nm and then to 22.5 nm, respectively. More importantly, the reset current of the nano-contact PCM cell is as low as about 1/10-3/10 of that ($I_{reset\text{-}c}$) of the conventional PCM cell, which is in good agreement with experimental

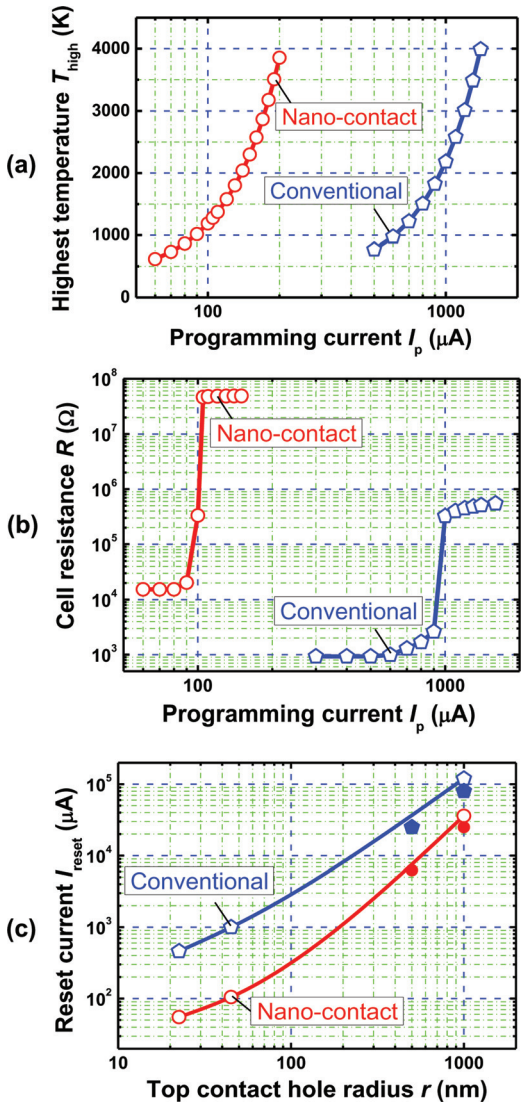

FIG. 4. (a) Highest temperature as a function of the programming current for PCM cells with a contact hole radius of 45 nm. (b) Cell resistance as a function of programming current for PCM cells with a contact hole radius of 45 nm. (c) Reset current as a function of the contact hole radius. Experimental results (solid symbols) are in good agreement with simulated results (empty symbols) for PCM cells.

results,[16] solid symbols shown in Fig. 4(c). The device structure used in this analysis is very close to the one used in our previous experiments. And especially, it was well confirmed that the self-assembled nanostructures existed above GST layer in the contact hole in the final device structure by scanning electron microscopy and transmission electron microscopy.[16] The reset current ratio ($I_{\text{reset-nc}}/I_{\text{reset-c}}$) generally becomes small with scaling down based on our analysis and experiments. This means that the writing reset current can be effectively reduced owing to the current density enhancement as well as the low electronic conductivity of O-GST. Furthermore, the consumption power ($P = I_{reset}^2 \cdot R_{set}$, where R_{set} is the low resistance at the set state) of the nano-contact cell can be also reduced to about 1/10 that of the conventional cell due to the small programming volume during reset operation. It should be noted that the writing current is expected to be reduced further by adopting high SiO_x coverage of 63.6%, as mentioned above. Our fabrication of nanostructures with about 5–8 nm will allow this work to be practically applied in the future.[29]

In summary, a low writing current PCM cell was proposed in the study, in which self-assembled nanostructures were introduced into the interface between the phase change layer and the heater. Finite element analysis exhibited that the current density can be greatly enhanced in the gaps between the adjacent nanostructures and in the phase change layer underneath the gaps. The current density enhancement as well as the low electronic conductivity of the thin modified GST layer contributes to the reduction of the writing reset current and power consumption.

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[1]M. H. R. Lankhorst, B. W. S. M. M. Ketelaars, and R. A. M. Wolters, Nature Mater. **4**, 347 (2005).
[2]D. S. Chao, C. H. Lien, C. M. Lee, Y. C. Chen, J. T. Yeh, F. Chen, M. J. Chen, P. H. Yen, M. J. Kao, and M. J. Tsai, Appl. Phys. Lett. **92**, 062108 (2008).
[3]S. Lai and T. Lowrey, Tech. Dig. - Int. Electron Devices Meet. **2001**, 36.5.1.
[4]T. Hasegawa, N. Alpana, T. Ohno, K. Terabe, T. Tsuruoka, J. K. Gimzewski, and M. Aono, Appl. Phys. A: Mater. Sci. Process. **102**, 811 (2011).
[5]J. Liu, B. Yu, and M. P. Anantram, IEEE Electron Device Lett. **32**, 1340 (2011).
[6]Y. Yin, T. Noguchi, H. Ohno, and S. Hosaka, Appl. Phys. Lett. **95**, 133503 (2009).
[7]L. Wu, Z. Song, F. Rao, Y. Gong, and S. Feng, Appl. Phys. Lett. **94**, 243115 (2009).
[8]R. Pandian, B. J. Kooi, G. Palasantzas, J. T. M. D. Hosson, and A. Pauza, Appl. Phys. Lett. **91**, 152103 (2007).
[9]Y. Yin and S. Hosaka, Appl. Phys. Lett. **100**, 253503 (2012).
[10]G. Bruns, P. Merkelbach, C. Schlockermann, M. Salinga, M. Wuttig, T. D. Happ, J. B. Philipp, and M. Kund, Appl. Phys. Lett. **95**, 043108 (2009).
[11]Y. Yin, T. Noguchi, and S. Hosaka, Jpn. J. Appl. Phys., Part 1 **50**, 105201 (2011).
[12]X. Zhou, L. Wu, Z. Song, F. Rao, Y. Cheng, C. Peng, D. Yao, S. Song, B. Liu, S. Feng, and B. Chen, Appl. Phys. Lett. **99**, 032105 (2011).
[13]Y. Yin, N. Higano, H. Sone, and S. Hosaka, Appl. Phys. Lett. **92**, 163509 (2008).
[14]M. Li, R. Zhao, L. T. Law, K. G. Lim, and L. Shi, Appl. Phys. Lett. **101**, 073502 (2012).
[15]D. Loke, T. H. Lee, W. J. Wang, L. P. Shi, R. Zhao, Y. C. Yeo, T. C. Chong, and S. R. Elliott, Science **336**, 1566 (2012).
[16]W. I. Park, B. K. You, B. H. Mun, H. K. Seo, J. Y. Lee, S. Hosaka, Y. Yin, C. Ross, K. J. Lee, and Y. S. Jung, ACS Nano **7**, 2651 (2013).
[17]Y. Lu, S. Song, Z. Song, F. Rao, L. Wu, M. Zhu, B. Liu, and D. Yao, Appl. Phys. Lett. **100**, 193114 (2012).
[18]Y. Yin, H. Sone, and S. Hosaka, J. Appl. Phys. **102**, 064503 (2007).
[19]G. B. Beneventia, L. Perniola, V. Sousa, E. Gourvest, S. Maitrejean, J. C. Bastien, A. Bastard, B. Hyot, A. Fargeix, C. Jahan *et al.*, Solid State Electron. **65–66**, 197 (2011).
[20]N. Matsuzaki, K. Kurotsuchi, Y. Matsui, O. Tonomura, N. Yamamoto, Y. Fujisaki, N. Kitai, R. Takemura, K. Osada, S. Hanzawa *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2005**, 738.
[21]S. W. Ryu, J. H. Oh, J. H. Lee, B. J. Choi, W. Kim, S. K. Hong, C. S. Hwang, and H. J. Kim, Appl. Phys. Lett. **92**, 142110 (2008).
[22]D. Lee, S. S. Yim, H. K. Lyeo, M. H. Kwon, D. Kang, H. G. Jun, S. W. Nam, and K. B. Kim, Electrochem. Solid State Lett. **13**, K8 (2010).
[23]A. Pirovanoa, F. Pellizzera, I. Tortorellia, A. Riganóa, R. Harriganb, M. Magistrettia, P. Petruzzaa, E. Varesia, A. Redaellia, D. Erbettaa *et al.*, Solid-State Electron. **52**, 1467 (2008).

[24]Y. Yin, H. Sone, and S. Hosaka, Jpn. J. Appl. Phys., Part 1 **45**, 6177 (2006).
[25]W. I. Park, J. M. Yoon, M. Park, J. Lee, S. K. Kim, J. W. Jeong, K. Kim, H. Y. Jeong, S. Jeon, K. S. No *et al.*, Nano Lett. **12**, 1235 (2012).
[26]W. I. Park, K. Kim, H. I. Jang, J. W. Jeong, J. M. Kim, J. Choi, J. H. Park, and Y. S. Jung, Small **8**, 3762 (2012).
[27]Y. Liu, Z. song, Y. Ling, Y. Gong, and S. Feng, Jpn. J. Appl. Phys., Part 1 **48**, 024502 (2009).
[28]A. Fantini, V. Sousa, L. Perniola, E. Gourvest, J. C. Bastien, S. Maitrejean, S. Braga, N. Pashkov, A. Bastard, B. Hyot *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2010**, 29.1.1.
[29]M. Huda, J. Liu, Y. Yin, and S. Hosaka, Jpn. J. Appl. Phys., Part 1 **51**, 06FF10 (2012).