Development of a Digitalized Position Decoder Circuit for Brain PET consisting of Silicon Photomultiplier

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***Abstract*– This paper presents a circuit of a digitized position decoder circuit for brain PET consisting of Silicon Photomultiplier (SiPM). Difference of proposed circuit and traditional circuit is the existence of analog-to-digital convertor (ADC). In this work, we conclude that the combination of ADC, field programmable gate array (FPGA) and digital data acquisition (DAQ) board can be substitute for an existing analog DAQ.**

I. INTRODUCTION

Images of various brain diseases are very valuable for brain research. At the same time, manufacturing a brain diagnosis equipment with the low price and high accuracy becomes an important matter. Nowadays Positron emission tomography (PET) is a dominant diagnosis equipment for a brain. Generally, PET consists of sensors, preamps, position decoder circuits (PDC) and data acquisition (DAQ) system.

The silicon photomultiplier (SiPM) is a kind of solid-state photo sensor. It is consist of Geiger mode avalanche photodiodes (GAPD). These GAPD were coupled with the others by a quenching resistor and have a high gain (~10^6). Also it is operated at low voltage (25~70 V) than a photomultiplier tube (PMT). Besides there is no effect of signal in a magnetic field. Above these advantage, several group are conducting in development in PET-MR using SiPM modules. The module is made up SiPM array.[1-4]

Generally, a positron emission tomography (PET) system processes analog signals from the SiPM modules. Also, those signal is handled by analog data acquisition board (DAQ).

In terms of total production cost of PET, DAQ system takes possession of great importance from among those components. In these reason, it is essential to reduce production cost of DAQ system for cutting down one of PET. In this work, we develop a PDC to adapt DAQ system using digital ports. Designed PDC was based on a field programmable gate arrays (FPGA). Also the PDC output is sum of bit streams of ADC and an identity of each channel. This work can change the input of DAQ system to only digital signals. As a result of above transition, it have no use for a pulse restoration circuit. Also it can reduce the cost and the volume of PET.

II. METHODS

2.1 Structure

A traditional PDC included offset voltage level control, gain adjust, signal delay, signal switching, energy discrimination, and digital signal processing. [5] In the proposed PDC, a multiplexer (MUX) and ADC added on the traditional PDC.

Signals are amplified by preamps. The amplified signals of sensors are divided into both comparator and delay circuit. In case of comparator, if signal of comparator's input is larger than low-level discriminator (LLD) of comparator, delayed signals are fed into MUX. A position of operated comparator is memorized by FPGA, then it decide a select signal of MUX. The signal passed through MUX fed into ADC, then the output of ADC is signal energy information. And this signal is combined with above digital stream and position and time information. In these process, the output of PDC is consist of only digital bit stream. Therefore, it don't need an analog DAQ board.

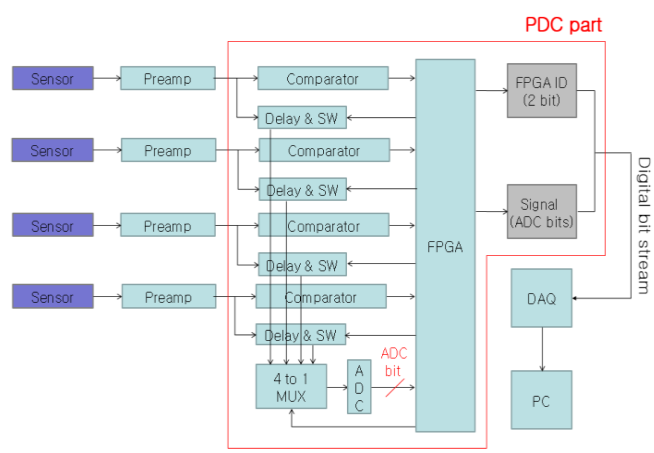

Figure 1 Block diagram of 4 to 1 PET module

2.2 FPGA part

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We used Xilinx spartan2 and the function are programed base on Verilog hardware descript language (HDL). FPGA part has three constraint mainly. First, system detect fired SiPM for the first time. It is the most effective signal of SiPM module. Secondly, the system don't receive in system processing time. Typically, processing time is 100ns and can be modified according to the need of situation. Finally, the system ignore signals detecting at same time. These constraint is described by figure 2.

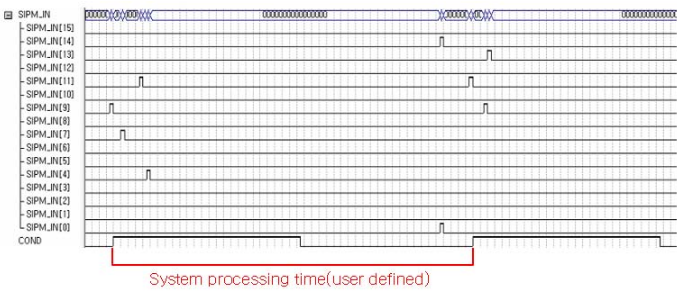

Figure 2 Example of functional diagram

2.3 Analog circuit part

A preamp and a delay circuit was designed operational amplifers. The preamp is adjustable and the delay circuit has a constanst group dealy of 32ns.

Firgure 3 is decribed the output of amplified signal for SiPM and Firgure 4 is the output of ADC

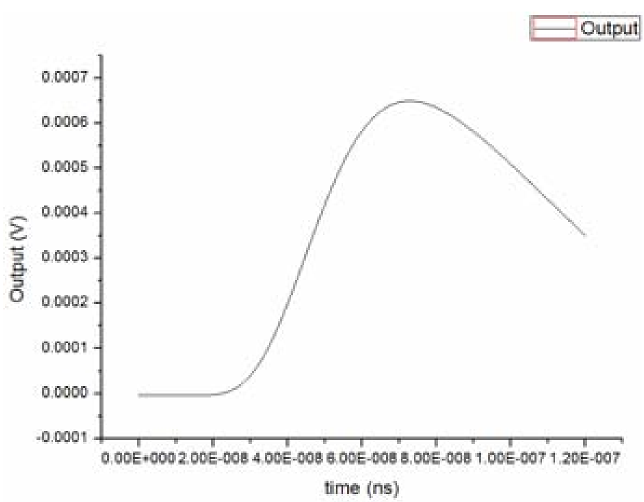

Figure 3 Output of amplified SiPM

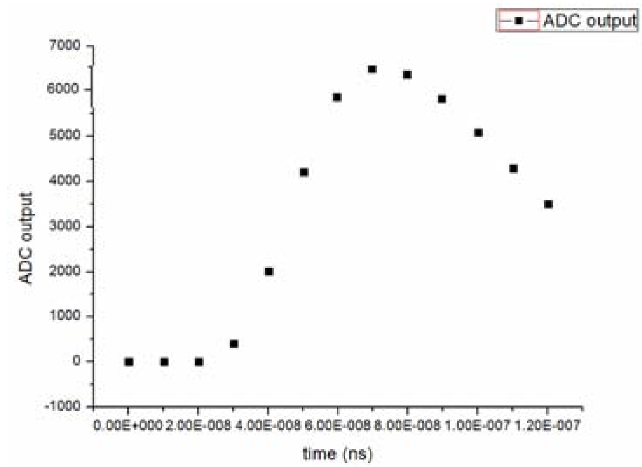

Figure 4 Output of ADC

Through two result, we can find that Out of ADC is enough to reconstruct the output of SiPM. ADC output value is up to set-up of ADC.

III. CONCLUSION

We simulated the front-end ASIC part and fabricated FPGA part. In case of front-end ASIC, commercial op. amp was used to simulate circuit. And FPGA was programmed using Verilog HDL and it meet all PET constraints.

In fact, we are scheduled to estimate time resolution and energy resolution thereby 4 to 1 digitalized PDC module originally. Unfortunately, we didn't assess time resolution and energy resolution.

However, as this work we can confirm that the combination of ADC, FPGA and digital DAQ boards can be substitute for the analog DAQ.

Therefore we study this work continuously and develop this part to application-specific integrated circuit

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