Suppression of Power/Ground Inductive Impedance and Simultaneous Switching Noise Using Silicon Through-Via in a 3-D Stacked Chip Package

Chunghyun Ryu, Jiwoon Park, Jun So Pak, Kwangyong Lee, Taesung Oh, and Joungho Kim

***Abstract*—We have thoroughly investigated the advantages of a silicon through-via (STV) interconnection in decreasing the inductive impedance of a power distribution network (PDN) and suppressing simultaneous switching noise (SSN) in a 3-D stacked chip package. A double-stacked chip package with STV interconnections was fabricated and measured together with a similar double-stacked chip package with conventional bonding-wire interconnections. We successfully demonstrated that significant reduction of the inductive PDN impedance, from 1.66 nH to 0.79 nH, can be achieved by replacing the conventional bonding wires in the multiple-stacked chip package by STV interconnections. Furthermore, we have shown that the STV interconnections can considerably reduce high-frequency SSN, by more than 80%, compared to the conventional bonding-wire interconnections.**

***Index Terms*—Power distribution network (PDN) impedance, silicon through-via (STV), simultaneous switching noise (SSN), 3-D stacked chip package.**

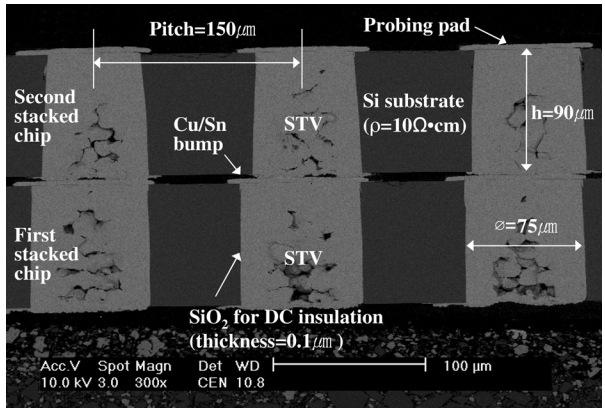

Fig. 1. Cross-sectional view of the fabricated STVs in the double-stacked chip package.

I. Introduction

THERE is a strong demand for 3-D high-density stacked chip packages that vertically integrate multiple semiconductor chips and passive components in a single package. These packages are suitable for small and lightweight mobile electronic products, such as mobile phones, personal digital assistants (PDAs), and digital cameras, as they allow considerable space savings and significant downsizing [1]. As the packages are beginning to include high-speed and high-current integrated circuits (ICs), distribution of stable power supply voltages and suppression of simultaneous switching noise (SSN) in the power supply network have become critical design issues. However, conventional bonding-wire interconnections for the power/ground delivery networks in the 3-D stacked chip packages can generate significant SSN above a frequency of a few hundred megahertz, due to large parasitic inductance that is in the order of nH. Although the 3-D stacked chip packages have on-package discrete decoupling capacitors to reduce the SSN by providing a low-inductance power supply and return current paths, the suppression effect of the discrete decoupling capacitors is not sufficient above a few hundred megahertz due to large equivalent series inductance (ESL) [2].

A silicon through-via (STV) for a vertical interconnection structure is an outstanding interconnection candidate for the 3-D stacked chip package to lower the inductive interconnection impedance between chips, passives, and package substrates for signal, power, and return current path connections. Furthermore, it allows enhanced packaging integration techniques, such as wafer-level 3-D packaging and stacking of various types of microcomponents mounted directly on CMOS chips [3].

In this letter, we describe a thorough investigation of the prominent advantages of the STV in reducing the inductive power distribution network (PDN) impedance and in suppressing the SSN in the 3-D stacked chip package. A double-stacked chip package with STV interconnections was fabricated, measured, and compared together with a similar double-stacked chip package with conventional bonding-wire interconnections.

II. Structure of Test Devices

A cross-sectional view from a scanning electron micrograph of the fabricated STV interconnections in the 3-D stacked chip package is shown in Fig. 1. Copper vias had a diameter of 75 μm, a height of 90 μm, and a pitch of 150 μm, and were formed on a p-type silicon substrate with a resistivity of 10 $\Omega\cdot$ cm. A thin SiO_2 insulating layer of 0.1 μm thickness was deposited on the silicon via wall using a dry oxidation method to form a dc insulation layer between the Cu via

Manuscript received April 23, 2007; revised August 20, 2007. This work was supported by the Center for Electronic Packaging Materials (ERC) of MOST/KOSEF and the Joint Laboratory Program for CEPM-Fraunhofer IZM under Grants R11-2000-085-07001-0 and R11-2000-085-00001-0.

C. Ryu, J. Park, J. S. Pak, and J. Kim are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: sdomain@eeinfo.kaist.ac.kr).

K. Lee and T. Oh are with Hongik University, Seoul, Korea.

Digital Object Identifier 10.1109/LMWC.2007.910485

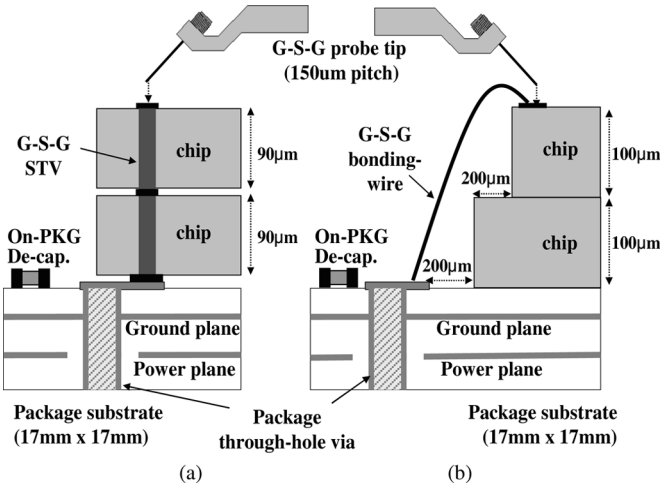

Fig. 2. Test devices for the PDN impedance measurement: (a) a double-stacked chip package with STVs and (b) a double-stacked chip package with conventional bonding wires.

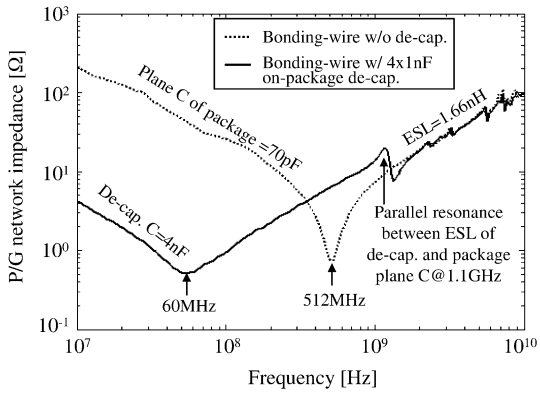

Fig. 3. Measured PDN impedance curves of the structure shown in Fig. 2(b).

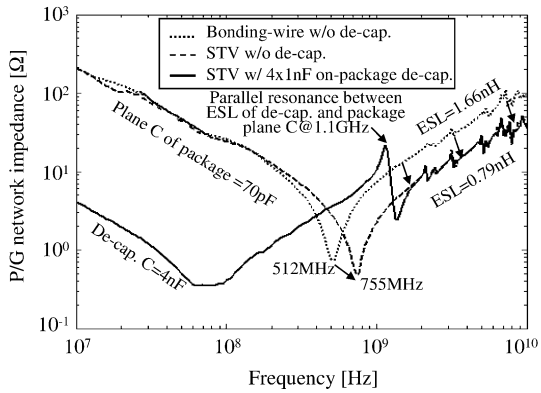

Fig. 4. Measured PDN impedance curves of the structures shown in Fig. 2.

barrel and the silicon substrate. The test device to measure the PDN impedance consisted of two stacked chips and a package substrate, as shown in Fig. 2(a). The test device had a lateral ground—signal—ground (G-S-G) STV configuration for high-frequency microprobing. Cu/Sn bumps were used to connect the G-S-G STV interconnections vertically.

The Cu/Sn bumps were also used to connect the G-S-G STV of the first stacked chip to pads on the test package substrate. The diameter and height of the Cu/Sn bumps were 100 μm and 3 μm, respectively. The pads on the package, which were bonded to the STVs, were connected to the ground and power planes at the package substrate using through-hole vias. Using a combination of ceramic and PTFE as the dielectric material, the dielectric permittivity of the package substrate was 4.5. The test package substrate had a four-layer stack. The ground and power planes were sandwiched between a top signal layer and a bottom signal layer, with dielectric thickness of 580 μm $-$380 μm $-$580 μm. The test package substrate had four pairs of pads for mounting decoupling capacitors on the top signal layer. To compare the PDN impedance of the STVs with that of conventional bonding wires, a test device, as shown in Fig. 2(b), was also fabricated. The test device with the bonding wires in Fig. 2(b) had an identical package substrate to that of the STVs shown Fig. 2(a).

III. Measurement Results and Discussion

In order to measure PDN impedances accurately with a milliohm-scale for the test devices, a two-port self-impedance measurement technique was used [4]. Plots of the measured PDN impedance curves (Z_{11}) are shown in Fig. 3 for two different cases of the test devices with the bonding wires as shown in Fig. 2(b). The dotted curve represents the impedance of the double-stacked chip package with the bonding wires without any on-package decoupling capacitor. The PDN impedance curve exhibits a capacitive behavior due to the power/ground plane cavity in the package substrate at frequencies below 512 MHz. Then, at a frequency of 512 MHz, a series resonant peak is observed, which occurs due to a serial resonance between the package plane cavity capacitance and the equivalent series inductance (ESL) of the package power/ground interconnections, while these inductive interconnections include the power/ground plane, the package through-hole vias, the bonding pads, and the bonding wires. At frequencies above this serial resonant frequency, the ESL dominates the PDN impedance behavior. The small resonance features occurring at frequencies in the gigahertz frequency range originate from multimode cavity resonances at the power/ground plane cavity in the package substrate. The solid curve in Fig. 3 represents the measured PDN impedance for the double-stacked chip package with the same bonding wires as in Fig. 2(b), but with four on-package decoupling capacitors with a total capacitance of 4 nF. The discrete decoupling capacitors exhibit a decoupling role at frequencies below 60 MHz.

However, at 1.1 GHz, a new high-impedance resonant peak is created due to a parallel resonance between the package plane cavity capacitance and the combined ESL from the discrete capacitors, the discrete capacitor-mounting pads, and the necessary power/ground through-hole vias. It should be noted that the discrete capacitors are no longer effective in reducing the inductive PDN impedance above a few hundred megahertz.

In contrast, using the STVs in the stacked chip package, as displayed in Fig. 2(a), we achieved a significant reduction in the ESL of the PDN at frequencies above 755 MHz, as shown by the dashed curve in Fig. 4. The magnitude of the ESL at the PDN was reduced from 1.66 nH to 0.79 nH by using the STVs. The reduction in the ESL at the PDN is obtained by the elimination of the inductance caused by the bonding wires. In

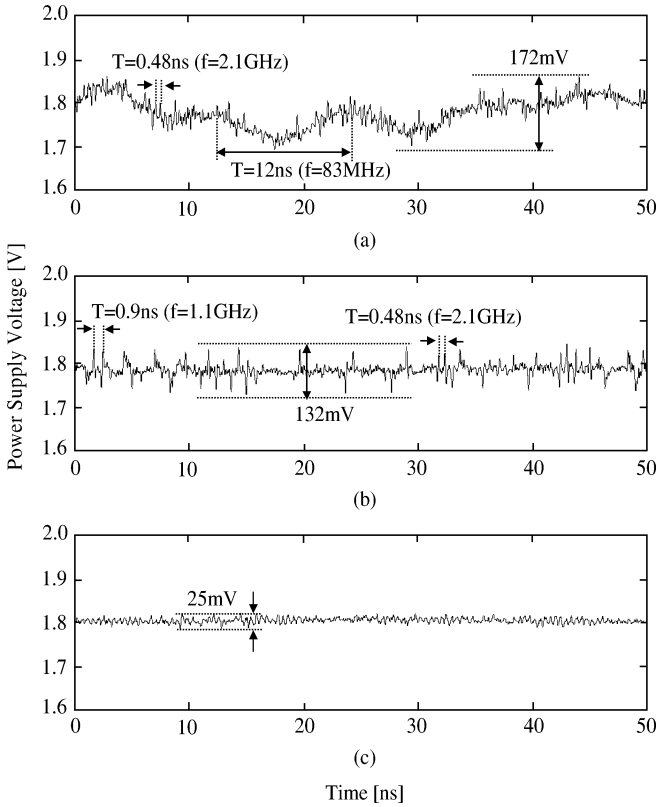

Fig. 5. Measured power supply noise excited by a pseudorandom bit sequence of 1.5 Gbps: (a) the double-stacked chip package with bonding wires without on-package decoupling capacitors, (b) the double-stacked chip package with bonding wires with four on-package decoupling capacitors with a total of 4 nF, and (c) the double-stacked chip package with STVs with four on-package decoupling capacitors with a total of 4 nF.

the graph, we also found that the series resonant peak occurring at 512 MHz was shifted to 755 MHz because of the reduced ESL using the STV. When the discrete decoupling capacitors were attached to the test device with the STVs, we could further reduce the PDN impedance below a frequency of 400 MHz. However, the on-package discrete decoupling capacitors create the same parallel resonant peak at 1.1 GHz, as shown by the solid curve in Fig. 3. This shows that the discrete decoupling capacitors must be carefully designed on the package substrates.

Fig. 5 presents the measured SSN waveforms excited by a digital switching signal with a 1.5 Gbps pseudorandom bit sequence (PRBS). This PRBS digital data pattern was injected in the top probing pads of the double-stacked chip packages, as shown in Fig. 2. The SSN waveforms were measured at the same top probing pads in Fig. 2 using a high-impedance active probe connected to a real-time oscilloscope. Therefore, it can be said that the measured voltage waveforms in Fig. 5 are responses of the power distribution networks for the PRBS digital data switching current. Switching noise of 172 mV peak-to-peak was observed in the double-stacked chip package with the bonding wires without any decoupling capacitor, as illustrated in Fig. 5(a). The measured SSN waveform in Fig. 5(a) revealed various frequency components for the 1.5 Gbps PRBS data pattern excitation, and several noise frequency components were indicated in the graph.

Meanwhile, Fig. 5(b) indicates that the implementation of the on-package decoupling capacitors could reduce the SSN from 172 mV peak-to-peak to 132 mV peak-to-peak in the double-stacked chip package with the bonding wires. However, the high-frequency noise components in the gigahertz range, which were originated from the multimode cavity resonances of the package substrate were still maintained in the SSN waveform. It is because the discrete decoupling capacitors were not effective above a frequency of a few hundred megahertz due to the ESL of the decoupling capacitors. Conversely, the STVs on the double-stacked chip package prove a noticeable suppression of the SSN over the gigahertz frequency range, as shown in Fig. 5(c). Consequently, by combining the STVs and the discrete on-package decoupling capacitors on the 3-D stacked chip package, the SSN could be reduced by more than 80%, from 132 mV peak-to-peak to 25 mV peak-to-peak.

IV. Conclusion

We have successfully demonstrated that the use of the STV is a suitable design approach for the suppression of the inductive PDN impedance and the corresponding SSN in a 3-D stacked chip package. The main cause of these benefits is the elimination of the parasitic inductance of the conventional bonding-wire interconnections using vertical STV interconnections. These advantages are convincing and effective in the frequency ranges dominated by the inductive behavior of the PDN impedance where the on-package discrete decoupling capacitors are not effective. As the number of the stacked chips and the data rate of ICs increase in the 3-D stacked chip packages, the bonding-wire interconnections will soon reach their limits. Then the STV interconnections can play a substantial role in providing stable power supply voltages.

References

[1] S. F. Al-sarawi, D. Abbott, and P. D. Franzon, "A review of 3-D packaging technology," *IEEE Trans. Compon., Packag., Manufact. Technol.*, vol. 21, no. 1, pp. 2–14, Feb. 1998.

[2] J. Lee, H. Kim, and J. Kim, "High dielectric constant thin film EBG power/ground network for broad-band suppression of SSN and radiated emissions," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 8, pp. 505–507, Aug. 2005.

[3] D. Henry, D. Belhachemi, J.-C. Souriau, C. Brunet-Manquat, C. Puget, G. Ponthenier, J. L. Vallejo, C. Lecouvey, and N. Sillon, "Low electrical resistance silicon through vias: Technology and characterization," in *Proc. 56th Electron. Comp. Technol. Conf.*, San Diego, CA, May/Jun. 2006, pp. 1360–1366.

[4] I. Novak, "Measuring milliohms and picohenrys in power-distribution networks," presented at the DesignCon'00, Feb. 2000 [Online]. Available: http://www.home.att.net/~istvan.novak/papers/dc2000_slides.pdf