Matrix Substitution Method for Power Bus Analysis With Isolated Power Island in High-Speed Packages and PCBs

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***Abstract*—We propose a matrix substitution method for analyzing a power bus containing a power island in high-speed packages and printed circuit boards (PCBs). The method is based on a segmentation method and a resonant cavity model for a rectangular cavity, and the impedance of the power bus containing the power island can be calculated analytically. Finally, the proposed method is verified by means of impedance measurements in the frequency domain.**

***Index Terms*—Matrix substitution method, resonant cavity model, segmentation method, simultaneous switching noise.**

I. INTRODUCTION

AN INCREASE in simultaneous switching noise, consistent with high system operating frequency and high power consumption, has been identified as the bottleneck of system performance. In high-frequency power bus design in packages and printed circuit boards (PCBs), an isolation technique using a power island has generally been used for effectively minimizing the switching noise, in addition to techniques using decoupling capacitors. Accordingly, many simulation methods have been proposed for analyzing the characteristics of the power bus containing the power island, before applying the structures to practical packages and PCBs. These methods include the transmission line method (TLM) [1] and two- (2-D) or three-dimensional (3-D) full-wave numerical methods, such as finite-difference time-domain (FDTD), finite element method (FEM), and method of moments (MOM) [2], [3]. A TLM is an efficient simulation method for the characterization of a power bus because of its short simulation time and high accuracy. However, a uniform grid step in a TLM causes simulation errors when components or sources are connected to the model, and a SPICE simulator is required for simulation using a TLM. On the other hand, although we can accurately analyze any power bus structures using full-wave numerical methods, such methods are relatively complex, and significant simulation time and resources are required. To overcome the limitations of the analysis methods mentioned above, many analytical approaches have been developed, and analytical solutions for simple power bus structures, such as rectangular power/ground planes, have been derived and used widely [4]. Furthermore, a segmentation method was proposed for analyzing complex power bus structures, such as the irregular power/ground plane structure, and this enables the impedance calculation of complex power bus structures using the resonant cavity model of rectangular power/ground planes [4], [5]. In this letter, we propose a fast and accurate analytical calculation method using a matrix substitution method based on the segmentation method and the resonant cavity model. With the proposed method, we can calculate the impedance of a power bus structure containing a power island, with relative ease.

II. PROPOSED ANALYTICAL MODELING METHOD FOR POWER BUS ANALYSIS WITH ISOLATED POWER ISLAND

A. Resonant Cavity Model for Rectangular Power/Ground Planes

In this letter, the basic impedance calculations are based on the resonant cavity model for rectangular power/ground planes. Using the modal (1), which is based on the resonant cavity model, we can calculate the self—and transfer impedances at arbitrary ports on rectangular power/ground planes, rapidly, and accurately [4]

$$\begin{aligned} Z_{ij} = j\omega\mu h \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} & \frac{C_m^2 C_n^2}{ab\left(k_{xm}^2 + k_{yn}^2 - k^2\right)} \\ & \times \cos(k_{xm}x_i)\cos(k_{yn}y_i)\cos(k_{xm}x_j)\cos(k_{yn}y_j) \\ & \times \sin c\left(\frac{k_{xm}dx_i}{2}\right)\sin c\left(\frac{k_{yn}dy_i}{2}\right) \\ & \times \sin c\left(\frac{k_{xm}dx_j}{2}\right)\sin c\left(\frac{k_{yn}dy_j}{2}\right) \end{aligned} \quad (1)$$

m	mth mode associated with the x dimension;
n	nth mode associated with the y dimension;
a, b	metal plane widths in the x and y directions, respectively;
$(x_i, y_i), (x_j, y_j)$	coordinates of the ith and jth ports
$(dx_i, dy_i), (dx_j, dy_j)$	port widths of the ith and jth ports
k	wave number, $(k_{xm} = m\pi/a, k_{yn} = n\pi/b)$.

The constant $C_m^2 C_n^2 = 1$ for $m = n = 0; C_m^2 C_n^2 = 2$ for $m = 0, n \neq 0$ or $m \neq 0, n = 0; C_m^2 C_n^2 = 4$ for $m \neq 0, n \neq 0$.

B. Matrix Substitution Method

Fig. 1 shows the concept of the matrix substitution method. As shown, we can obtain a power bus structure containing a hole by subtracting the hole structure from the solid power bus structure, and we can calculate the impedance of the power bus,

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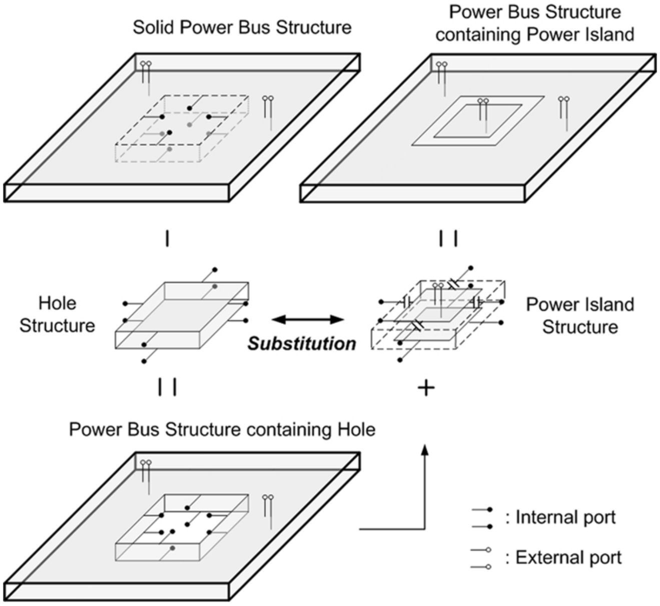

Fig. 1. Concept of the matrix subsitution method.

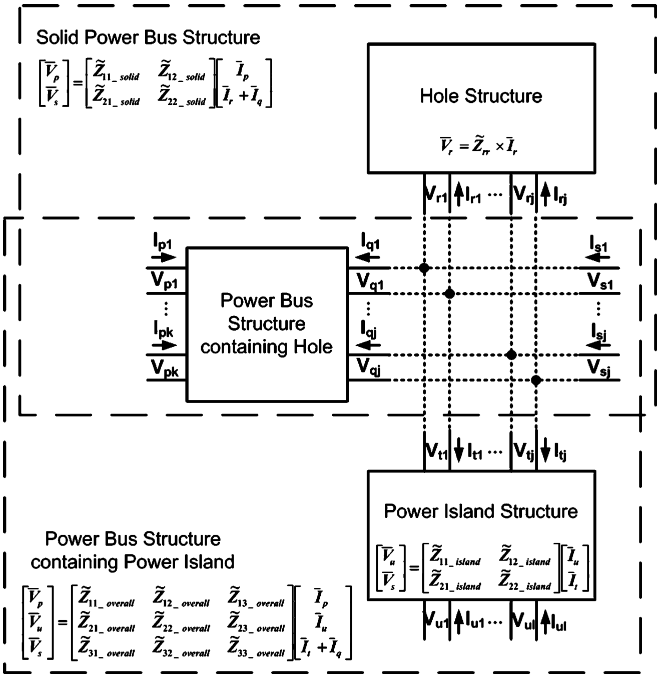

Fig. 2. Solid power bus structure containing a hole and a hole structure and one containing a power island consisting of a power bus structure including a hole and a power island structure.

which contains the hole, using the voltage and current relations at external and internal ports [6]. In this concept, the hole structure means a small solid power bus structure with the same shape and size of the hole, and the impedances of this hole structure can be calculated by the expression (1). In this letter, we extend this concept for the analysis of a power bus containing a power island. As shown in Fig. 1, we can obtain the power bus structure containing a power island by adding the latter to the one containing a hole, and we can obtain the impedance matrices of such power bus structures substituting the impedance matrices of the hole structure with those of the power island.

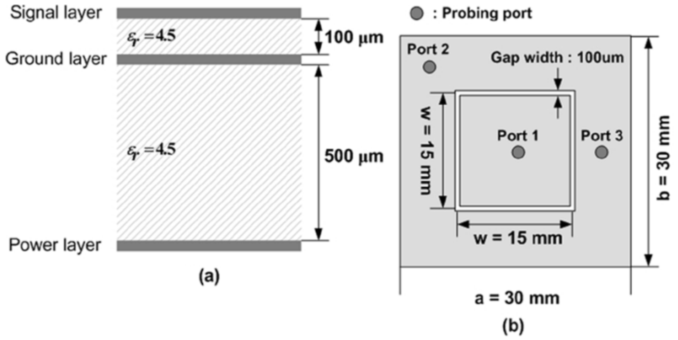

Fig. 3. Test package substrate. (a) Cross section of the test package substrate. (b) Top view of the power layer.

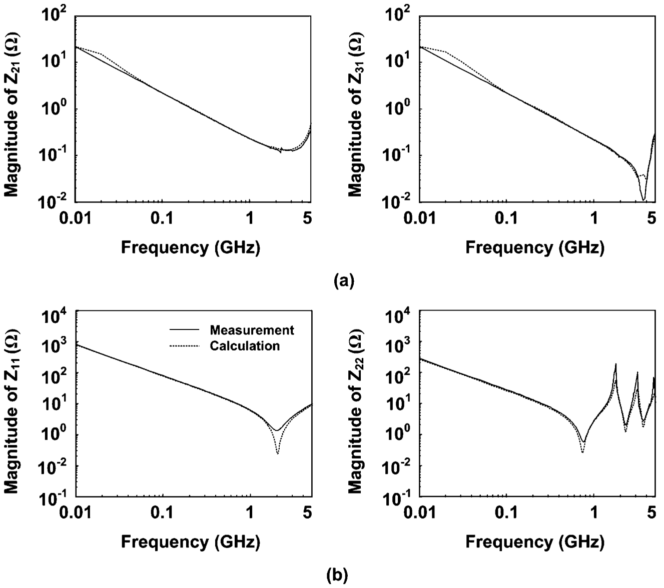

Fig. 4. Comparison of calculated and measured results. The solid line represents the calculated impedances using the proposed method, whereas the dotted line represents the impedance obtained from these measurements. (a) Transfer impedances (Z_{21} and Z_{31}). (b) Self impedances. (Z_{11} and Z_{22}).

When a solid power bus structure is given, we need to assign external and internal ports, and the internal ones should be assigned for connection with those at the hole and power island structures. As mentioned above, the impedance parameters of a solid power bus and hole structures can be calculated using (1). On the other hand, a power island should be modeled as a solid power bus, which is smaller than the hole and the capacitors representing the equivalent circuit model of the gap (Fig. 1) [5]. In the model, the ground plane below the gap is considered as short connections, and the assumption is valid when the gap on the power plane is small. When the capacitor (C) is connected to the ports in series, only the self impedance is increased by $1/\mathrm{j}\,\omega\mathrm{C}$. Therefore, we can calculate the impedance matrices of a power bus structure containing a power island using the expression (1) and the capacitance of the gap.

To derive the general impedance expression of a power bus structure containing a power island, the external (the p and u groups) and internal (the r, q, t, and s groups) ports were assigned as schematically shown in Fig. 2. Although—for reasons of simplicity—in Fig. 1, four internal ports were assigned to each power bus, for accurate calculation the number of internal

$$\begin{bmatrix} \bar{V}_p \\ \bar{V}_u \\ \bar{V}_s \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{11\_\text{overall}} & \tilde{Z}_{12\_\text{overall}} & \tilde{Z}_{13\_\text{overall}} \\ \tilde{Z}_{21\_\text{overall}} & \tilde{Z}_{22\_\text{overall}} & \tilde{Z}_{23\_\text{overall}} \\ \tilde{Z}_{31\_\text{overall}} & \tilde{Z}_{32\_\text{overall}} & \tilde{Z}_{33\_\text{overall}} \end{bmatrix} \begin{bmatrix} \bar{I}_p \\ \bar{I}_u \\ \bar{I}_t + \bar{I}_q \end{bmatrix}$$
$$= \begin{bmatrix} \tilde{I} & \tilde{0} & -\tilde{Z}_{12\_\text{solid}} \times ((\tilde{Z}_{rr})^{-1} - (\tilde{Z}_{22\_\text{island}})^{-1}) \\ \tilde{0} & \tilde{0} & \tilde{I} - \tilde{Z}_{22\_\text{solid}} \times ((\tilde{Z}_{rr})^{-1} - (\tilde{Z}_{22\_\text{island}})^{-1}) \\ \tilde{0} & \tilde{I} & -\tilde{Z}_{12\_\text{island}} \times (\tilde{Z}_{22\_\text{island}})^{-1} \end{bmatrix}^{-1}$$
$$\times \begin{bmatrix} \tilde{Z}_{11\_\text{solid}} & \tilde{Z}_{12\_\text{solid}} \times (\tilde{Z}_{22\_\text{island}})^{-1} \times \tilde{Z}_{21\_\text{island}} & \tilde{Z}_{12\_\text{solid}} \\ \tilde{Z}_{21\_\text{solid}} & \tilde{Z}_{22\_\text{solid}} \times (\tilde{Z}_{22\_\text{island}})^{-1} \times \tilde{Z}_{21\_\text{island}} & \tilde{Z}_{22\_\text{solid}} \\ \tilde{0} & \tilde{Z}_{11\_\text{island}} - \tilde{Z}_{12\_\text{island}} \times (\tilde{Z}_{22\_\text{island}})^{-1} \times \tilde{Z}_{21\_\text{island}} & \tilde{0} \end{bmatrix} \begin{bmatrix} \bar{I}_p \\ \bar{I}_u \\ \bar{I}_t + \bar{I}_q \end{bmatrix} \quad (6)$$

ports should be increased according to the increase in the maximum frequency of interest.

When the ports on the solid power bus structure are divided into external and internal, the impedance matrices are

$$\begin{bmatrix} \bar{V}_p \\ \bar{V}_s \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{11\_\text{solid}} & \tilde{Z}_{12\_\text{solid}} \\ \tilde{Z}_{21\_\text{solid}} & \tilde{Z}_{22\_\text{solid}} \end{bmatrix} \begin{bmatrix} \bar{I}_p \\ \bar{I}_r + \bar{I}_q \end{bmatrix} \quad (2)$$

where

$$\bar{V}_p = \begin{bmatrix} V_{p1} \\ \vdots \\ V_{pk} \end{bmatrix}, \quad \bar{I}_p = \begin{bmatrix} V_{p1} \\ \vdots \\ V_{pk} \end{bmatrix}$$
$$\tilde{Z}_{11\_\text{solid}} = \begin{bmatrix} Z_{p1p1} & \cdots & Z_{pkp1} \\ \vdots & \ddots & \vdots \\ Z_{p1pk} & \cdots & Z_{pkpk} \end{bmatrix}.$$

In addition, the impedance matrices for the power island structure can be expressed as

$$\begin{bmatrix} \bar{V}_u \\ \bar{V}_t \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{11\_\text{island}} & \tilde{Z}_{12\_\text{island}} \\ \tilde{Z}_{21\_\text{island}} & \tilde{Z}_{22\_\text{island}} \end{bmatrix} \begin{bmatrix} \bar{I}_u \\ \bar{I}_t \end{bmatrix}. \quad (3)$$

The impedance matrix for the hole structure is expressed as

$$\bar{V}_r = \tilde{Z}_{rr} \times \bar{I}_r. \quad (4)$$

Then, by substituting the voltage and current relations (5) into expressions (2)–(4), the impedance matrices of the power bus structure containing the power island are shown in

$$\bar{I}_s = \bar{I}_q + \bar{I}_r + \bar{I}_t \qquad \bar{V}_s = \bar{V}_q = \bar{V}_r = \bar{V}_t. \quad (5)$$

In (6), shown at the top of the page, $\tilde{I}$ and $\tilde{0}$ are the identity and zero matrices, respectively. Using (6), we can calculate the impedances ($\tilde{Z}_{11\_\text{overall}}$, $\tilde{Z}_{12\_\text{overall}}$, $\tilde{Z}_{21\_\text{overall}}$, and $\tilde{Z}_{22\_\text{overall}}$) at the external ports on the power bus structure containing the power island.

III. EXPERIMENTAL VERIFICATION

For the verification of the proposed matrix substitution method, a test package substrate was fabricated for impedance parameter measurements, and the measured results were compared with the calculated ones. Fig. 3 shows the cross section and layout of the test package substrate, which comprises three conductor layers with dimensions $a = 30$ mm and $b = 30$ mm. The dielectric material between the power and ground layers was FR4 and had a thickness and dielectric constant of 500 μm and 4.5, respectively. In Fig. 3(b), when the origin is set at the center of the test package substrates, port 1 is located at (0 mm, 0 mm), and ports 2 and 3 are located at (-11 mm, 11 mm) and (11 mm, 0 mm), respectively. In addition, an Agilent vector network analyzer 8753ES and Cascade GS type microprobes were used for measuring the impedance parameters from 10 MHz to 5 GHz.

For impedance calculation, we assigned three external and 40 internal ports ($k = 2, l = 1$, and j $= 40$ in Fig. 2). The number of internal ports was set to ensure the accuracy of the calculated results up to 5 GHz. The value of the capacitors representing the model of the gap was calculated by an analytical equation in [7], and the calculated capacitance of each capacitor in the test package was 30 fF. Fig. 4 shows the self—and transfer impedances of the test package substrate obtained by both measurement and calculation. The calculated impedances show good correlation with the measured impedances up to 5 GHz.

IV. CONCLUSION

In this letter, we proposed a matrix substitution method for calculating the impedance of a power bus structure containing a power island. This method enables calculation of the impedance of a power bus structure containing a power island by utilizing the resonant cavity model for a rectangular cavity. Finally, the method was verified by frequency domain measurements with a fabricated test package substrate.

REFERENCES

[1] K. Lee and A. Barber, "Modeling and analysis of multichip module power supply planes," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, no. 4, pp. 628–639, Nov. 1995.

[2] S. Van den Berghe, F. Olyslager, D. De Zutter, J. De Moerloose, and W. Temmerman, "Study of the ground bounce caused by power plane resonances," *IEEE Trans. Electromag. Comp.*, vol. 40, no. 2, pp. 111–119, May 1998.

[3] Y. Ji and T. H. Hubing, "EMAP5: A 3-D hybrid FEM/MOM code," *Appl. Computat. Electromagn. Soc. J.*, vol. 15, no. 1, pp. 1–12, Mar. 2000.

[4] T. Okoshi, *Planar Circuits for Microwaves and Lightwaves*. Munich, Germany: Springer-Verlag, 1985, ch. 2.

[5] Z. L. Wang, O. Wada, Y. Toyota, and R. Koga, "Modeling of gapped power bus structures for isolation using cavity modes and segmentation," *IEEETrans. Electromag. Comp.*, vol. 47, no. 2, pp. 210–218, May 2005.

[6] D. D. Wang, Z. F. Li, and Y. cao, "Fast analysis of bounces on power/ground planes using even-odd partition," *IEEE Trans. Antennas Propag.*, vol. 26, no. 1, pp. 65–72, Feb. 2003.

[7] T. C. Edwards and M. B. Steer, *Foundations of Interconnect and Microstrip Design (Third Edition)*. New York: Wiley, 2000, ch. 8.