# 3GHz Through-Hole Signal Via Model Considering Power/Ground Plane Resonance Coupling and Via Neck Effect

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**Abstract**

We describe an equivalent circuit model of a through-hole signal via in a multi-layer printed circuit board (PCB) for frequencies up to 3 GHz. In addition to the via itself, power/ground plane (parallel plate cavity) resonance and via neck effects are also reflected in the model. The model parameters are extracted by S-parameter measurement and a subsequent optimization fitting process. With the proposed model, the signal coupling to the power/ground plane resonance can be accurately estimated. Furthermore, it is demonstrated by near-field probe measurement that the radiated emission from the edge of power/ground planes has intimate correlation to the through-hole signal via.

## I. Introduction

As package, printed circuit boad (PCB), and on-chip interconnections require more devices on their substrates, routing complexity is ever increased. At the same time, a system size is reduced further and a switching frequency is continuously increased to the range of GHz. In accordance with these trends, a through-hole via becomes the most populated structure in high-speed and high-density multi-layer packages and PCBs. It is extensively used for signal interconnections when a signal traces changes layers, or when a plane is connected to another plane providing a low impedance current path. A through-hole via decreases the routing complexity and provides a low impedance power/ground network. However, it also causes signal distortion, such as reflection and loss, and makes inroad on the timing margin, such as a delay and a skew for a high-speed digital system.

Because a through-hole signal via penetrates a power/ground plane, a signal has a discontinuous return path and it can be affected by a power/ground parallel plate cavity. Because the dimension of a via is generally larger than that of a signal line, a transition structure called 'via neck' is required for connection between the two.

In order to estimate the performance of a multi-layer PCB, a reliable and accurate model of a via should be provided. However, in the previous models suggested from the previous researches, an electromagnetic wave coupling to a power/ground plane through vias is not took into consideration [1]-[3].

We measured various test patterns, which were different from one another, in terms of the number of vias and their positions on a power/ground plane. From the measured S-parameters, we found that a via induces considerable signal distortion and it becomes a source of power/ground plane resonance coupling. The resonance frequency of the power/ground plane is determined by its dimension as well as dielectric material. The power/ground plane resonance excited by a through-hole via proves to be a source of the radiated emission from the edge of a PCB. Furthermore, because the previous models assume that a ground plane exists below a via neck, they become inaccurate at higher frequencies.

In this paper, we describe an equivalent circuit model of a through-hole signal via in a multi-layer printed circuit board (PCB) for frequencies up to 3 GHz. In addition to the via itself, power/ground plane (parallel plate cavity) resonance and via neck effects are also took into consideration.

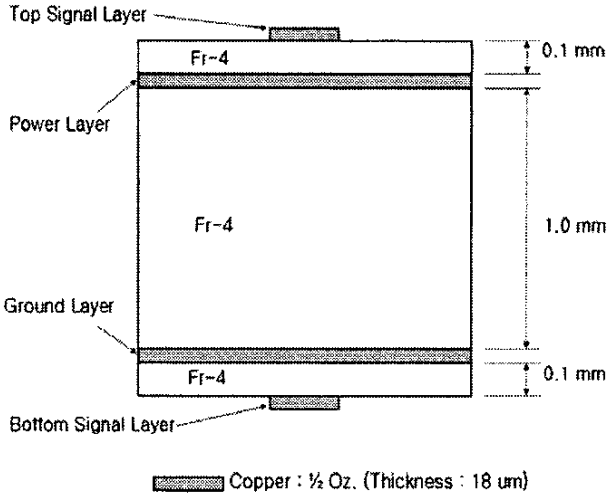


**Figure 1. 4-Layer PCB Stack-Up of DUT**

## II. Device-under-Test

We had to select multilayer PCB stack up and through-hole signal via structure. We chose spec. of personal computer mainboard. Because our interests is on large size board, currently personal computer is the best world wide thing, and main clock frequency is going up to GHz range including harmonic frequencies. Figure 1 shows the PCB stack up of DUT. The layers between power and ground were removed for the lack of relation with signal path. All substrates are FR-4, which has about 4.5 dielectric constant, and about 0.03 dielectric loss tangent. Figure 2 is the structure of through-

hole signal via. This strucure is also that of main board signal line. DUTs are classified to all 2 groups according to power/ground plane shape(Figure 3).

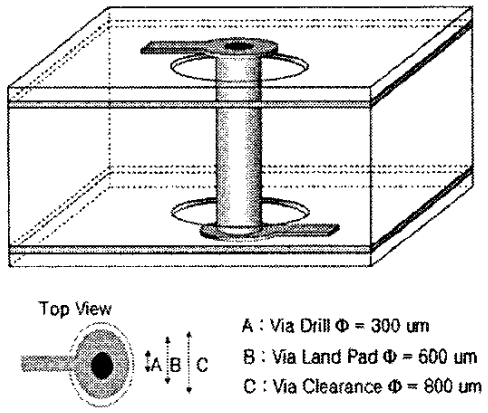


**Figure 2. Structure of Through-Hole Signal Via**

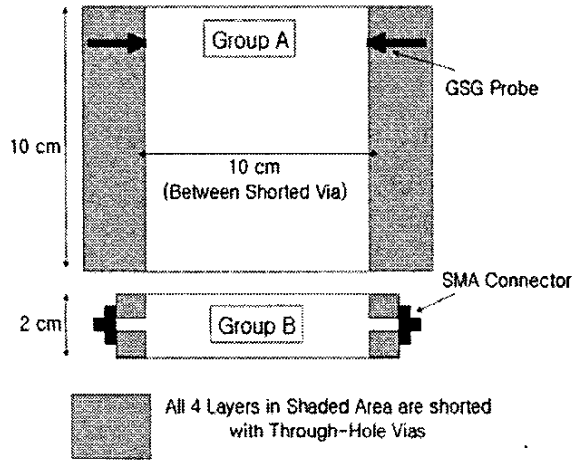


**Figure 3. DUT. Group A has 10cm X 10cm size of power/ground plane. Group B has 10cm X 2cm size. Each group has test patterns of A,B initial notation.**

The group A, which is for the modeling of through-hole signal via, has 10cm X 10cm plane size including total 3 microstrip lines. Each line has a even number through-hole signal via, e. g. 0(microstrip line:AML), 2(ML including 2 via:AMLV2), 4(AMLV4), 6(AMLV6), 8(AMLV8), and 10(AMLV10), respectively. The group B, which is for the analysis of coupling to power/ground plane resonance and PCB edge radiation, has 10cm X 2cm. In group B case, each DUT has single microstrip line with 0(BML), 1(BMLV1), and 2(BMLV2). All DUTs has 2 shorted, and 2 open sides of power/ground planes for the use of measurement point grounding. The reason of using narrow rectangular in group B is to decrease the number of power/ground plane resosnce. Namely, the group B case has the resonances related to 10cm length in 200MHz to 3GHz range. For example, 2cm length in FR-4(Er=4.5) substrate makes the lowest resonance at 3.5GHz. Therefore, Group A has maximum 13 resonances, and Group B has maximum 3.

## III. Measurement

Measurement was done at frequency domain and time domain. Figure 4 shows Transmission S-parameters of group A.

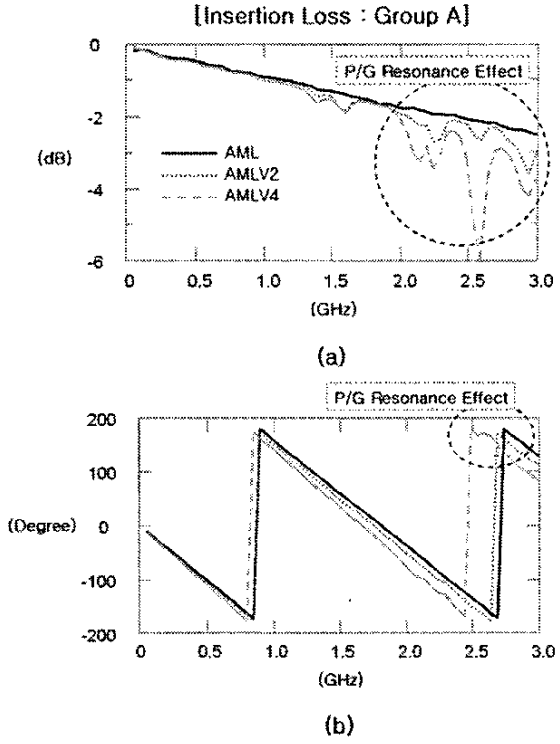


**Figure 4. Transmission S-parameter measurement of Group A. This two figures show the reflection and transmisstion loss problem of through-hole signal via (a) Insertion loss of AML, AMLV2, and AMLV4. AML response shows only dielectric and conduction loss. Insertion loss of AMLV2 and AMLV4 increase at power/ground resonance frequencies. (b) Transmission phase delay. ALM has a linearity. The linearity of AMLV2 and AMLV4 phase are broken by power/ground resonances. All AMLV(#) have similar responses.**

The magnitude of insertion loss shows that no loss of through-hole signal via accures with exception of power/ground resonance effect(abrupt increasing loss) and dielectric, conduction loss of each line. But the phase delay linearly increase along the number of through-hole signal via. This results prove that through-hole signal via effect on signal line is only phase delay(=time delay). This is more clearly shown in TDT measurement(Figure 5), which measured with 100ps rising time equipment. We could know the time delay at through-hole signal via is 13.8ps/via, which can be also obtained at phase delay with below equation.

$$\frac{\theta_d}{360f} = timedelay/10vias$$

$\theta_d$ is the phase delay difference between ALM and ALMV10 at the selected single frequency, which is notated by $f$ .

For example, if 1.5 GHz frequency is selected, the phase delay difference is 7.2°/via and then the time delay is 13.3ps/via, which is good agreement with time measurement. This value is larger than that of microstrip line, 8.5ps, under same length of 1.2mm via.

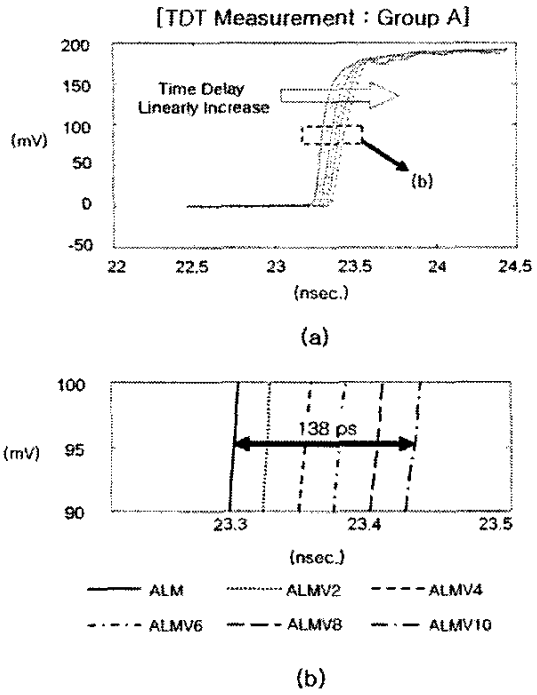


**Figure 5. Transmission time delay measurement of Group A. This two figures show the time delay problem of through-hole signal via. Since measurement setup has 100ps rising time, the discontinuity does not view in this measurement. But the voltages at 50 Ω load fluctuate in AMLV(#) cases. (a) TDT responses of AMLV(3) cases. Time delay increase linearly with increasing number of through-hole signal via. (b) Transmission time delay. ALMV10 has a 138ps larger time delay than ALM.**

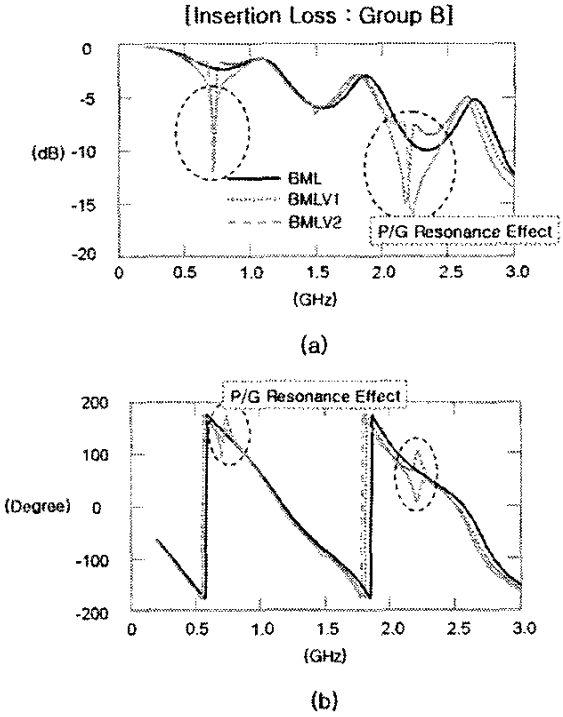


**Figure 6. Transmission S-parameter measurement of Group B. You can see the difference of power/ground plane resonance effecs through comparison with Figure 4. (a) Insertion loss of BML, BMLV1, and BMLV2. BML response shows not only dielectric and conduction loss but also impedance mismatching by SMA connector pads. Insertion loss of BMLV1 and BMLV2 increase at power/ground resonance frequencies. And mismatching at source and load increase power/ground plane effects on signal integrity (b) Transmission phase delay. BLM has a linearity. The linearity of BMLV1 and BMLV2 phase are broken by power/ground resonances.**

Group B measurement is shown in Figure 6. As expected, the power/ground plane resonances are appeard at maximum 3 points. Because group B has a smaller power/ground plane. And transmission results look like more lossy than group A. These come from SMA connector pad at measuring points. Microstrip lines are fabricated at 50Ω, and SMA connector pad has 13Ω. Therefore SMA connector pad make a large discontinuity, and a large reflection. Here we could know another fact that the through-hole signal via effects on signal integrity are larger without source, load matching.

As the results of two groups, the response of through-hole signal via is strongly dependent to power/ground plane shape, positions, and source/load matching.

## IV. Modeling of through-hole signal via

Figure 7 is the modeling procedure. The through-hole signal via model is accomplished with frequency domain measurements, and confirmed with time domain measurement. For the modeling, the results of Group A were used because of no distortion of SMA connector. For de-embedding of microstrip line from AMLV(#), AML modeling was begun. Figure 8 shows measurement and model simulation of AML.

Modeling methods is optimization technique with microstrip line library and lumped circuit model. Since AML is 92mm length, dielectric loss is not sufficiently expressed with lumped circuit model. After this, all microstrip line model is used in library. AML model parameters, and FR-4 substrate parameters were extracted as 147um line width, 18um metal thickness(1/2 OZ. copper) and 4.51 dielectric constant, 0.036 dielectric loss tangent, respectively (mocrostrip line impedance = 54Ω).

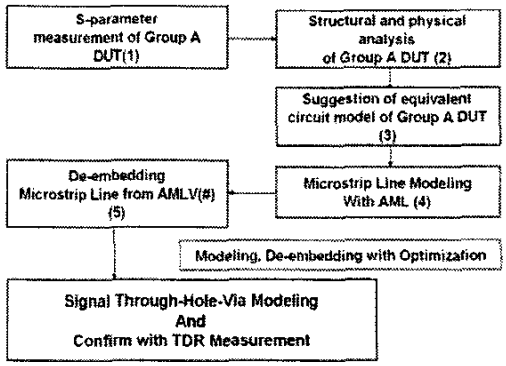


**Figure 7. Modeling procedure**

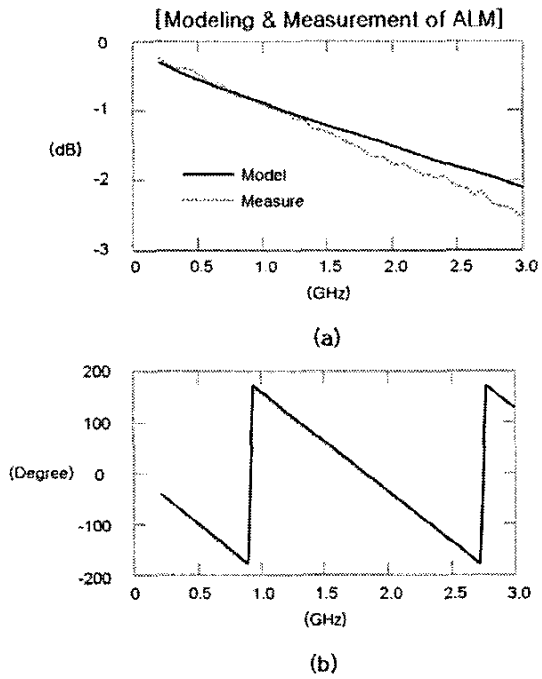


**Figure 8. Modeling and measurement of ALM. (a) Insertion loss is determined by dielectric loss tangent of substrate and characteristic impedance of microstrip line (b) Transmission phase delay is determined by dielectric constance of substrate and length of microstrip line.**

We suggested a double ∏-type model of the through-hole signal via shown in Figure 9. The description of model parameters are in Figure 10. Since we focused on the effect of discontinuos RF reference, this model type is suited. In other words, upper side of through-hole signal via is strongly combined with power layer, and lower side is ground layer, respectively. So two capacitors($C_{viabody-GND}$) have the same node at center. And via neck model is easily attatched with T-type at this model. The via neck is the connection point of microstrip line and through-hole signal via. From optimization technique, we could get model parameter values, which are shown in Figure 11.

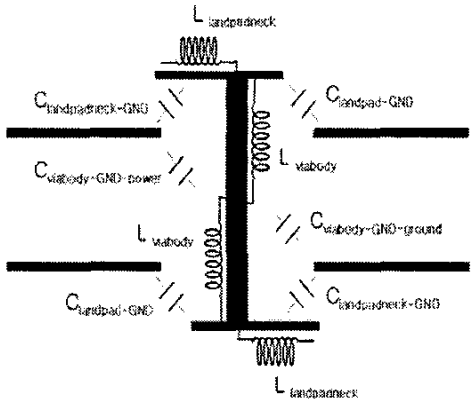


**Figure 9. Suggestion of through-hole signal via model including via neck effect. The via neck part is needed as considering power/ground plane resonance.**

As a results, the through-hole signal via has a capacitve characteristic impedance. This is the same trand of traditional via model. The via neck is inductive. The via neck has the inside of power/ground plane as farther distance RF reference than that of microstrip line. Therefore, the capacitance of via neck, inductance are smaller, larger, respectively. The whole impedance under influence of adding through-hole signal via is more inductive than that of microstrip line, and the larger time delay occurrs than that of microstrip line as mentioning in the front part of chapter III.

| Model Part | Model Parameters | Description |
|---|---|---|
| Through-Hole Signal Via | $L_{viabody}$ | Inductance of Half Via Body |
| | $C_{viabody-GND-power}$ | Capacitance of Via to Power Layer |
| | $C_{viabody-GND-ground}$ | Capacitance of Via to Ground Layer |
| | $C_{landpad-GND}$ | Capacitance of Via Land Pad to Power/Ground Layers |
| Via Neck | $L_{landpadneck}$ | Inductance of Via Neck and Via Land Pad |
| | $C_{Landpadneck-GND}$ | Capacitance of Via Neck To Power/Ground Layers |

**Figure 10. Description of suggestied model parameters.**

| Model Parameters | Extraction Values |
|---|---|
| $L_{viabody}$ | 254 (pH/halfvia) |
| $C_{viabody-GND-power}$ | 104 (fF/via-power) |
| $C_{viabody-GND-ground}$ | 104 (fF/via-ground) |
| $C_{landpad-GND}$ | 54 (fF/landpad) |
| $L_{landpadneck}$ | 802 (pH/2mm) |
| $C_{Landpadneck-GND}$ | 132 (fF/2mm) |

**Figure 11. Extracted model parameters of through-hole signal via. The via neck's inductance are 100pH larger, and capacitance are 70fF smaller than that of microstrip line, respectively. These come from via clearance.**

## V. Through-hole signal via coupling to power/ground plane resonance including via neck effect

Until now, we obtained a simple model. But this model does not wholly satisfy the measurement, especially about frequency domain case. Therefore, the model must include power/ground plane resonance effect. And we could get the whole through-hole signal model including power/ground plane resonance.

Firstly, we will show the relation of measurement and power/ground plane resonance with TLM simulation[4]. Figure 12 and Figure 13 are Group A, B cases, respectively. The plane resonce frequencies are expressed as that of high input impedance. TLM simulation is well known as a reliable and simple simulation for power/ground plane. Since our interest is up to 3GHz, each TLM cell has an1mm×1mm cell size, which is sufficient to get correct impedance profile.

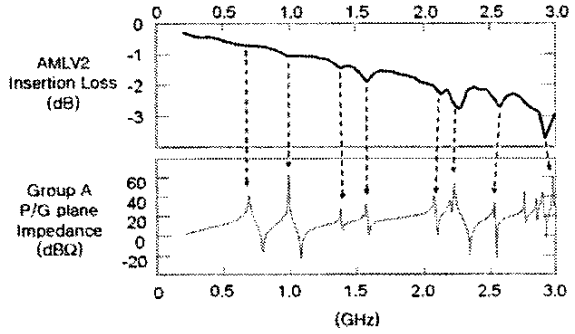


**Figure 12. Relation of insertion loss and 10cm X 10cm size power/ground plane resonce. This size plane has 13 resonace frequencies within 3GHz. Each resonce make insertion loss increase.**

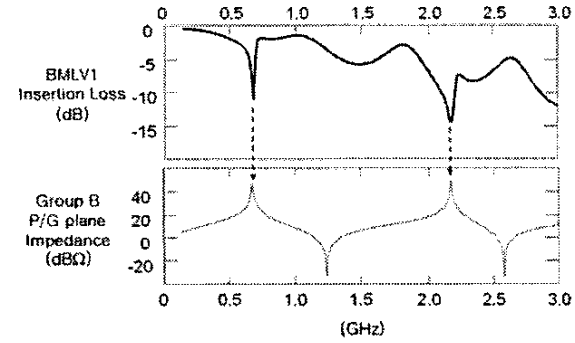


**Figure 13. Relation of insertion loss and 10cm X 2cm size power/ground plane resonce. This size plane has 3 resonace frequencies within 3GHz. But through-hole signal via located at center does not catch 2nd resonance. Each resonce make insertion loss increase.**

Next, we combined through-hole signal via model and power/ground TLM simulation results by replacing perfect ground reference with the impedance profile box at all each – GND named capacitors in Figure 9. The resonance peaks are well predicted by the via coupling capacitance in the obtained model and the TLM simulation. Even though the through-hole signal via's capacitance is the main trigger of the signal loss, the total loss and Q value are not explained without the microstrip line's capacitance. Therefore the via neck's capacitance also is connected to impedance profile box. The longer via neck part is the better agreement with measurement.

Finaly, we could get the whole through-hole signal model including power/ground plane resonance and via neck effect. Figure 14 shows that the obtained model well predicts power/ground plane effects and via neck effect.

We also simulated votalge fluctuation at capacitors for explanation of signal loss (Figure 15). In case of no power/ground plane model, the capacitor volatage is stable as Figure 16. But on including power/ground plane, the capacitor voltage decreases at resonance frequencies. Namely, the total impedance to perfect ground at via decreases by combining via coupling capacitor and inductive impedace of power/ground plane at resonance frequencies. This is expressed as signal loss in S-parameter measurement.

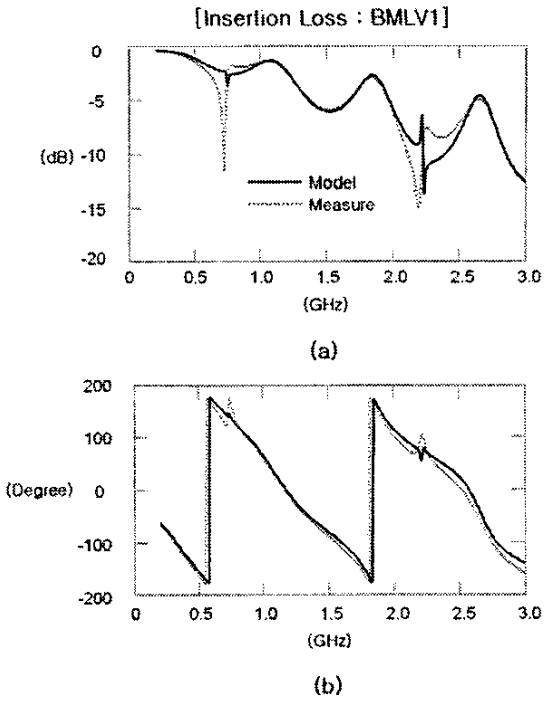


**Figure 14. Comparison measurement and modeling with the whole through-hole signal via model including power/ground plane resonance and via neck effect. (a),(b) well predict power/ground plane effects.**

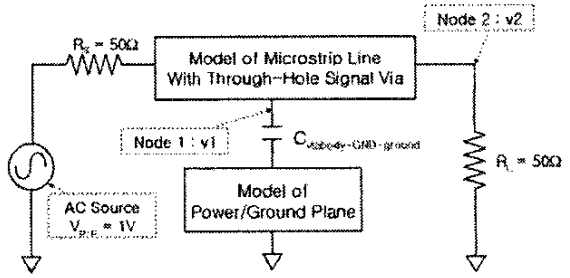


**Figure 15. Voltage fluctuation simulation at through-hole signal via(node 1) and load(node 2).**

In digital system, the signal wave form has wide band frequency. But the most signal energy are concentrated around the main clock frequency and its harmonic frequencies to the 3rd harmonic. If the power/ground plane resonace frequency is same as the main clock frequeccy or its harmonics, the signal wave form is disroted seriously. For example, the 700MHz digital clock meets the through-hole signal via on FR-4 10cm X 10cm size power/ground plane, then the digital clock may lose a great part of signal energy. So the design of multilayer PCB using through-hole signal via must be done by considering power/ground plane size offseting the main clock frequency and its harmonics.

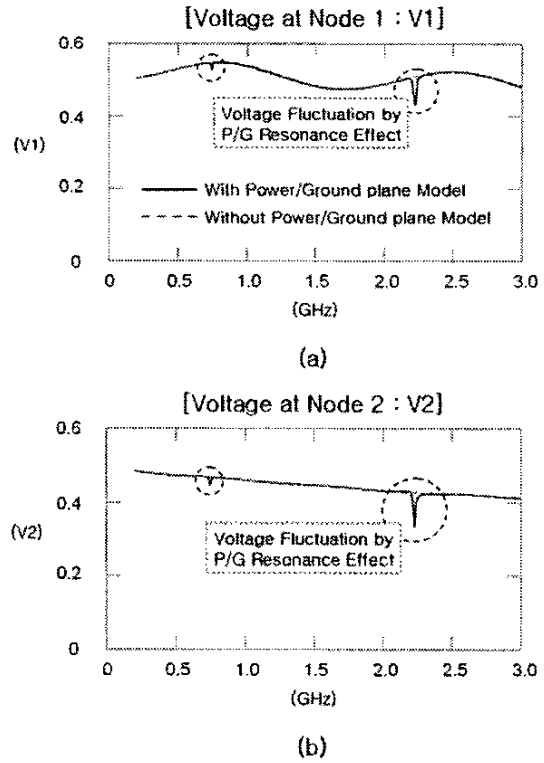


**Figure 16. Voltage fluctuation at through-hole signal via(node 1) and load(node 2). (a) through-hole signal via drops voltage at power/ground plane resonance. (b) voltage at load also drops. These show that through-hole signal via is a important position causing signal loss.**

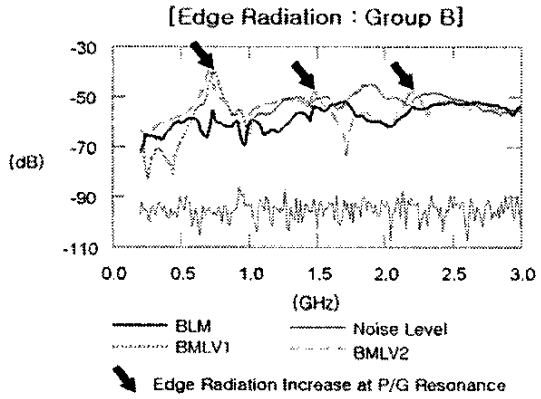


**Figure 17. The coupled signal to power/ground plane from the through-hole signal via is the source of PCB edge radiation. The radiation increase at power/ground plane resonance, at which coupling is strong. This measurement is done with near-field probe antenna.**

## VI. Through-hole signal via exciting power/ground plane edge radiation

The through-hole signal via coupling to power/ground plane resonance cuases another problem, which is EMI. Even though this is a different view of ECTC, we will mention for the total board design. As discussed in chapter V, the lost signal energy flows into somewhere on PCB, one of which is the reflection to signal source , and the other is the remaining inside power/ground plane. The former is explained with increased S11 value at resonance frequency of Figure 4, 6. The latter is explained with PCB edge radiation. We shows the edge radiation result in Figure 17. The edge radiation incrase maximum 30dB at resosnce frequency in comparison with no through-hole signal via case.

## VII. Conclusions

In this paper, the 3GHz model of through-hole signal via in multilayer PCB considering power/ground plane resonance and via neck effect.

We showed the through-hole signal via's effects with frequency donain and time domainis measurement, and explained the effects with modeling the through-hole signal via and the coupling to power/ground plane. And we confirmed that the through-hole signal via is the critical EMI source.

Therefore, an appropriate sizing of power/ground plane and a positioning of through-hole signal via can reduce the signal distortion and PCB edge radiation under consideration of system clock frequency.


## Acknowledgment

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