On-Chip PDN (Power Distribution Network) Comparison between Single Chip and Stacked Multi-Chips with TSV (Through Silicon Via)

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1. INTRODUCTION

Nowadays, System in Package (SiP) is the highest technology to make mobile electronic devices be small enough to realize in a single device for hand held application. Therefore, the demands for SiP are increasing and predicted from 1,573 million units in 2007 to 2,495 million units in 2011 [1]. The conventional SiP is being manufactured with a few chips on a single package substrate and with 2-dimensional approach using long wire-bonding type interconnection. As a result, though data processing speed of a chip becomes higher, the overall system speed is limited and not enough to meet currently demanded speed due to large inductance of the long wire-bonding. Consequently, 3-dimensional (3-D) stacked chip package is highly needed to get short signal and low impedance of power distribution network (PDN) for enhancing qualities of signal integrity (SI) and power integrity (PI) by shortening interconnection length or lowering inductance between chips. [2]-[3]

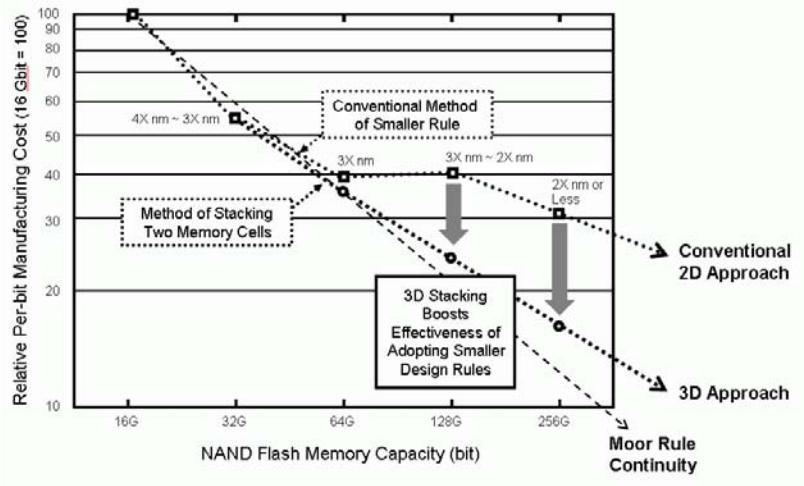

Figure 1. 3D Stacked Chip for Cost down thru Chip Density Increment

Additionally, many semiconductor manufacturers want to increase their benefits by decreasing cost per bit by means of shrinking manufacturing technologies as shown in Fig. 1. However, theses shrinking technology method does not give merits after using under 30 nm technology. Therefore, they want to use 3-D technology for their benefits to meet Moor Rule and to keep increasing.

Stacked chips with wire-bonding don't guarantee good SI and PI due to its large equivalent series inductance (ESL). [4] Consequently, the technologies for reducing inter-chip interconnection length are developing. The state-of-the-art technology of them is through-silicon-via (TSV), which routes the

electrical path through all stacked chips, rather than wire-bonding. (Fig. 2) TSV is a promising interconnection method to connect vertically (3-D) stacked chips with the shortest interconnection, which means the lowest ESL interconnection is given. In this paper, we show the comparison between single chip PDN (Power Distribution Network) and stacked multi-chip PDN depending on TSV conditions.

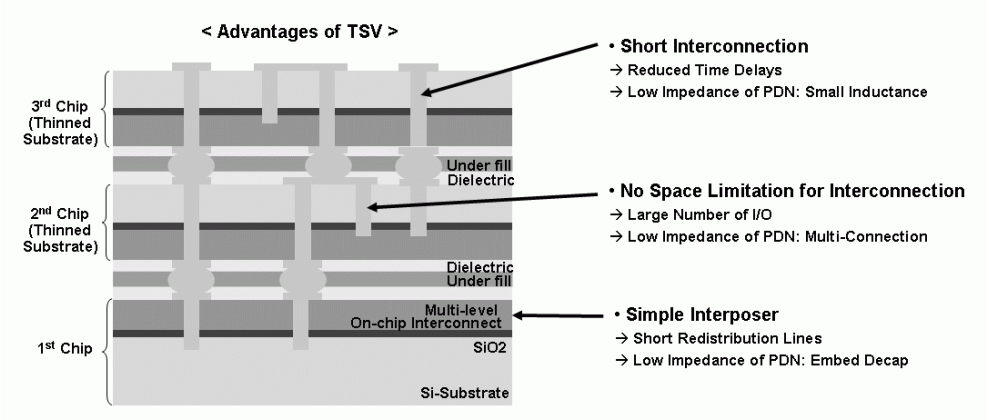

Figure 2. Best Solution for 3-D Stacked Chip Package

2. Electrical Characteristics of TSV depending on its Structure

To obtain on-chip PDN impedance, we simulated TSV with various dimensions and on-chip PDN with HFSS and ADS Momentum simulators, respectively. In TSV case, we have assumed that TSV with 30 um diameter is formed in silicon substrate with 10 Ω·cm resistivity and 1 um thickness SiO2 (Silicon Dioxide) around TSV. Usually, TSV has thin SiO2 around itself to protect DC leakage to silicon substrate. Two TSVs were simulated for Power and Ground paths. In on-chip PDN case, we have used segmentation method. Using defined unit cell of on-chip PDN, we could obtain on-chip PDN impedances of various size on-chip PDN. In this paper, two cases of 2 mm x 2 mm and 1 mm x 1 mm on-chip PDNs are used to see the effects of TSV on on-chip PDN impedance in stacked chips.

PDN is used for power supply to operate chip's circuit. Therefore, its impedance must be close to zero ohm. However, since PDN is formed with finite size metal, it has inductance and capacitance. An inductance increases PDN impedance and a capacitance decreases PDN impedance. Consequently, to know the TSV effects on on-chip PDN impedance, we should understand inductance and capacitance of TSV previously. When TSV is terminated with ideally electrical short condition, we can obtain TSV's resistance and inductance. When TSV is terminated with ideally electrical open condition, TSV's capacitance and conductance are obtained. (Fig. 5) But, since TSV has 200 ~ 100 um length, its resistance is very small around tens of mΩ and its analysis is skipped in this paper.

Figs 3 and 4 show TSV inductances and capacitances depending on TSV's length (L) and pitch (P). Pitch means the distance between two centers of two Power and Ground TSVs. When L and P are reduced, the loop size of two Power/Ground TSVs is also reduced and its inductances are decreased. (Inductances: solid line > dashed line > dash-dot line, Fig. 3).

In case of TSV capacitance (Figs 4 and 5), the reduced L means the reduced TSV surface area and reduced TSV capacitance, but the reduced P does not effect on capacitance. It is because that Gsi is the main AC current path and Csio2 is almost 100 times larger than Csi. (Fig 5)

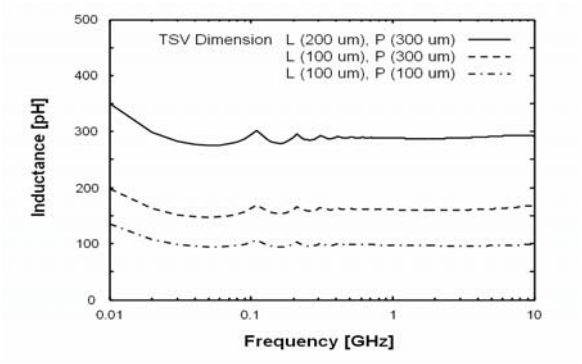

Figure 3. TSV Inductances

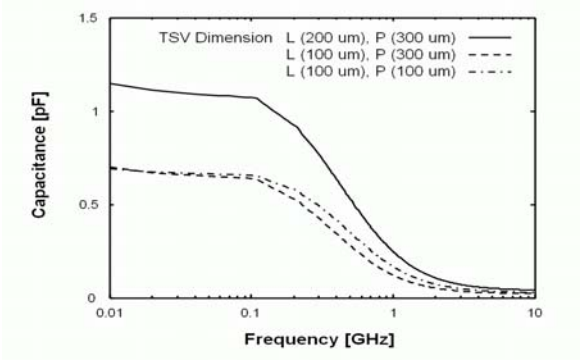

Figure 4. TSV Capacitances

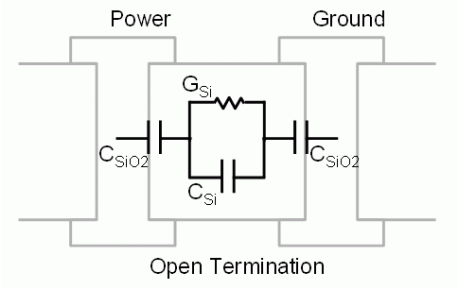

Figure 5. TSV with Open Termination and its Equivalent Circuit Model

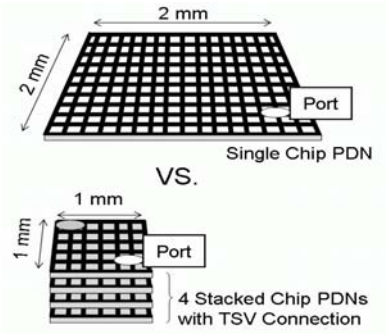

Figure 6. Single Chip PDN vs. Stacked Chip PDNs

3. Comparison between Single Chip PDN and Stacked Chip PDNs

Four PDN impedances of four PDN conditions are compared. One is 2 mm x 2 mm on-chip PDN, the second has 1 mm x 1 mm size, the third is stacked four 1 mm x 1 mm connected by single Power/Ground TSV pair from top to bottom, and the fourth has the same structure as the third and four Power/Ground TSV pairs, as shown in Figs. 6 and 7.

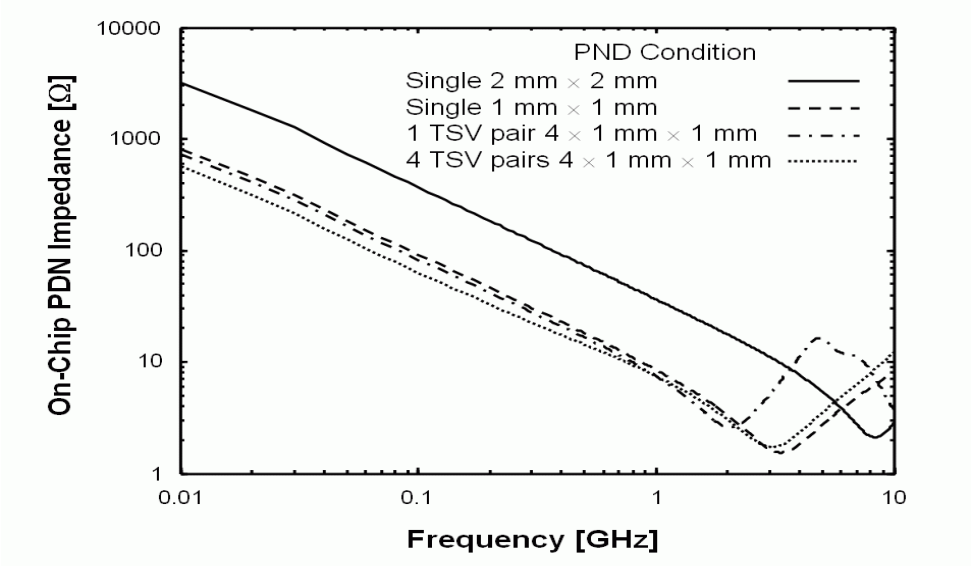

Figure 7. Single Chip PDN vs. Stacked Chip PDNs

Of course single 2 mm x 2 mm on-chip PND (solid line) shows larger capacitance (lower impedance) than single 1 mm x 1 mm on-chip PDN (dashed line), but shows larger inductance (larger impedance) in high frequency range due to its larger size. When four 1 mm x 1 mm on-chip PDNs (dash-dot line) are stacked and connected by single Power/Ground TSV pair, the stacked on-chip PDNs show the same capacitance as 2 mm x 2 mm on-chip PDN due to the same total on-chip PDN area, but larger inductance are shown due to TSV inductance. In addition, at 5 GHz, dual impedance peaks appear because TSV inductance electrically blocks the capacitances of two bottom side 1 mm x 1 mm on-chip PDNs. Finally, the number of Power/Ground TSV pairs between 1 mm x 1 mm on-chip PDNs is changed from 1 to 4, then the inductance is very close to single 2 mm x 2 mm on-chip PDN due to parallel connected TSV inductances. The larger capacitance (lower impedance) can be obtained by TSV capacitance.

4. CONCLUSION

In this paper, the inductance and capacitance of TSV depending on it dimensions and the TSV effects on on-chip PDN impedances have been studied. When TSVs are used for stacked on-chip PDN interconnections, its inductance can block electrical connections to far located on-chip PDN. Therefore, TSV length should be smaller than 100 um and the number of Power/Ground TSV pairs should be over 4 per 1 mm x 1 mm on-chip PDN size to reduce inductances of on-chip PDN interconnections in stacked chips. Especially, TSV has larger design freedom such as position and number on chip than wire bonding, and Lower inductance and lower on-chip PDN impedance can be achieved easily.

Acknowledgement

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