Variable-Precision Distributed Arithmetic (VPDA) MIMO Equalizer for Power-and-Area-Efficient 112 Gb/s Optical DP-QPSK Systems

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***Abstract*—A variable-precision distributed arithmetic (VPDA) multi-input multi-output (MIMO) equalizer is presented to reduce the size and dynamic power of 112 Gb/s dual-polarization quadrature phase-shift-keying (DP-QPSK) coherent optical communication receivers for 80 km metro applications. The VPDA MIMO equalizer compensates for channel dispersion as well as various non-idealities of a time-interleaved successive approximation register (SAR) based analog-to-digital converter (ADC) simultaneously by using a least mean square (LMS) algorithm. As a result, area-hungry analog domain calibration circuits are not required. In addition, the VPDA MIMO equalizer achieves 45% dynamic power reduction over fixed resolution counterparts by utilizing the minimum required resolution for the equalization of each dispersed symbol.**

***Index Terms*—Analog-digital conversion, digital signal processors, equalizer, optical receivers, power dissipation.**

I. Introduction

COHERENT optical DP-QPSK systems with electrical domain dispersion compensation at a wavelength of 1550 nm are being adapted for 112 Gb/s long-haul optical communication links in order to combat chromatic dispersion (CD) [1], [2]. Fig. 1 shows a typical block diagram of a 112 Gb/s DP-QPSK coherent optical receiver [2], [3]. The phase information of the received optical signal is converted to two pairs of analog voltage signals and $2\times$ oversampled using four 56 GS/s ADCs. A digital equalizer subsequent to the ADCs compensates for the channel dispersion. Such a high data rate requires a massive parallelization in the ADC and digital equalizer due to the bandwidth limitation of active components.

The tight performance requirements of the ADC necessitates complex and area-hungry calibration circuits to overcome various non-idealities caused by mismatch among parallel ADCs and nonlinearities in each ADC [4], [5]. The power consumption of the digital equalizer increases in proportion to its dispersion compensation capability and the level of computational precision. The power and area of the conventional coherent DP-QPSK system have been the major impediments to its adaptation to high-volume applications such as Metro DWDM despite its excellent dispersion compensation capability. In this paper, we propose a power-and-area-efficient VPDA MIMO equalizer for coherent optical DP-QPSK systems suitable for Metro DWDM applications which require performance, low power and miniaturization. The target distance is 80 km. Significant reduction in power and area is achieved on the basis of the following two factors: (i) digital equalizer in this proposed design compensates for the channel dispersion as well as the non-idealities of the ADC without hardware overhead, which does not necessitate area-hungry analog domain calibration cirucits, and (ii) each dispersed symbol is equalized with the minimum required resolution. The latter factor leads to dynamic power reduction of 45% in the digital equalizer.

Section II depicts the proposed receiver architecture and Section III describes the distributed arithmetic (DA) MIMO channel equalizer architecture which also compensates for various mismatches and non-linearities of the SAR ADC. Then, Section IV describes the variable-precision concept applied to the DA MIMO architecture for the dynamic power reduction. Section V provides the simulation results of the VPDA MIMO equalizer and finally, Section VI summarizes the discussion.

II. Receiver Architecture

Fig. 2 shows the block diagram of the proposed coherent DP-QPSK receiver for 80 km metro DWDM applications. The outputs of four 56 GS/s 5 bit ADCs are connected to both the VPDA MIMO equalizer and a clock recovery block. Conventional dispersion-tolerant phase detectors [6] typically operate under residual CD in long-haul coherent systems can be utilized in this case without pre-equalization because the target distance is only 80 km [6], [7]. In addition, because the phase detector detects the symbol rate directly from 2x oversampled ADC outputs without any assistant from the equalizer, typical start-up issue does not exist. The VPDA MIMO equalizer is intentionally designed to operate in time domain because the frequency domain counterparts [8] has higher level of complexity in 80 km metro applications where the chromatic dispersion is less than 1280 ps/nm.

III. Compensation of ADC Non-Ideality

Digital signal processing methods to overcome either the mismatch or nonlinearity have been reported [9], [10]. The proposed DA MIMO architecture integrates these two methods together with the channel equalizer without hardware overhead over conventional FIR channel equalizers employed in 112 Gb/s coherent optical DP-QPSK systems.

Manuscript received April 09, 2012; revised July 30, 2012, October 18, 2012; accepted November 16, 2012. Date of publication November 26, 2012; date of current version December 28, 2012. This work was supported by the Smart IT Convergence System Research Center funded by the Ministry of Education, Science and Technology as Global Frontier Project (SIRC 2011-0031861).

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Digital Object Identifier 10.1109/JLT.2012.2230244

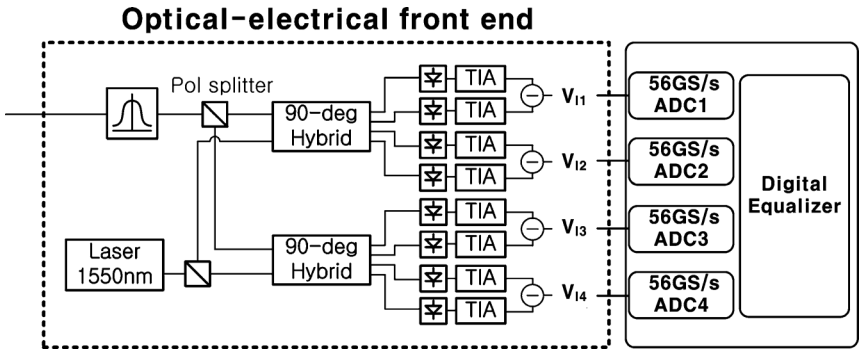

Fig. 1. Block diagram of the 112 Gb/s DP-QPSK receiver.

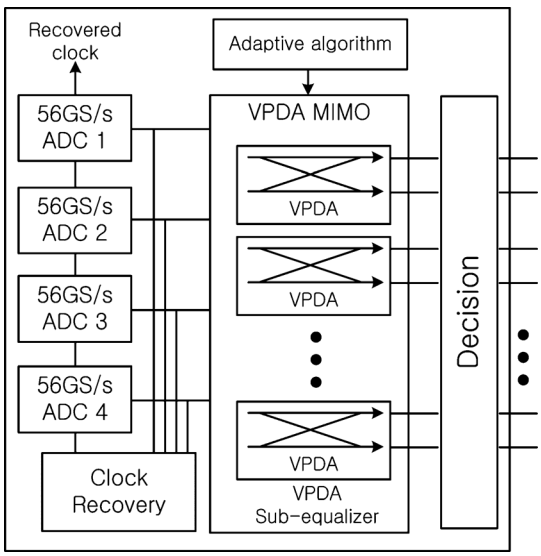

Fig. 2. Block diagram of proposed coherent DP-QPSK receiver for 80 km metro DWDM applications.

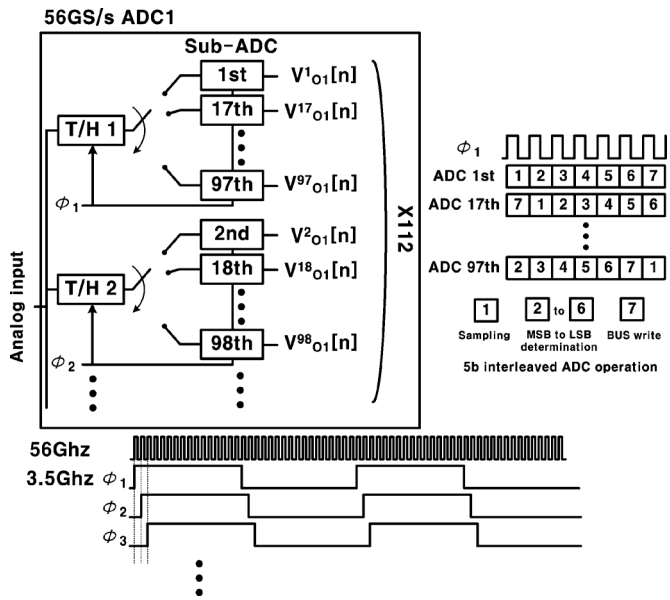

Fig. 3. Block diagram of the 112 time-interleaved ADC.

A. Mismatch Compensation

It has been shown that the MIMO equalization method can compensate for the offset, gain and sampling time mismatches of a time-interleaved parallel ADC [9]. Fig. 3 shows a conceptual block diagram of a 56 GS/s time-interleaved SAR-based ADC [11]. The resolution of the ADC is set to five bits to suppress the OSNR penalty below 0.5 dB at a BER of 10^{-3} [12], [13]. In our ADC model, 16 track-and-hold (T/H) circuits operating at 3.25 GS/s are parallelized for the sampling rate of 56 GS/s. We assumed that the sub-ADCs subsequent to the T/H requires seven clock cycles for each data conversion based on [11]. Thus, a total of $16 \times 7 = 112$ SAR ADCs are parallelized. As a result, the digitized samples show 112 different cyclic characteristics, which can be modeled by a radix-112 system. Let $V_I^i[n]$ denote the i-th input signal in the radix-112 system, then the n-th input matrix $V_I[n]$ of the radix-112 ADC system is given by

$$V_I[n] = \left[V_I^1[n]\, V_I^2[n] \cdots V_I^{112}[n]\right]^T. \tag{1}$$

Similarly, the n-th output matrix of the ADC is

$$V_O[n] = \left[V_O^1[n]\, V_O^2[n] \cdots V_O^{112}[n]\right]^T. \tag{2}$$

Various mismatch effects of the ADC can be interpreted using linear MIMO matrices. Let the matrix G, P and O represent the gain, phase and offset mismatches of the time-interleaved ADC, respectively. V_I and V_O satisfy

$$[G]_{112\times112} \cdot [P]_{112\times112} \otimes_c [V_I]_{112\times1} + [O]_{112\times1} = [V_O]_{112\times1}. \tag{3}$$

The mathematic operator $\otimes_c$ denotes the element-by-element convolution [14]. The quantization noise is not considered for simplicity. The gain mismatch G is a diagonal matrix, which is given by

$$G_{ij} = \begin{cases} g_i & i = j \\ 0 & i \neq j \end{cases}, \quad i, j = 1 \ldots 112, \tag{4}$$

where g_i represents the gain of the i-th ADC. The sampling phase mismatch P can be described using linear interpolation between adjacent samples in V_I, as

$$P_{112\times112} = \Phi^{-1}_{112\times112} + \Phi^{0}_{112\times112} + \Phi^{1}_{112\times112}$$
$$\Phi^{k}_{i,j}[n] = \phi_{i,j,k}\delta[112n + i - j - k], \quad i, j = 1 \ldots 112, \tag{5}$$

where $\phi_{i,j,k}$ is the phase coefficient for the i-th ADC input and $\delta[n]$ denotes the discrete time delta function. Because the input signal V_I is $2\times$ oversampled, the P matrix models the phase mismatch with sufficient accuracy.

The offset vector O is a 112×1 matrix, as given by

$$O = [O^1\, O^2\, \cdots\, O^{112}]^T, \tag{6}$$

where O^i represents the offset of the i-th ADC.

A coherent DP-QPSK receiver requires four 56 GS/s ADCs, as shown in Fig. 1; thus, the total number of sub ADCs is $112 \times 4 = 448$. Let

$$S_I = \begin{bmatrix} V_{I1} \\ V_{I3} \end{bmatrix}, \quad S_Q = \begin{bmatrix} V_{I2} \\ V_{I4} \end{bmatrix}, \tag{7}$$

where S_I and S_Q denote the in-phase and quadrature-phase signals in a QPSK system, respectively. Equation (3) can be expanded to include all four ADC inputs S_I and S_Q as

$$M_I \otimes_c S_I + j \cdot M_Q \otimes_c S_Q + C = R_I + j \cdot R_Q \tag{8}$$

where

$$\begin{aligned} M_I &= \begin{bmatrix} G_1 \cdot P_1 & 0 \\ 0 & G_3 \cdot P_3 \end{bmatrix}_{224\times224}, \\ M_Q &= \begin{bmatrix} G_2 \cdot P_2 & 0 \\ 0 & G_4 \cdot P_4 \end{bmatrix}_{224\times224}, \\ C &= \begin{bmatrix} O_1 \\ O_3 \end{bmatrix}_{224\times1} + j \cdot \begin{bmatrix} O_2 \\ O_4 \end{bmatrix}_{224\times1} \\ &= C_I + j \cdot C_Q, \end{aligned} \tag{9}$$

$$R_I + j \cdot R_Q = \begin{bmatrix} V_{O1} \\ V_{O3} \end{bmatrix} + j \cdot \begin{bmatrix} V_{O2} \\ V_{O4} \end{bmatrix}. \tag{10}$$

Ideal ADC outputs S_I and S_Q can be retrieved as

$$S_I + jS_Q = M_I^{-1} \otimes_c R_I + j \cdot M_Q^{-1} \otimes_c R_Q + C', \tag{11}$$

where

$$C' = -M_I^{-1} \otimes_c C_I - j \cdot M_Q^{-1} \otimes_c C_Q. \tag{12}$$

Let the $2\times$ oversampled transmitted QPSK signal vectors through X and Y polarizations are $X_{I,Q}$ and $Y_{I,Q}$, respectively. $X_{I,Q}$ and $Y_{I,Q}$ can be written in 112×1 matrix as given by

$$\begin{aligned} X_{I,Q} &= [X_{I,Q}^1[n]\, X_{I,Q}^1[n]\, X_{I,Q}^2[n]\, X_{I,Q}^2[n]\, \cdots\, X_{I,Q}^{56}[n]]^T \\ Y_{I,Q} &= [Y_{I,Q}^1[n]\, Y_{I,Q}^1[n]\, Y_{I,Q}^2[n]\, Y_{I,Q}^2[n]\, \cdots\, Y_{I,Q}^{56}[n]]^T, \end{aligned} \tag{13}$$

where $X_{I,Q}^i[n] = x_{I,Q}[56n + i]$ and $Y_{I,Q}^i[n] = y_{I,Q}[56n + i]$. Note that $x_{I,Q}$ and $y_{I,Q}$ denote transmitted symbols. CD in the radix-112 matrix format is

$$\mathrm{CD}_{ij}[n] = cd[112n + i - j], \quad i, j = 1 \ldots 112, \tag{14}$$

where $cd[n]$ denotes the $2\times$ oversampled complex impulse response of CD.

The first-order polarization mode dispersion (PMD) can also be written as a radix-112 matrix, as

$$\begin{aligned} \mathrm{PMD} &= \begin{bmatrix} \cos\alpha \times I^{\theta_x} & -\sin\alpha \times I^{\theta_y} \\ \sin\alpha \times I^{\theta_x} & \cos\alpha \times I^{\theta_y} \end{bmatrix} \\ I_{ij}^{\theta_{x,y}} &= \delta[112n + i - j - \theta_{x,y}], \quad i, j = 1 \ldots 112. \end{aligned} \tag{15}$$

PMD adds a phase delay of θ to each polarization and attenuates the transmitted signal by rotating the polarization angle by α. The combined channel dispersion matrix H including CD and PMD is

$$\begin{aligned} H_{224\times224} = &\begin{bmatrix} [CD]_{112\times112} & 0 \\ 0 & [CD]_{112\times112} \end{bmatrix} \\ &\otimes_c [PMD]_{224\times224}. \end{aligned} \tag{16}$$

Let matrix $\hat{D}$ denote the combined transmitted signal as given by

$$\hat{D} = \begin{bmatrix} X_I + j \cdot X_Q \\ Y_I + j \cdot Y_Q \end{bmatrix}. \tag{17}$$

Because the received dispersed signal at the input of the ADC is related to $\hat{D}$ as given by

$$[\hat{D}]_{224\times1} = [H]_{224\times224}^{-1} \otimes_c S_I + j \cdot [H]_{224\times224}^{-1} \otimes_c S_Q, \tag{18}$$

the transmitted data matrix $\hat{D}$ can be retrieved from non-ideal outputs of the ADCs by using (11) and (18) as

$$\hat{D} = \hat{A} \otimes_c R_I + j \cdot \hat{B} \otimes_c R_Q + \hat{C}'', \tag{19}$$

where

$$\hat{A}_{224\times224} = H^{-1} \otimes_c M_I^{-1},\ \hat{B}_{224\times224} = H^{-1} \otimes_c M_Q^{-1} \tag{20}$$

and

$$\hat{C}'' = H^{-1} \otimes_c C'. \tag{21}$$

However, because the received signal is $2\times$ oversampled, only half of the components in $\hat{D}$ must be equalized. Therefore,

$$D = A \otimes_c R_I + j \cdot B \otimes_c R_Q + C'', \tag{22}$$

where

$$A_{112\times224} = \begin{bmatrix} \hat{A}_1 \\ \hat{A}_3 \\ \cdots \\ \hat{A}_{223} \end{bmatrix}, \quad B_{112\times224} = \begin{bmatrix} \hat{B}_1 \\ \hat{B}_3 \\ \cdots \\ \hat{B}_{223} \end{bmatrix} \tag{23}$$

and

$$D_{112\times1} = \begin{bmatrix} X_I^1[n] + jX_Q^1[n] \\ \cdots \\ X_I^{56}[n] + jX_Q^{56}[n] \\ Y_I^1[n] + jY_Q^1[n] \\ \cdots \\ Y_I^{56}[n] + jY_Q^{56}[n] \end{bmatrix},\ C''_{112\times1} = \begin{bmatrix} \hat{C}''_1 \\ \hat{C}''_3 \\ \cdots \\ \hat{C}''_{223} \end{bmatrix} \tag{24}$$

Equation (22) can be realized with a MIMO equalizer and the mismatches in the parallel ADCs and the channel dispersion can be compensated for simultaneously by adapting the coefficients of A, B, and C'' using an LMS algorithm.

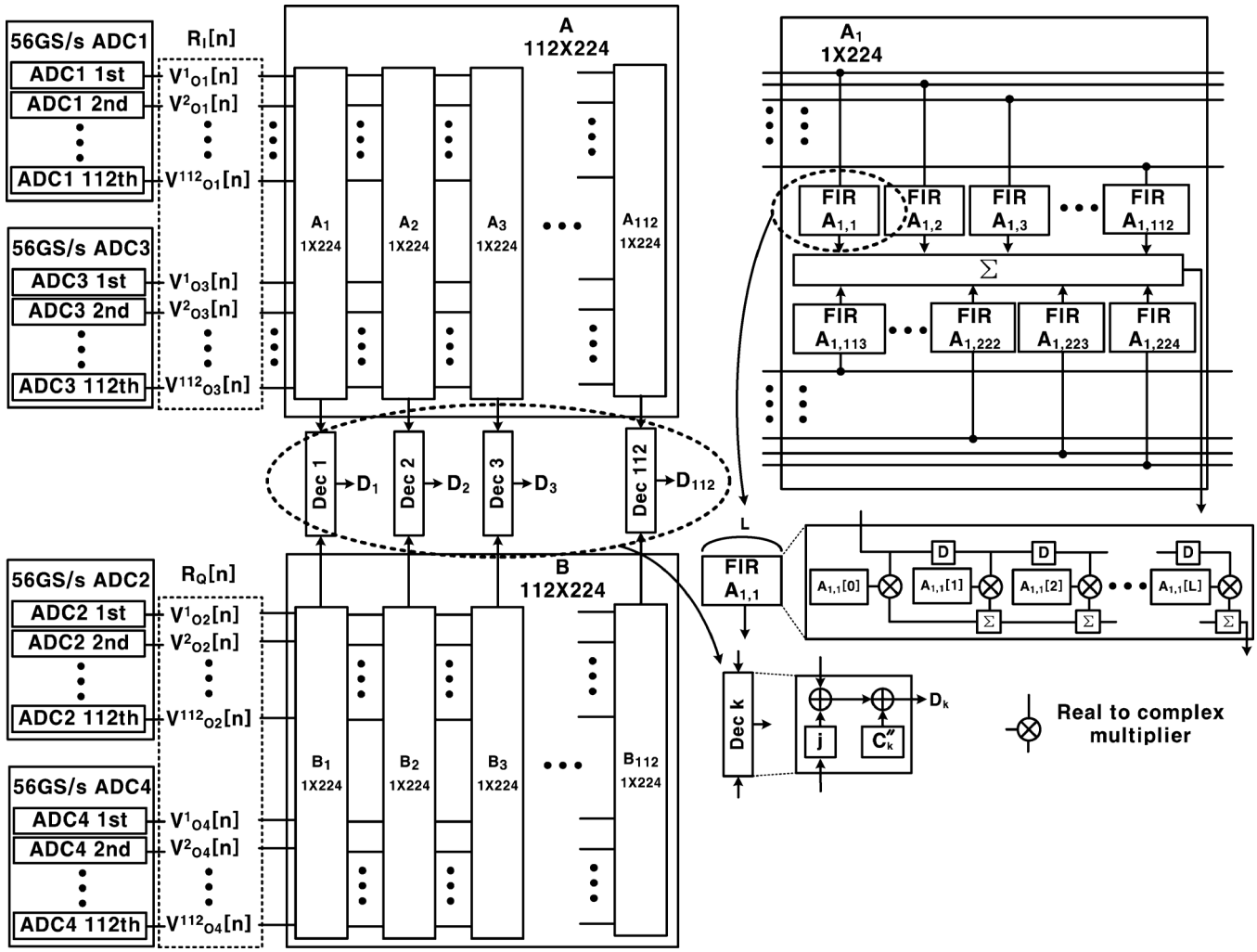

Fig. 4. Block diagram of the MIMO equalizer.

The MIMO equalizer doesn't require a front-end equalizer for the compensation of the gain and phase mismatches of an optical hybrid. It is because the MIMO equalizer can compensate for such non-idealities together with the gain and phase mismatches of an ADC.

A block diagram of the MIMO equalizer is shown in Fig. 4. $A_1 \sim A_{112}$ denote sub-equalizers and $A_{1,1} \sim A_{1,224}$ denote the coefficients of A_1, as given by

$$A = \begin{bmatrix} A_1 \\ A_2 \\ \cdots \\ A_{112} \end{bmatrix} \quad A_1 = [A_{1,1}\, A_{1,2} \cdots A_{1,224}]. \tag{25}$$

Fig. 5 shows a section of hardware utilized for the equalization of two transmitted symbols through X and Y polarizations. The length of a fractionally spaced sub-equalizer (FSE) is L. The coefficients of the FSE satisfy

$$\begin{aligned} XA_1[112 \times n + k] &= A_{1,k}[n] \quad k = 1 \ldots 112, \\ YA_1[112 \times n + k - 112] &= A_{1,k}[n] \quad k = 113 \ldots 224, \\ XB_1[112 \times n + k] &= B_{1,k}[n] \quad k = 1 \ldots 112, \\ XB_1[112 \times n + k - 112] &= B_{1,k}[n] \quad k = 113 \ldots 224. \end{aligned} \tag{26}$$

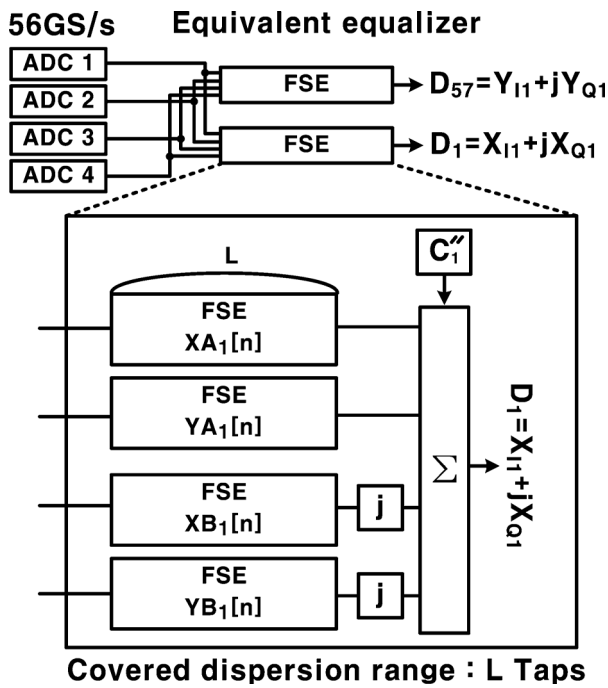

Fig. 5. Equalizer hardware for the compensation of two symbols transmitted through X and Y polarizations.

TABLE I
TABLE OF THE NUMBER OF MULTIPLIERS FOR THE EQUALIZATION OF ONE SYMBOL

	length	parallel	real-value multiplier	FSE factor	Total
(a)	L	8	2	1	$16L$
(b)	$\frac{L_1}{2}$	2	4	2	$8L_1 + 16L_2$
	L_2	4	4	1	

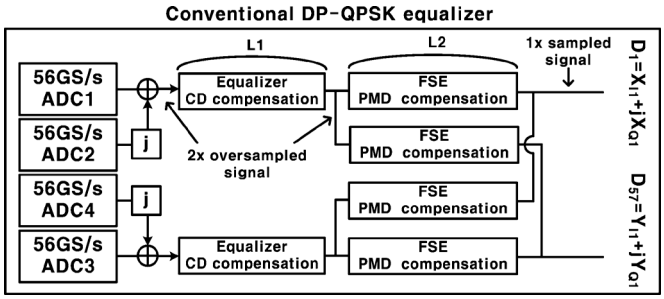

Fig. 6. Block diagram of a conventional Equalizer [15].

The total number of parallelized sub-equalizers for one polarization is 56, as 112 parallelized ADCs are oversampling the received signal by a factor of 2. The total number of real-value multiplications required for the reconstruction of two transmitted symbols X_{IQ} and Y_{IQ} in the MIMO equalizer is $L \times 8 \times 2 = 16 \times L$ as shown in Table I(a). Note that the factor of 2 is multiplied because the filter coefficients are complex numbers.

Fig. 6 shows the block diagrams of one sub-equalizer in a conventional parallel FIR equalizer for 112 Gb/s DP-QPSK coherent systems [15]. L_1 and L_2 denote the length of the FIR filter taps required for the compensation of CD and PMD, respectively. L_1 and L_2 should satisfy $L_1 + L_2 = L$ given that the dispersion compensation capabilities of conventional and MIMO equalizers are equal. CD and PMD are compensated for separately and each FSE receives complex samples from two ADCs. Because the PMD equalization process is performed sequentially, the CD equalizer should maintain a $2\times$ oversampling ratio to minimize the SNR penalty in the PMD compensator. Note that both filter coefficients and sampled ADC outputs are complex in this case. However, the reduction of the number of multipliers for the CD equalization to $(L_1)/(2)$ is possible because of the even symmetry of the impulse response [8]. Therefore, the total number of real-value multiplications required for the reconstruction of two transmitted symbols X_{IQ} and Y_{IQ} in the conventional equalizer is $((L_1)/(2) \times 2 \times 2 + L_2 \times 4) \times 4 = 8 \times L_1 + 16 \times L_2$ which is smaller than $16 \times L$ as shown in Table I(b). For 80 km metro applications, $L_1 = 32$ and $L_2 = 9$ taps are required for CD and PMD compensations [8] and the expected power ratio between the MIMO and the conventional equalizer is

$$\frac{P_{\text{MIMO}}}{P_{\text{conventional}}} = \frac{16 \times L}{16 \times L_2 + 8 \times L_1} = 1.64. \tag{27}$$

Consequently, the MIMO equalizer has 64% power penalty in terms of multiplier counts over conventional FIR equalizers.

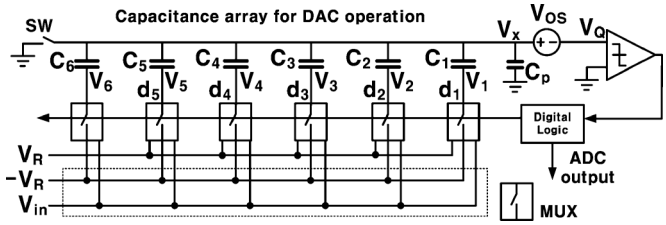

Fig. 7. Block diagram of a five-bit switched-capacitor SAR-ADC.

B. ADC Nonlinearity Compensation

SAR ADC is considered as most suitable type for coherent optical communication. [4] It has been shown that the non-linearity of a SAR ADC can be compensated for using a digital-domain signal processing method [10]. Unlike the previous work which uses a reference ADC for calibration, the proposed DA MIMO equalizer can compensate for the nonlinearity of a SAR ADC and channel dispersion simultaneously by using the estimated output mean square error. Because this compensation process is an interpretation rather than a calibration scheme to deal with the non-linearity, a certain amount of SNR penalty at the final output can exist.

A SAR ADC consists of a capacitance array for digital-to-analog conversion (DAC), a comparator for the decision, and a digital logic block for the DAC control (see Fig. 7) [10]. When switch SW is connected during the sampling period, the input signal V_{in} is sampled at the bottom plate of the capacitor array and $V_1 \sim V_6$ become V_{in}. The switch SW is turned off after the sampling period and $V_1 \sim V_6$ are connected to $-V_R$. The voltage change at V_x, defined as ΔV_x, is related to the voltage changes at $V_1 \sim V_6$ as given by

$$\frac{\Delta V_x}{\Delta V_i} = \frac{C_i}{C_{\text{tot}} + C_p} = K_i \quad i \in \{1 \dots 6\} \tag{28}$$

where ΔV_i denotes the voltage change at V_i, $C_{\text{tot}} = \Sigma_{i=1}^{6} C_i$ and C_p is the parasitic capacitance. The total voltage change ΔV_x is

$$\Delta V_x = \Sigma_{i=1}^{6} K_i \Delta V_i = \Sigma_{i=1}^{6} K_i(-V_R - V_{\text{in}}). \tag{29}$$

The capacitor array receives digital codes $d1 \sim d5$ from the digital logic block and adds the corresponding analog voltage to the sampled input signal V_{in} using a charge redistribution process. The digital logic block uses a binary search algorithm to find the digital code which takes V_x to the sub-LSB level. V_x is related to the digital code $d1 \sim d5$, V_{in} and V_R as given by

$$\begin{aligned} V_x &= \Sigma_{i=1}^{6} K_i(-V_R - V_{\text{in}}) + \Sigma_{i=1}^{5} d_i \cdot 2K_i V_R \\ &= \Sigma_{i=1}^{5}(2d_i - 1)K_i V_R - K_0 V_R - K_{\text{tot}} V_{\text{in}}, \end{aligned} \tag{30}$$

where

$$K_{\text{tot}} = \Sigma_{i=1}^{6} K_i = \frac{C_{\text{tot}}}{C_{\text{tot}} + C_p}. \tag{31}$$

Hence, the input signal V_{in} is

$$\begin{aligned} V_{\text{in}} &= K_{\text{tot}}^{-1}\left(\Sigma_{i=1}^{5}(2d_i - 1)K_i V_R - K_0 V_R - V_x\right) \\ &= K_{\text{tot}}^{-1}\left(\Sigma_{i=1}^{5}(2d_i - 1)K_i V_R - K_0 V_R - (V_Q + V_{os})\right), \end{aligned} \tag{32}$$

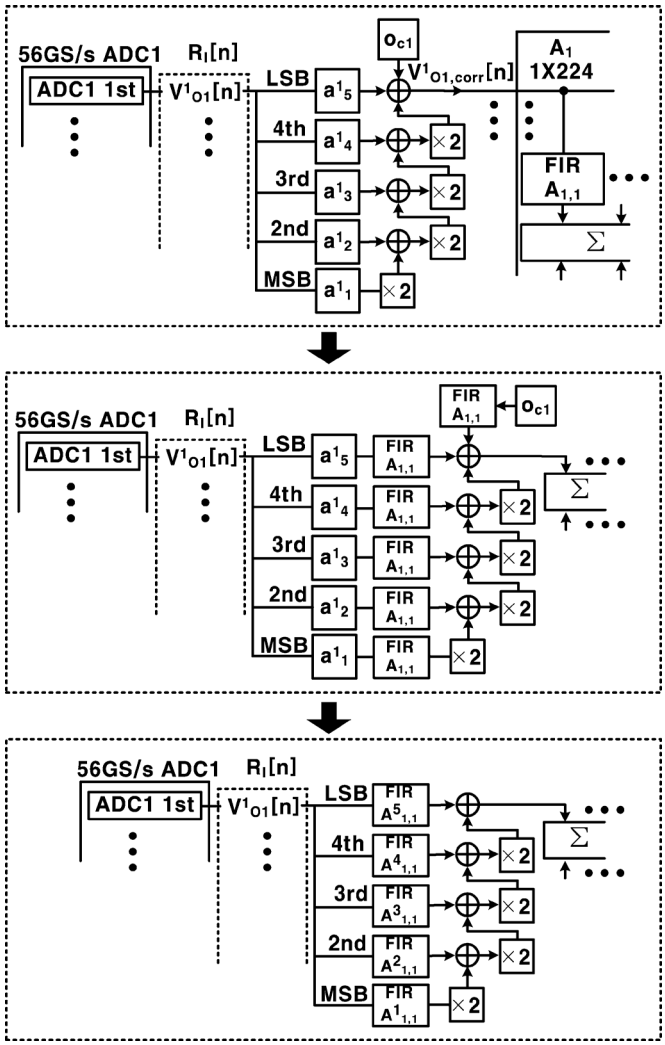

Fig. 8. Conceptual block diagram: Merging coefficients for nonlinearity compensation with those for MIMO equalization.

where V_{os} and V_Q are the comparator offset and the quantization noise, respectively. Equation (32) shows that the input signal $V_{\rm in}$ can be accurately reconstructed from digital codes $d1 \sim d5$ by multiplying adequate coefficients with each bit and adding a proper offset in a SAR ADC.

The corrected output signal $V_{O,\rm corr}$ of a five-bit SAR ADC can be written as

$$V_{O,\rm corr} = \Sigma_{i=1}^{5} a_i \times d_i + o_c, \tag{33}$$

where a_i and o_c are the coefficient and offset for the correction, respectively. The correction factors a_i and o_c were retrieved using a slow-but-accurate reference ADC in the earlier work [10]. However, a_i can be combined with the filter coefficients of the digital FIR filter by using a DA scheme as shown in Fig. 8, and adjusted adaptively by an LMS algorithm. Fig. 9 shows a block diagram of a sub-equalizer of the DA MIMO equalizer. The coefficient $A_{j,k}^{i}$ in the DA MIMO equalizer is related to that of the MIMO equalizer $A_{j,k}$ in (25) as given by

$$A_{j,k}^{i} = a_i^k \times A_{j,k},$$
$$i = 1 \cdots 5,\ j = 1 \ldots 112,\ k = 1 \ldots 224 \tag{34}$$

where the correction factor a_i^k satisfies

$$V_{O1,\rm corr}^{k} = \Sigma_{i=1}^{5} a_i^k \times d_i^k + o_c^k,$$
$$V_{O3,\rm corr}^{k} = \Sigma_{i=1}^{5} a_i^{k+112} \times d_i^{(k+112)} + o_c^{k+112}.$$
$$k = 1 \ldots 112 \tag{35}$$

In summary, channel dispersion and ADC nonlinearity can be compensated for simultaneously by multiplying different FIR filter coefficients $A_{j,k}^{1} \cdots A_{j,k}^{5}$ with each ADC output bit and combining them at the output. The offset correction factor o_c is implemented in the last stage of the DA MIMO equalizer by subtracting the average values of output $E_{i,j}$ from the recovered symbols. This process aligns the center of the QPSK signal space of each sub-equalizer to the origin.

IV. A Variable-Precision Distributed Arithmetic (VPDA) MIMO Equalizer

The VPDA MIMO equalizer reduces the dynamic power consumption of the DA MIMO equalizer by using only the minimum required resolution for the equalization of each dispersed symbol. Fig. 11 shows the equalized QPSK symbols under different ADC resolutions in a two-dimensional signal space. The magnitude of the standard deviation σ_k and the resulting BER are inversely proportional to the resolution of the ADC. However, equalized symbols located distant from decision thresholds in the signal space can be correctly determined with high probability even under low ADC resolutions. In other words, the required resolution for the equalization of each dispersed symbol is different. Fig. 10 shows a conceptual block diagram of the proposed variable-precision algorithm. The proposed pipelined equalizer begins the computation from the most significant bit (MSB) towards the least significant bit (LSB) sequentially. Range checkers are inserted between the sub-equalizers described in Fig. 9 to determine whether further computation with a higher resolution is required. In case a partially equalized symbol is located outside the suspicious region in the signal space (see Fig. 10), a final decision is made and no further computations are performed. In contrast, if the partial result is within the suspicious region, the precision of the partial result is increased by one bit and the location of the equalized symbol in the signal space is rechecked. Thus, the average resolution for the equalization can be reduced significantly and hence the dynamic power consumption can also be decreased.

The estimated power ratio of the VPDA MIMO equalizer over the DA MIMO equalizer is approximately

$$\frac{P_{\rm VPDA}}{P_{\rm DA}} = \frac{P_{\rm VPDA}}{P_{\rm MIMO}} \approx \Sigma_{k=1}^{5} \frac{1}{5} \times \Pr(En_k), \tag{36}$$

where $P_{\rm VPDA}$ and $P_{\rm DA}$ are the power consumptions of the VPDA MIMO and the DA MIMO equalizers, respectively, and $\Pr(En_k)$ denotes the probability that a single bit equalizer at each resolution step is being enabled as shown in Fig. 12. The power consumption of the VPDA MIMO equalizer at each resolution step is approximately $(1/5)$ that of the DA MIMO equalizer. It is because the total power consumption of the

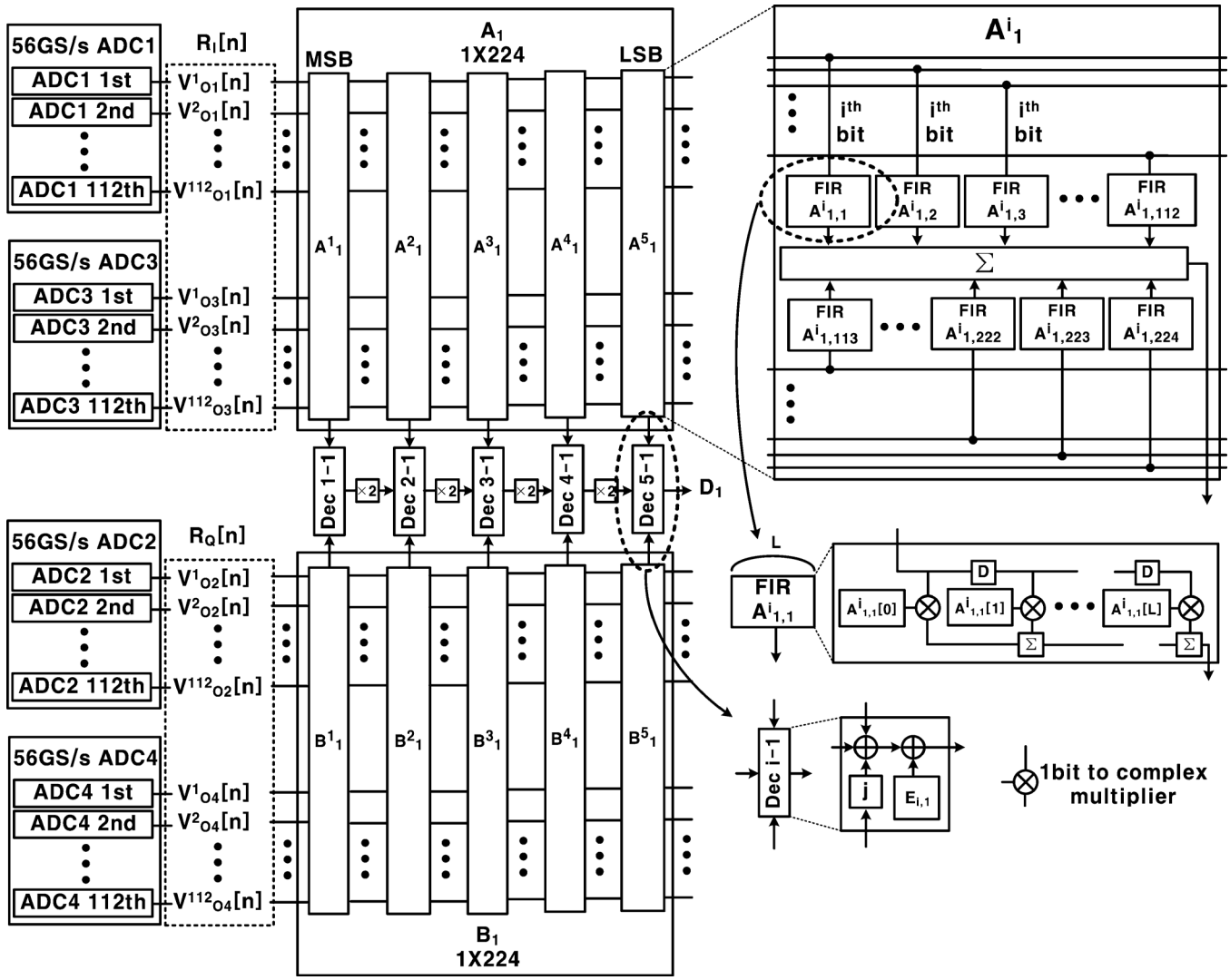

Fig. 9. Block diagram of a sub-equalizer in a DA MIMO equalizer.

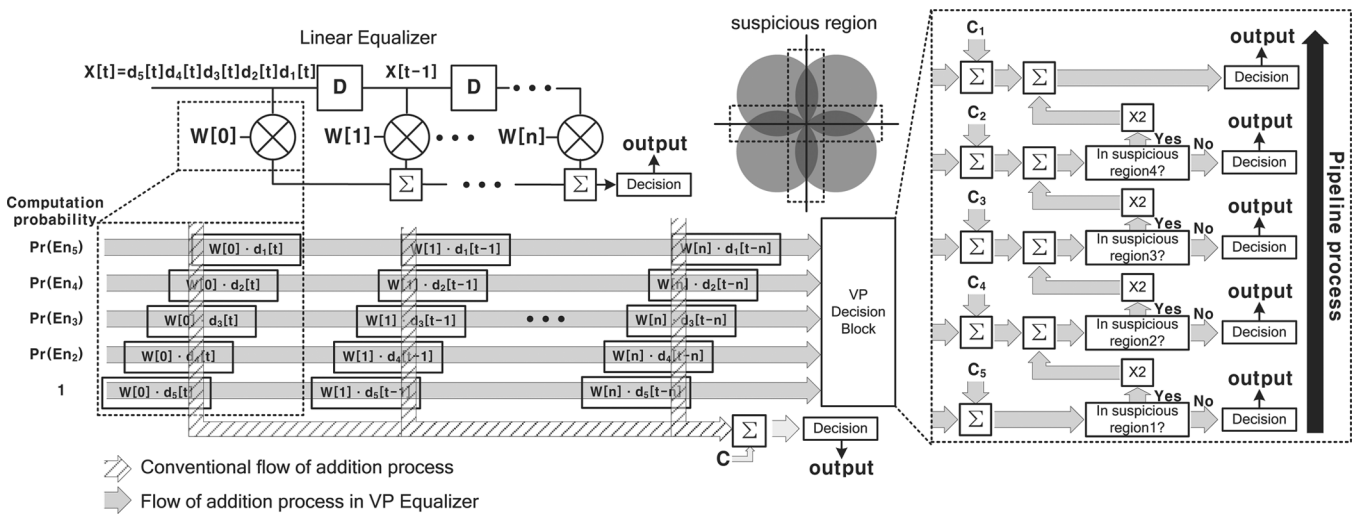

Fig. 10. Block diagram of the variable precision algorithm.

VPDA MIMO equalizer including all resolution step should be identical to that of the DA MIMO equalizer employing conventional multiplication process as shown in Fig. 10.

The probability $\Pr(En_k)$ is determined by both SNR and the area of suspicious region at each resolution step. Proper selection of the suspicious region in the signal space is crucial for

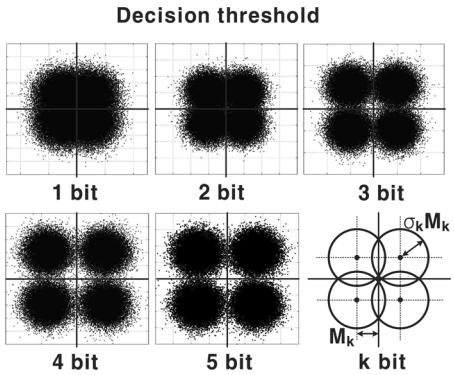

Fig. 11. Constellations of the equalized symbol with various ADC resolutions.

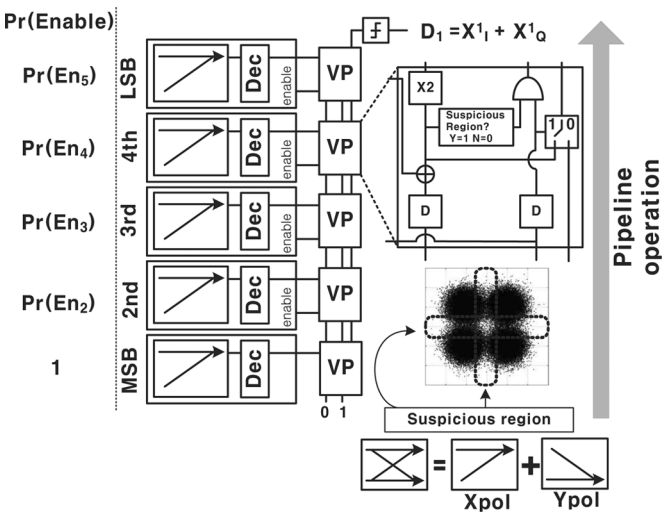

Fig. 12. Block diagram of the VPDA MIMO equalizer.

the VPDA MIMO equalizer because premature inaccurate decisions caused by insufficient area of the suspicious regions increase BER penalty.

Therefore, the design target for the dynamic power minimization of the VPDA MIMO equalizer is to minimize the average ADC resolution by minimizing the area of the suspicious regions without a significant BER penalty. The transition rate, defined as the probability of an equalized symbol being in the suspicious region in the kth stage depends on both the size of the suspicious region in the current stage and the transition rate in the previous stages. Thus, the size of the suspicious regions should be determined sequentially from MSB to LSB. The suspicious region of the first stage, Sus_1, is determined based on the BER while assuming that the suspicious regions in the subsequent stage are infinite and that no extra bit-error occurs from the variable-precision architecture. The estimated BER at the output of the first stage is

$$\begin{aligned}\mathrm{BER} = {} & \Pr\left(\text{bit error} \cap P_1^c\right) \\ & + \Pr\left(\text{bit error} \cap P_1 \cap P_5^c\right), \end{aligned} \quad (37)$$

where P_k denotes the set of events that the output symbol in the kth stage, $\mathrm{Sym}_k = (X_k, Y_k)$, is in the suspicious region and P_k^c

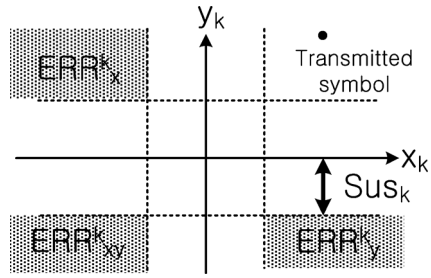

Fig. 13. Erroneous regions in the QPSK signal space when (1,1) is sent.

denotes the complementary set of P_k. In case symbol (1,1) is transmitted, $\Pr(\text{bit error} \cap P_k^c)$ can be expanded as

$$\begin{aligned}& \Pr\left(\text{bit error} \cap P_k^c\right) \\ & \quad = \Pr\left(\text{bit error} \mid E_k^x\right) \cdot \Pr\left(E_k^x\right) \\ & \qquad + \Pr\left(\text{bit error} \mid E_k^y\right) \cdot \Pr\left(E_k^y\right) \\ & \qquad + \Pr\left(\text{bit error} \mid E_k^{xy}\right) \cdot \Pr\left(E_k^{xy}\right), \end{aligned} \quad (38)$$

where E_k^x, E_k^y and E_k^{xy} are the sets of erroneous events, as given by

$$\begin{aligned} E_k^x &= \left\{\mathrm{Sym}_k \in \mathrm{ERR}_x^k\right\} \\ E_k^y &= \left\{\mathrm{Sym}_k \in \mathrm{ERR}_y^k\right\} \\ E_k^{xy} &= \left\{\mathrm{Sym}_k \in \mathrm{ERR}_{xy}^k\right\}, \end{aligned} \quad (39)$$

and where ERR_x^k, ERR_y^k and ERR_{xy}^k denote the areas shown in Fig. 13. Note that the conditional probabilities in (38) are

$$\begin{aligned} \Pr\left(\text{bit error} \mid E_k^x\right) &= \frac{1}{2}, \\ \Pr\left(\text{bit error} \mid E_k^y\right) &= \frac{1}{2}, \\ \Pr\left(\text{bit error} \mid E_k^{xy}\right) &= 1. \end{aligned} \quad (40)$$

Because the two-dimensional probability density function of Sym_k is symmetric with respect to $Y_k = X_k$, (38) can be simplified to

$$\begin{aligned}& \Pr\left(\text{bit error} \cap P_k^c\right) \\ & \quad = \frac{1}{2} \cdot \Pr\left(E_k^x\right) + \frac{1}{2} \cdot \Pr\left(E_k^y\right) + \Pr\left(E_k^{xy}\right) \\ & \quad = \Pr\left(E_k^x\right) + \Pr\left(E_k^{xy}\right) = \Pr\left(E_k^x \cup E_k^{xy}\right). \end{aligned} \quad (41)$$

Because the noise in each equalized symbol is a linear combination of independent and identically distributed (i.i.d) additive noises caused by quantization and limited input signal-to-noise ratio in each sample, it can be assumed to show a Gaussian distribution according to the central limit theorem. Then, the probabilities $\Pr(E_k^x)$ and $\Pr(E_k^{xy})$ are given by

$$\begin{aligned}\Pr\left(E_k^x\right) &= \int_{-\infty}^{-\mathrm{Sus}_1} \int_{\mathrm{Sus}_1}^{\infty} g(x, 1, \sigma_k) \cdot g(y, 1, \sigma_k) dx dy \\ &= Q\left(\frac{\mathrm{Sus}_1 + 1}{\sigma_k}\right) \cdot Q\left(\frac{\mathrm{Sus}_1 - 1}{\sigma_k}\right) \end{aligned} \quad (42)$$

$$\begin{aligned}\Pr\left(E_k^{xy}\right) &= \int_{-\infty}^{-\mathrm{Sus}_1} \int_{-\infty}^{-\mathrm{Sus}_1} g(x, 1, \sigma_k) \cdot g(y, 1, \sigma_k) dx dy \\ &= Q\left(\frac{\mathrm{Sus}_1 + 1}{\sigma_k}\right)^2, \end{aligned} \quad (43)$$

where σ_k is the standard deviation of the noise at kth stage and $g(x, \mu, \sigma)$ is a Gaussian function, as given by

$$g(x, \mu, \sigma) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{\frac{(x-\mu)^2}{2\sigma^2}}. \tag{44}$$

Because P_k is symmetrical with respect to $Y_k = X_k$, $\Pr(\text{bit error} \cap P_m \cap P_n^c), m \leq n$ can be written using (41) as

$$\begin{aligned}&\Pr\left(\{\text{bit error} \cap P_n^c\} \cap P_m\right)\\ &\quad = \Pr\left(\{E_n^x \cup E_n^{xy}\} \cap P_m\right)\\ &\quad = \Pr\left(E_n^x \cap P_m\right) + \Pr\left(E_n^{xy} \cap P_m\right).\end{aligned} \tag{45}$$

Let $N_{m,n}$ be the noise added to the equalized output signal when ADC resolution is reduced from n bit to m bit. $N_{m,n}$ can be modeled by a Gaussian distribution of $N(0, \sqrt{\sigma_m^2 - \sigma_n^2})$. Then, $\Pr(E_n^x \cap P_m)$ is given by

$$\begin{aligned}&\Pr\left(E_n^x \cap P_m\right)\\ &\quad = \Pr(\{X_n < -\text{Sus}_n\} \cap \{\text{Sus}_n < Y_n\}\\ &\qquad \cap \{\{-\text{Sus}_m < X_m < \text{Sus}_m\}\\ &\qquad \cup \{-\text{Sus}_m < Y_m < \text{Sus}_m\}\})\\ &\quad = \Pr(\{X_n < -\text{Sus}_n\} \cap \{\text{Sus}_n < Y_n\}\\ &\qquad \cap \{\{-\text{Sus}_m < N_{m,n}^x + X_n < \text{Sus}_m\}\\ &\qquad \cup \{-\text{Sus}_m < N_{m,n}^y + Y_n < \text{Sus}_m\}\})\\ &\quad = \Pr(\{X_n < -\text{Sus}_n\} \cap \{\text{Sus}_n < Y_n\}\\ &\qquad \cap \{\{-\text{Sus}_m - X_n < N_{m,n}^x < \text{Sus}_m - X_n\}\\ &\qquad \cup \{-\text{Sus}_m - Y_n < N_{m,n}^y < \text{Sus}_m - Y_n\}\}).\end{aligned} \tag{46}$$

Equation (46) is changed to

$$\begin{aligned}&\Pr\left(E_n^x \cap P_m\right)\\ &\quad = \Pr(\{X_n < -\text{Sus}_n\} \cap \{\text{Sus}_n < Y_n\}\\ &\qquad \cap \{-\text{Sus}_m - X_n < N_{m,n}^x < \text{Sus}_m - X_n\}\})\\ &\qquad + \Pr(\{X_n < -\text{Sus}_n\} \cap \{\text{Sus}_n < Y_n\}\\ &\qquad \cap \{-\text{Sus}_m - Y_n < N_{m,n}^y < \text{Sus}_m - Y_n\}\})\\ &\qquad - \Pr(\{X_n < -\text{Sus}_n\} \cap \{\text{Sus}_n < Y_n\}\\ &\qquad \cap \{\{-\text{Sus}_m - X_n < N_{m,n}^x < \text{Sus}_m - X_n\}\\ &\qquad \cap \{-\text{Sus}_m - Y_n < N_{m,n}^y < \text{Sus}_m - Y_n\}\}).\end{aligned} \tag{47}$$

Similarly, $\Pr(E_n^{xy} \cap P_m)$ is

$$\begin{aligned}&\Pr\left(E_n^{xy} \cap P_m\right)\\ &\quad = \Pr\left(\{X_n < -\text{Sus}_n\} \cap \{Y_n < -\text{Sus}_n\}\right.\\ &\qquad \left.\cap \left\{-\text{Sus}_m - X_n < N_{m,n}^x < \text{Sus}_m - X_n\right\}\right)\\ &\qquad + \Pr(\{X_n < -\text{Sus}_n\} \cap \{Y_n < -\text{Sus}_n\}\\ &\qquad \cap \left\{-\text{Sus}_m - Y_n < N_{m,n}^y < \text{Sus}_m - Y_n\right\}\})\\ &\qquad - \Pr(\{X_n < -\text{Sus}_n\} \cap \{Y_n < -\text{Sus}_n\}\\ &\qquad \cap \left\{\left\{-\text{Sus}_m - X_n < N_{m,n}^x < \text{Sus}_m - X_n\right\}\right.\\ &\qquad \left.\cap \left\{-\text{Sus}_m - Y_n < N_{m,n}^y < \text{Sus}_m - Y_n\right\}\right).\end{aligned} \tag{48}$$

Assuming that the random variables X_n, Y_n, $N_{m,n}^x$ and $N_{m,n}^y$ are independent, (46) becomes

$$\begin{aligned}&\Pr\left(E_n^x \cap P_m\right)\\ &\quad = \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(x_n)dx_n \cdot Q\left(\frac{-1 + \text{Sus}_n}{\sigma_n}\right)\\ &\qquad + \int_{\text{Sus}_n}^{\infty} F_{m,n}(y_n)dy_n \cdot Q\left(\frac{1 + \text{Sus}_n}{\sigma_n}\right)\\ &\qquad - \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(x_n)dx_n \cdot \int_{\text{Sus}_n}^{\infty} F_{m,n}(y_n)dy_n,\end{aligned} \tag{49}$$

where $F_{m,n}(x)$ is defined in (50):

$$\begin{aligned}F_{m,n}(x) = &\left(Q\left(\frac{-\text{Sus}_m - x}{\sqrt{\sigma_m^2 - \sigma_n^2}}\right) - Q\left(\frac{\text{Sus}_m - x}{\sqrt{\sigma_m^2 - \sigma_n^2}}\right)\right)\\ &\cdot g(x, 1, \sigma_n).\end{aligned} \tag{50}$$

Similarly, $\Pr(E_n^{xy} \cap P_m)$ is given by

$$\begin{aligned}&\Pr\left(E_n^{xy} \cap P_m\right)\\ &\quad = \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(x_n)dx_n \cdot Q\left(\frac{1 + \text{Sus}_n}{\sigma_n}\right)\\ &\qquad + \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(y_n)dy_n \cdot Q\left(\frac{1 + \text{Sus}_n}{\sigma_n}\right)\\ &\qquad - \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(x_n)dx_n \cdot \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(y_n)dy_n\\ &\quad = 2 \cdot \int_{-\infty}^{-\text{Sus}_n} F_{m,n}(x_n)dx_n \cdot Q\left(\frac{1 + \text{Sus}_n}{\sigma_n}\right)\\ &\qquad + \left(\int_{-\infty}^{-\text{Sus}_n} F_{m,n}(x_n)dx_n\right)^2\end{aligned} \tag{51}$$

The addition of (49) and (51) renders the conditional probability of $\Pr(\{\text{bit error} \cap P_n^c\} \cap P_m)$. Then, the relationship between Sus_1 and BER can be achieved from (37) and the minimum Sus_1 satisfying a BER target can be chosen. The relationship between BER and Sus_2 with the minimum Sus_1 value chosen above is

$$\begin{aligned}\text{BER} = &\Pr\left(\text{bit error} \cap P_1^c\right)\\ &+ \Pr\left(\text{bit error} \cap P_1 \cap P_2^c\right)\\ &+ \Pr\left(\text{bit error} \cap P_1 \cap P_2 \cap P_5^c\right).\end{aligned} \tag{52}$$

$\Pr(\text{bit error} \cap P_1 \cap P_2 \cap P_5^c)$ can be simplified to $\Pr(\text{bit error} \cap P_2 \cap P_5^c)$ given that Sus_2 is smaller than Sus_1; thus, $P_1 \cap P_2 \approx P_2$. In general, the relationship between BER and Sus_k with a predetermined minimum $\text{Sus}_1 \cdots \text{Sus}_{k-1}$ is given by

$$\begin{aligned}\text{BER} = &\Pr\left(\text{bit error} \cap P_1^c\right)\\ &+ \Sigma_{i=2}^{k} \Pr\left(\text{bit error} \cap P_{i-1} \cap P_i^c\right)\\ &+ \Pr\left(\text{bit error} \cap P_k \cap P_5^c\right)\\ &k = 2, 3, 4\end{aligned} \tag{53}$$

provided that

$$\Pr(P_1 \cap P_2 \ldots P_k) \approx \Pr(P_k), \tag{54}$$

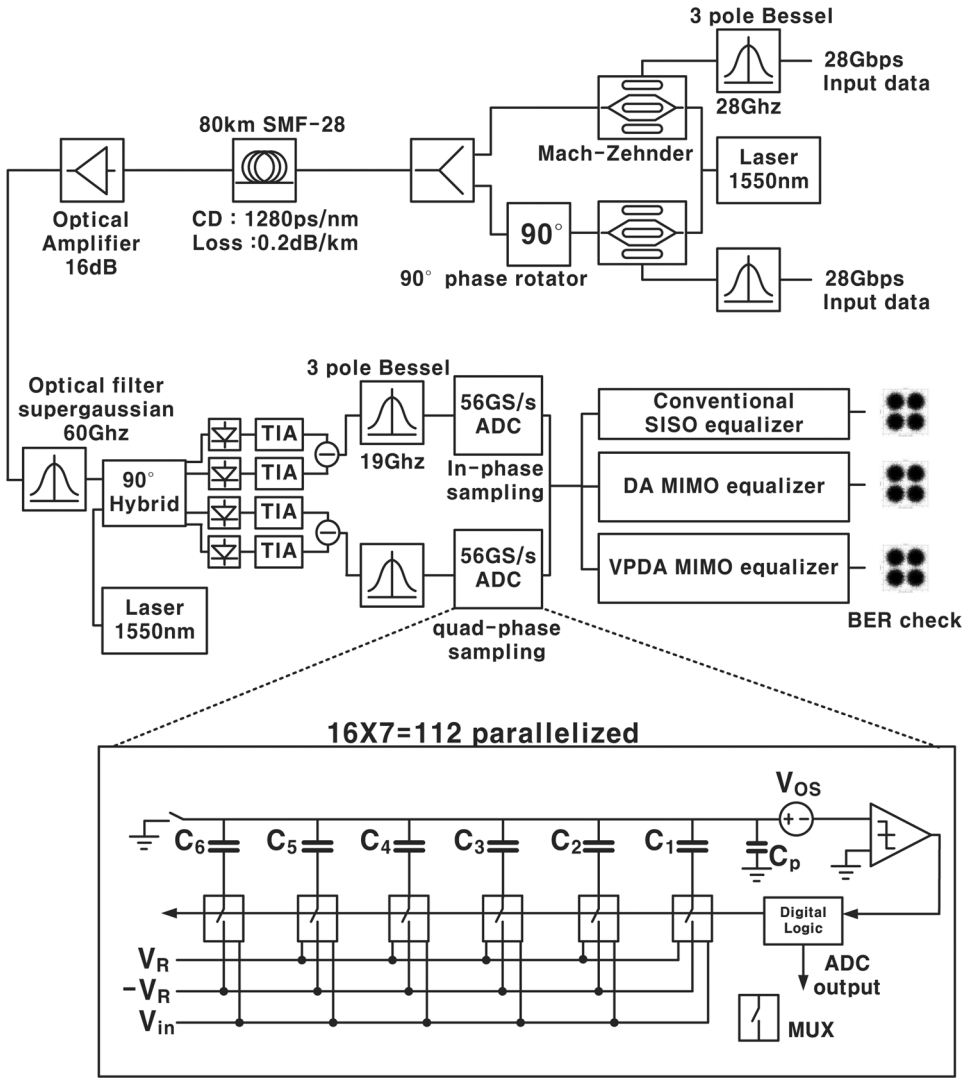

Fig. 14. Simulation setup.

where $\Pr(P_k)$ is derived in (55).

$$\begin{aligned}\Pr(P_k) &= \Pr(\{-\mathrm{Sus}_k < X_k < \mathrm{Sus}_k\} \\ &\quad \cup \{-\mathrm{Sus}_k < Y_k < \mathrm{Sus}_k\}) \\ &= \Pr(\{-\mathrm{Sus}_k < X_k < \mathrm{Sus}_k\}) \\ &\quad + \Pr(\{-\mathrm{Sus}_k < Y_k < \mathrm{Sus}_k\}) \\ &\quad - \Pr(\{-\mathrm{Sus}_k < X_k < \mathrm{Sus}_k\} \\ &\quad \cap \{-\mathrm{Sus}_k < Y_k < \mathrm{Sus}_k\}) \\ &= 2 \cdot \left(Q\left(\frac{-1-\mathrm{Sus}_k}{\sigma_k}\right)\right. \\ &\quad \left. -Q\left(\frac{-1+\mathrm{Sus}_k}{\sigma_k}\right)\right) \\ &\quad - \left(Q\left(\frac{-1-\mathrm{Sus}_k}{\sigma_k}\right)\right. \\ &\quad \left. -Q\left(\frac{-1+\mathrm{Sus}_k}{\sigma_k}\right)\right)^2. \\ &\qquad\qquad k = 1 \ldots 4 \\ \Pr(P_5) &= 0 \end{aligned} \tag{55}$$

Finally, the dynamic power reduction ratio of the VPDA MIMO equalizer can be estimated by using (36) because $\Pr(P_k) = \Pr(En_{k+1})$.

V. Simulation

The simulation setup of the VPDA MIMO equalizer is shown in Fig. 14. The channel and optical components are modeled using OPTSIM and the equalizer is simulated using MATLAB. Chromatic dispersion up to 1280 ps/nm, equivalent to 80 km in SMF-28 single mode fiber at a wavelength of 1550 nm, without PMD is considered as the channel impairment. Hence, 56 Gbps QPSK data transmitted through a single polarization is used for the verification of the proposed VPDA MIMO architecture for simplicity. The bandwidth of the optical filter at the receiver is set to 60 GHz and third-order Bessel filters with a bandwidth of 19 GHz are used. 201322 randomly generated bits are used for the BER simulation, where the BER target is 10^{-3}. The data sampled by the two nonlinear 56 GS/s ADCs is fed into a conventional equalizer, a DA MIMO equalizer and a VPDA MIMO equalizer for comparison. The tap length of each equalizer is 32 and the coefficients are adapted using an LMS algorithm. A total

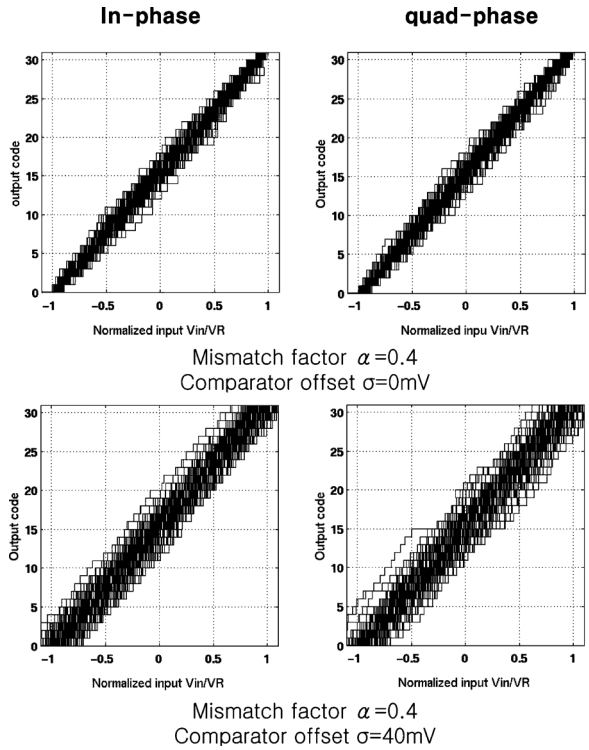

Fig. 15. Randomly generated total 224 nonlinear characteristics of the SAR-ADCs.

TABLE II
NORMALIZED STANDARD DEVIATIONS OF EQUALIZED SYMBOLS UNDER VARIOUS ADC RESOLUTION

resolution	1-bit	2-bit	3-bit	4-bit	5-bit
σ_k	0.7262	0.5045	0.3931	0.3534	0.3407

of $16 \times 7 \times 2 = 224$ different nonlinear characteristics of SAR ADCs are randomly generated for two 56 GS/s ADCs by randomizing the capacitance mismatches and comparator offsets. The standard deviations of the capacitances are set proportional to $\sqrt{\text{area}}$ [16], as given by

$$\begin{aligned} \sigma_{C_k} &= \alpha \times \sqrt{2^{5-k}} \times C_6 \\ C_k &= 2^{5-k} \times C_6, \quad k = 1 \ldots 5 \\ C_5 &= C_6, \end{aligned} \tag{56}$$

where α is a process parameter. In this simulation α is set to 0.4 [16]. The standard deviation of the comparator offset is set to 40 mV and the full scale of the ADC is set to $\pm 400\ \text{mV}_{\text{peak}-\text{peak}}$. Total 112 randomly generated nonlinear characteristics of a single ADC are shown in Fig. 15. The gain and sampling phase mismatches between 16 track and hold circuits are randomly generated with standard deviations of 0.2 V/V and 4 ps $(0.22UI)$, respectively. The precisions of the coefficients of the DA and VPDA MIMO FIR equalizers are set to 8 bit in order to suppress the penalty due to the finite precision below 0.1 dB at a BER of 10^{-3}.

The simulated values of σ_k in Fig. 11 for the different ADC resolutions are summarized in Table II. The relationships between BER and the range of the suspicious regions for each VPDA MIMO stage from (53) are plotted as solid lines in Fig. 16. The hollow circle markers in the figure denote the simulated BER points. The analytic results (lines) discussed in Section IV closely match the simulation results (hollow circle). The normalized suspicious regions with respect to the QPSK signal space for each level of ADC precision from MSB to LSB are set to 1.82, 0.86, 0.44 and 0.19 as shown in Fig. 16 considering the BER penalty. Table III summarizes the analytical and simulated enable rate of the equalizer at each resolution step with the suspicious regions selected in the above. The estimated dynamic power ratio of the proposed VPDA MIMO equalizer over the DA MIMO equalizer is 0.55 from (36) and thus 45% of dynamic power consumption can be reduced. The power ratio of the VPDA MIMO and the conventional equalizer, by using 1.64 achieved in (27), is

$$\frac{P_{\text{VPDA}}}{P_{\text{conventional}}} = \frac{P_{\text{VPDA}}}{P_{\text{DA}}} \times 1.64 = 0.9. \tag{57}$$

Consequently, the VPDA MIMO equalizer achieves 10% power reduction over conventional approaches.

TABLE III
ENABLE RATE OF A SINGLE BIT EQUALIZER

$Pr(En_k)$	$Pr(En_2)$	$Pr(En_3)$	$Pr(En_4)$	$Pr(En_5)$
Eq.(55)	0.983	0.625	0.147	0.021
simulation	0.985	0.624	0.143	0.020

Fig. 17 shows the simulated OSNR vs. BER graphs for three different equalizers. The VPDA MIMO equalizer with the dynamic power reduction of 45% shows a negligible OSNR penalty compared to the DA MIMO equalizer. The VPDA MIMO equalizer subsequent to the non-ideal ADCs shows a 0.5 dB worst-case OSNR penalty compared to the ideal five-bit ADCs followed by an ideal equalizer at a BER of 10^{-3}. In contrast, the conventional equalizer with an identical non-ideal ADCs shows an OSNR penalty of more than 2.5 dB at a BER of 10^{-3}.

The adaptation speed of the VPDA MIMO equalizer is 56 times slower than that of a conventional parallel equalizer because one adaptation engine sequentially sets the coefficients of 56 parallel sub-equalizers. Fig. 18 shows the simulated tracking performance of the VPDA MIMO equalizer under the rotation of the polarization plane at a rate of 50 rad/s. Such a rotational rate is considered severe in 80 km applications [17]. Variable precision scheme is disabled for simplicity. SNR is set to 13.5 dB and the initial coefficients of the VPDA MIMO equalizer are set to 0. The clock frequency is 500 MHz and the BER is measured every 3.6 μs. The estimated time constant of the adaptation engine is less than 2 ms and the VPDA MIMO equalizer demonstrates negligible BER penalty.

VI. CONCLUSION

A power-and-area efficient BER-aware VDPA MIMO architecture for a 112 Gb/s DP-QPSK coherent receiver is presented. The VPDA MIMO equalizer achieves almost same dynamic power consumption as conventional FIR equalizers and does not require area-hungry analog domain calibration circuits for the ADC. The VPDA MIMO architecture is an area-and-power efficient architecture for distances less than 120 km where the time domain equalization shows less complexity than the frequency

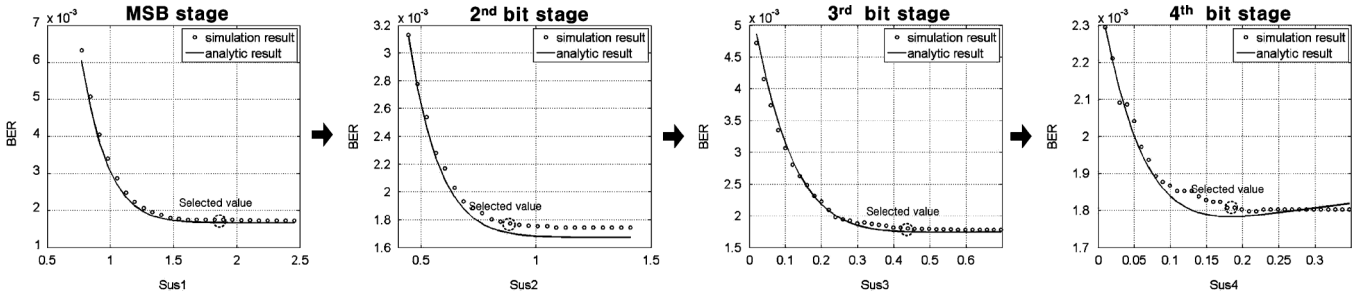

Fig. 16. BER increment with respect to the size of the suspicious regions for each stage.

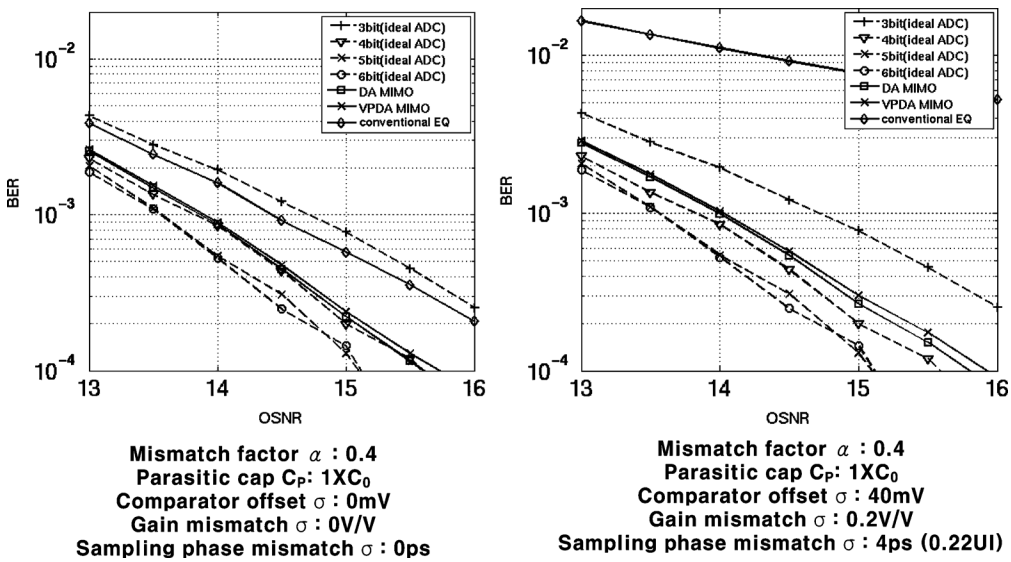

Fig. 17. Simulation results of the VPDA MIMO equalizer.

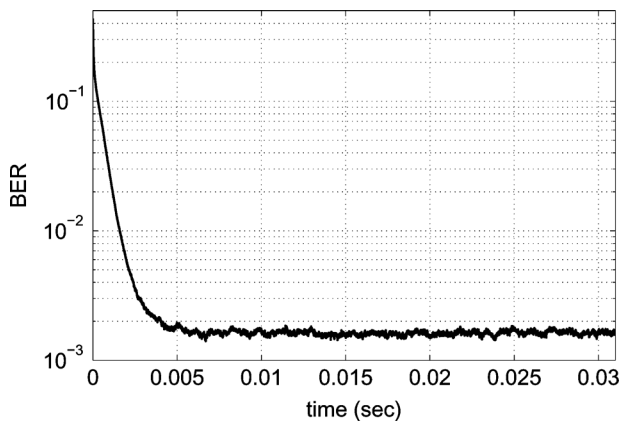

Fig. 18. Tracking performance of the VPDA MIMO equalizer.

domain counterparts [8]. However, architectural improvements on the VPDA MIMO equalizer, such as combining ADC's non-ideality compensator with the frequency domain channel equalizer, are required in order to extend the target reach beyond 120 km efficiently.

ACKNOWLEDGMENT

The authors wish to thank RSOFT for supplying OPTSIM for this work.

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Author biographies not included by author request due to space constraints.