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A pH sensor with a double-gate silicon nanowire field-effect transistor

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A pH sensor composed of a double-gate silicon nanowire field-effect transistor (DG Si-NW FET) is demonstrated. The proposed DG Si-NW FET allows the independent addressing of the gate voltage and hence improves the sensing capability through an application of asymmetric gate voltage between the two gates. One gate is a driving gate which controls the current flow, and the other is a supporting gate which amplifies the shift of the threshold voltage, which is a sensing metric, and which arises from changes in the pH. The pH signal is also amplified through modulation of the gate oxide thickness. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4793655]

pH sensors have been utilized in a wide range of applications, including support of basic research, monitoring environmental condition, manufacturing and processing of food, and monitoring chemical processes. Because control of the pH is essential in various chemical reactions, precise measurement of the pH is a stringent demand prior to pH control methods.

Glass electrodes are widely used to measure the pH.[1] A glass membrane that is permeable by H^+ ions is placed on a tip of the glass electrode. The pH can be measured by tracing the voltage which is produced in the glass membrane. Although pH glass electrodes measure the pH precisely and reliably, they are fragile and vulnerable to external stimuli. More seriously, it is very difficult to make them smaller and more compact, which inevitably imposes a constraint on their miniaturization, which is important when measuring the pH in a nano-system.

A pH sensor based on a field-effect transistor (FET) was demonstrated by the employment of the structure of an ion-sensitive field-effect transistor (ISFET), which is comprised of a solid-state source and drain, a silicon channel, and a liquid gate onto the gate dielectric. This prototype of an ISFET-based pH sensor was initially proposed by Bergveld to overcome the aforementioned weaknesses of pH sensors made of glass electrodes.[2,3] While commercialized conventional FETs are composed solely of a solid-state gate electrode, ISFETs utilize an ionic solution and a reference electrode submerged in the solution. The gate dielectric is exposed to the ionic solution, and the surface potential in the silicon channel is changed by the binding of H^+ ions onto the gate dielectric surface. The relationship between the surface potential (ψ_0) and the solution pH can be described using the combination of the site-binding (SB) theory and Gouy-Chapman-Stern (GCS) model,[4,5] which include properties of the gate dielectric and buffer solution. The pH sensitivity of the gate dielectric surface is given as

$$\frac{d\psi_0}{d\mathrm{pH}} = 2.303\alpha\frac{kT}{q},$$

where α is a dimensionless sensitivity parameter which varies between 0 and 1 depending on the intrinsic buffer capacitance of the gate dielectric and the ionic concentration of the buffer solution, k is Boltzmann's constant, T is the absolute temperature, and q is the elementary charge. When the sensitivity parameter (α) is approaching to unity, the gate dielectric surface shows maximum pH sensitivity at a value of 59.5 mV/pH at room temperature (300 K), which is known as the Nernst limit. It should be noted that a change of the surface potential results in a change of the threshold voltage (V_T). Thus, the pH is measured by monitoring the shift of V_T. ISFETs have inherent advantages of miniaturization, usefulness in multi-sensing applications, a rapid response, and a low cost stemming from the mature semiconductor fabrication technology.

Recently, there have been many attempts to amplify the signal caused by the pH change through structural modifications of FET devices. One modification led to the creation of a planar type of a dual-gate structure which is implemented on a silicon-on-insulator (SOI) substrate.[6–9] The planar type dual-gate FET is composed of two gates. One is a top gate, which is a reference electrode immersed in the solution. The other is a back gate (buried gate) which is positioned underneath the buried oxide of the SOI. The driving voltage which determines the FET characteristics is set through the reference electrode, and the surface potential produced by the pH is then amplified through the back gate. Although the pH sensitivity is limited by the properties of the gate dielectric, the surface potential produced on the gate dielectric is translated into V_T and amplified into a larger signal by means of the dual-gate structure.[6–9] The simple configuration without additional signal amplifier circuit is the distinctive feature of the dual-gate readout. Surprisingly, the dual-gate FET showed notable pH response which exceeded the Nernst limit. However, the FET has two weaknesses: (1) The reference electrode is difficult to be monolithically integrated on a chip; (2) individual addressing is not allowed due to the nature of the global back gate structure.

In this work, a double-gate silicon nanowire field-effect transistor (DG Si-NW FET) composed of two gates, which straddle both sidewalls of the Si-NW channel and face each

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other as they are on the coplanar buried oxide of the SOI substrate, is demonstrated for a pH sensor. As shown in Figures 1(a) and 1(b), individual addressing and monolithic integration are feasible due to the use of two local gates, which independently control the channel potential of the Si-NW.[10] Moreover, it is possible to construct an array configuration by virtue of the coplanar gate structure, and thus the Si-NW in the array can be selectively turned on or off. The monolithic integration, which is compatible with readout circuitry, is possible because the fabrication process of the DG Si-NW FET is very similar to that of the FinFET,[11] which has recently attracted a considerable amount of attention from major semiconductor industries as a next-generation FET.

The DG Si-NW FETs were fabricated with the recently reported top-down method.[12,13] A commercial SOI wafer was used (SOITEC, p-Si(100) with a resistivity of 8.5–11.5 Ω cm, a top silicon thickness of 55 nm, and a buried oxide thickness of 145 nm) as the starting material. First, a silicon nitride layer with a thickness of 80 nm was deposited by a low-pressure chemical vapor deposition (LPCVD) method. To create Si-NWs, the silicon nitride and silicon layers were patterned by deep ultraviolet (DUV) lithography (KrF stepper; wavelength of 248 nm), photoresist trimming, and sequential dry etching step. A tetraethylorthosilicate (TEOS) oxide layer with a thickness of 30 nm and an n^+ *in situ* doped polycrystalline silicon (poly-Si) layer with a thickness of 200 nm were sequentially deposited, which served as a gate dielectric and a gate electrode, respectively. To ensure that the separated gate (double-gate) electrodes straddled both sidewalls of the Si-NW, a chemical mechanical polishing (CMP) process was applied until the buried silicon nitride was revealed. The silicon nitride served as an etching stopper to protect the Si-NW from being etched during the CMP process. The thickness of the remaining silicon nitride on top of the Si-NW was reduced to 30 nm by the CMP process (to be stripped off later). After the patterning of the gate, the source and drain (S/D) were created by means of ion implantation (Arsenic, energy of 30 keV and a dose of $5 \times 10^{15}\,cm^{-2}$). Afterwards, a process of rapid thermal annealing (1000 °C, 5 s) was employed to activate the dopants. An inter-layer dielectric (ILD) oxide layer with a thickness of 200 nm was deposited by LPCVD for the electrical isolation between the metal interconnection lines and the bottom substrate. A sensing region to accommodate ionic solution was delineated by conventional lithography. Then, the ILD oxide was etched using a diluted HF solution until the silicon nitride layer on top of the Si-NW was exposed. This exposed silicon nitride layer was stripped out using hot phosphoric acid (150 °C, 20 min). Once again, the devices were oxidized at 700 °C for 30 min to grow a sensing oxide with a thickness of 3 nm on top of the Si-NW. This sensing oxide was served as an ion-sensitive layer for detecting H^+ ions and as a blocking layer for reducing the leakage current from the ionic solution to the Si-NW channel. The devices were annealed in a forming gas ambient (N_2:H_2 = 10:1) at 400 °C for 30 min to reduce the density of the interface states between the silicon dioxides and the Si-NW channel. Metal contacts were lithographically patterned and opened using a diluted HF solution, which etched the ILD oxide. Next, another lithography process was applied to pattern metal interconnection lines with a lift-off process. Chromium (Cr) with a thickness of 10 nm and gold (Au) with a thickness of a 200 nm was sequentially deposited by physical vapor deposition to fill the contact holes and create the interconnection lines. Except for the abovementioned sensing region, all other areas were then encapsulated with a passivation photoresist with a thickness of 3 μm for the electrical isolation of each metal interconnection line which connected the gates and the S/D. A polydimethylsiloxane (PDMS) reservoir to accommodate a volume of 50 μl was constructed and placed on the sensor surface to allow an ionic solution to be contained.

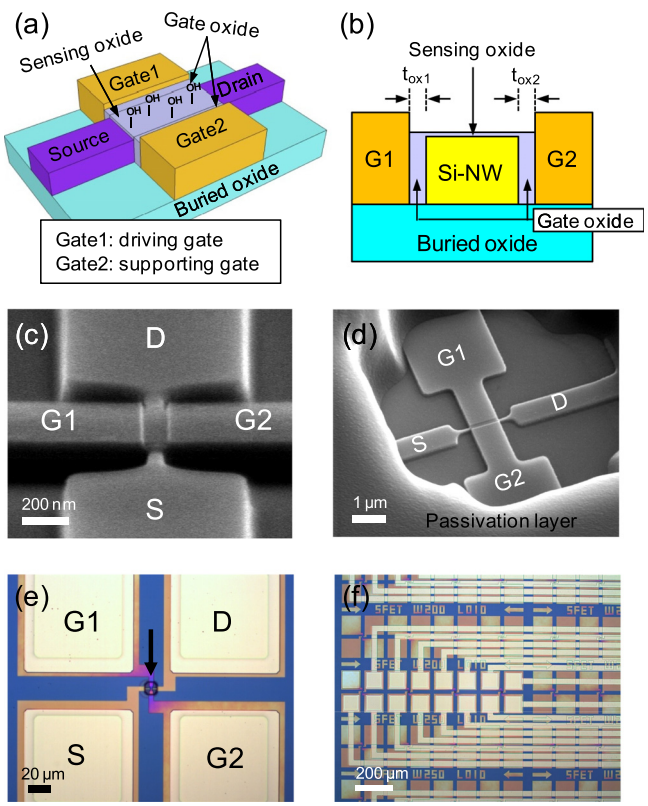

FIG. 1. Images of the fabricated device. (a) Schematic of the double-gate nanowire FET for pH sensing. A silicon nanowire is formed on a buried oxide. The current flowing from the drain (D) to the source (S) is controlled by the voltages applied to gate 1 and gate 2. The hydroxyl groups (−OH) of the sensing oxide react with H^+ ions in the solution and then generate the surface potential. Therefore, the V_T value of the FET is changed. (b) Cross-sectional schematic of the double-gate nanowire FET along the gate direction. (c) A magnified SEM image of the fabricated double-gate nanowire FET. The nanowire sidewall is covered by the two gates, and the top surface of the nanowire is opened in order to react with the ionic solution. (d) A SEM image of the fabricated device. The nanowire device is seen inside the passivation layer. The passivation layer is formed in order to protect the metal lines from the ionic solution and to block the leakage current. (e) A microscopic image of the fabricated device. The arrow indicates the area of (d). The remaining area is covered by the passivation layer. (f) A microscopic image of the fabricated devices in an array form. Two gates per nanowire are assigned, which lead to individual access and elaborate control capabilities. The metal lines are extended out for the electrical measurement.

The proposed DG Si-NW FET is composed of two gates: a driving and a supporting gate, which are positioned at the sidewalls of the Si-NW in order to control the current flowing in the Si-NW, as shown in Figures 1(a) and 1(b). Figures 1(c) and 1(d) show scanning electron microscopy (SEM) images of the fabricated DG Si-NW FET. The fabricated device has a nanowire width of 110 nm and the gate length of 1 μm. The

opened top surface of the Si-NW serves as a sensing site to detect H^+ ions in the solution. Figures 1(e) and 1(f) show a magnified microscopic image of a unit sensor device and an overall microscopic image of the sensor array, respectively. While a global gate such as a liquid gate or back gate is used in a conventional nanowire FET sensor, a local gate is implemented in the proposed DG Si-NW FET sensors to allow individual access to each sensor and to take advantage of the monolithic integration characteristic with readout and control circuitry on a coplanar surface of the chip.

By adding a 0.1M HCl or a 0.1M NaOH solution to a $0.1\times$ PBS buffer solution (pH 7.4), various solutions with different pH values were prepared. Before each pH sensing experiment, the devices were dipped into deionized water for 10 h to stabilize the surface of the sensing oxide.[8] A 50-μl drop of the pH testing solution was dropped into the PDMS reservoir using a micropipette. The electrical characteristics of the devices were measured using a semiconductor parameter analyzer (HP 4156C). Probing tips connected to the analyzer were contacted to metal pads which extended out from the PDMS reservoir. In order to measure the transfer characteristics, the drain current (I_D) was measured while the gate voltage (V_G) was swept at a constant drain voltage (V_D) of 50 mV.

As shown in Figures 2(c) and 2(d), the fabricated device shows n-type FET characteristics. As the pH value of the injected solution is increased, the I_D-V_G curve is shifted in parallel toward the right-hand side. In addition, V_T, which is a sensing metric, increases as a result. V_T is defined at the gate voltage necessary to produce a drain current of 1 nA. Because the amount of H^+ ions bound onto the sensing oxide is reduced with an increase in the pH value, the surface potential is lowered, leading to an increased value of V_T.

Because the DG Si-NW FET has the two symmetric gates, there are two methods to sweep the gate voltage. First, the two gates are electrically tied and swept together. This method is known as the double-gate (DG) mode, as shown in Figure 2(a). Second, one of the two gates (gate 1) is used to sweep the gate voltage as a driving gate while a constant voltage is applied to the other gate (gate 2), which is a supporting gate to tune the channel potential of the Si-NW near a side of gate 2. This method is termed the independent double-gate (IDG) mode, as shown in Figure 2(b). Because the two gates are identical, exchanging the driving gate and supporting gate leads to the same result. The pH sensitivity using the two methods was compared for various pH values. As shown in Figure 2(e), the IDG mode shows better pH response than the DG mode. It should be noted that the pH sensing response of the IDG mode is beyond the Nernst limit, which is an intrinsic limit of a conventional pH sensor, with a value of 59 mV/pH at room temperature (300 K). Herein, the effect of the supporting gate on the amplification of the pH response was

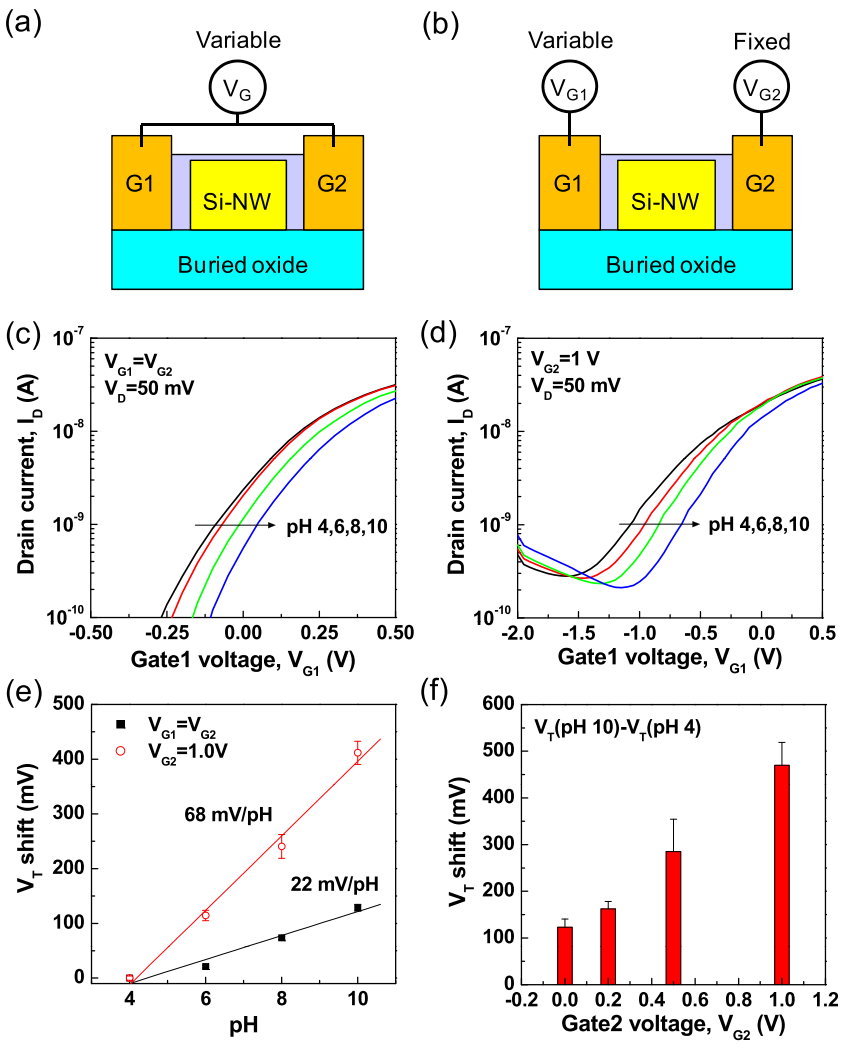

FIG. 2. Dependence of the pH response on the gate bias conditions. (a) Schematic showing the DG mode. Gate 1 and gate 2 are swept at the same voltage. (b) Schematic showing the IDG mode. Gate 1 is swept and a fixed voltage is applied to gate 2. (c) I_D-V_G characteristics according to various pH values under the DG mode. (d) I_D-V_G characteristics according to various pH values under the IDG mode. (e) The V_T shift versus pH. The two methods (DG and IDG modes) are compared. (f) Dependence of the V_T shift on the voltage of gate 2. After a constant voltage is applied to gate 2, the change in the value of V_T is measured while the pH value of the solution is changed from 4 to 10. This experiment is repeated with various conditions of gate 2.

further investigated. Various amounts of voltages were applied to the supporting gate, and the pH response was then measured. The pH response was defined as the amount of V_T shift when the pH in the injected solution was varied from pH 4 to pH 10. Figure 2(f) shows that the pH response is enhanced as the voltage applied to the supporting gate (gate 2) is increased. Under the IDG mode, there are two channel surfaces; one (surface 1) is close to gate 1 and the other (surface 2) is close to gate 2. As the voltage applied to gate 2 increases, a larger amount of current flows onto surface 2 while a relatively small current flows onto surface 1. This result implies that the current controllability of gate 1 is weakened; hence, higher voltage is needed to restore the current change arising from the H^+ ions. Therefore, the V_T shift due to the pH change is amplified as the voltage of gate 2 is increased. This is the major principle which allows the device to exceed the aforementioned Nernst limit.

To investigate the dependence of the gate oxide thickness on the pH response, two devices with different gate oxide thicknesses of 5 nm and 30 nm were prepared. As shown in Figure 3(a), the pH response is enhanced as the gate oxide thickness is increased. This experimental result is consistent with the simulated data acquired using a semiconductor device simulator.[14] As the gate oxide thickness is increased, the current controllability of the driving gate is reduced due to the lowered gate capacitance. As a result, a higher voltage should be applied to the driving gate to restore the current change stemming from the H^+ ions; thus, the V_T shift is increased.

In this work, the gate oxide thicknesses of gate 1 and gate 2 (t_{ox1} and t_{ox2}) of the fabricated devices are identical. However, asymmetric gate oxides ($t_{ox1} \neq t_{ox2}$) can be fabricated by slightly changing the fabrication step during the formation of the gate oxide.[15] The effects of asymmetric gate oxides on the pH sensitivity were investigated by means of the semiconductor device simulation. During the simulation, the potential generated by H^+ ions bound on the sensing oxide was modeled by setting the charges on the sensing oxide. The V_T shift under the condition of the DG mode ($V_{G1} = V_{G2}$) is plotted in Figure 3(b). Because gate 1 and gate 2 are identical due to the same voltage levels, the plotted graph is symmetric with respect to the condition of $t_{ox1} = t_{ox2}$. The response is increased when either t_{ox1} or t_{ox2} is increased. Figure 3(c) shows the V_T shift under the condition of the IDG mode, i.e., when V_{G1} (voltage of gate 1) is swept and when V_{G2} (voltage of gate 2) is fixed at different voltages. Similar to the DG mode ($V_{G1} = V_{G2}$), the response is enhanced as t_{ox1} is increased. In contrast, a reduced value of t_{ox2} leads to an increase in the response (V_T shift), although the influence of the modulation of t_{ox2} on the shift of V_T is less than that when t_{ox1} is modulated. In order to maximize the pH response, thicker t_{ox1} and thinner t_{ox2} layers are preferred. In other words, the driving gate (gate 1) with an increased value of t_{ox1} can effectively amplify the signal by increasing the capacitance of the supporting gate (gate 2) with a reduced value of t_{ox2}. Based on the simulation results, the pH response of the proposed sensor can be enhanced even more by the proper scaling of the gate oxide thickness.

The signal drift is the common effect of the FET-based pH sensors to degrade the long-term stability. Some possible

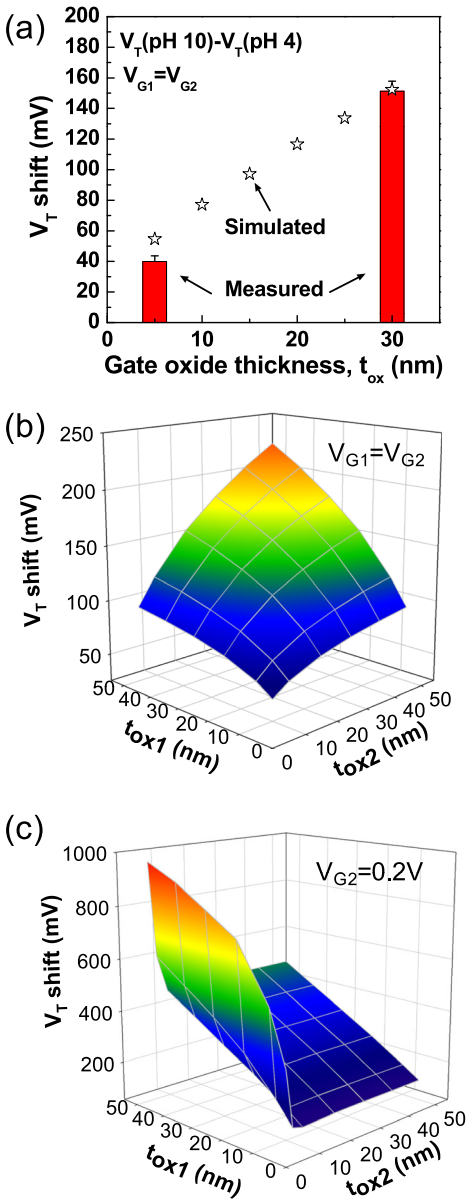

FIG. 3. Dependence of the pH response on the gate oxide thicknesses. (a) Dependence of the V_T shift on the gate oxide thickness. Two different thicknesses of the gate oxide which forms on the nanowire sidewall are used: 5 nm and 30 nm. The measured data are fitted with simulation data using a semiconductor device simulator. (b) Simulated result of the V_T shift depending on the oxide thicknesses of gate 1 and gate 2 under the DG mode ($V_{G1} = V_{G2}$). (c) Simulated result of the V_T shift depending on the oxide thicknesses of gate 1 and gate 2 under the IDG mode in which gate 1 is swept and a fixed voltage is applied to gate 2. In all simulations, the V_T shift is extracted after a test charge of -1×10^{11} cm^{-2} is set on the top surface of the nanowire. The test charge is obtained by fitting with measured data in (a).

reasons of the drift include variation of the surface state density at the interface between the channel and dielectric due to the ionic diffusion and the hydration of the dielectric surface.[16] The measured value of the drift in the proposed sensor is 27 mV/h, which is comparable to that of other nanowire-based pH sensors.[17] The long-term stability can be improved with optimization of the sensing oxide material. The SiO_2 used in this work is not the best material for the long-term stability due to high diffusivity of ions and easy hydration of the surface. By replacing the SiO_2 with the Si_3N_4 and Al_2O_3 as the sensing oxide, the drift can be suppressed, and the

stability can be improved because those materials are barriers against ionic diffusion and show high resistance to hydration of the surface compared to the SiO_2.[18]

In conclusion, double-gate silicon nanowire FETs were fabricated, and their pH sensing capabilities were investigated. The threshold voltage of the proposed sensor was shifted according to the pH value of a test solution. As the voltage of gate 2 (the supporting gate) was increased through asymmetric biasing between the driving and supporting gate, the pH response was amplified far beyond the Nernst limit. The pH response was also increased by asymmetrically changing the gate oxide thickness between the driving and supporting gate. The proposed double-gate nanowire FETs using local gates show great potential for simultaneous detections of chemical and/or biological species by virtue of the individual control of each sensor. This sensor system can be realized in a single integrated chip using mature semiconductor fabrication technology for a low-cost and rapid analysis. Therefore, a handheld POCT system may be feasible.

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