A 1.9-GHz Triple-Mode Class-E Power Amplifier for a Polar Transmitter

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***Abstract*—A 1.9-GHz CMOS power amplifier for polar transmitters was implemented with a 0.25-μm radio frequency CMOS process. All the matching components, including the input and output transformers, were fully integrated. The concepts of mode locking and adaptive load were applied in order to increase the efficiency and dynamic range of the amplifier. The amplifier achieved a drain efficiency of 33% at a maximum output power of 28 dBm. The measured dynamic range was 34 dB for a supply voltage that ranged from 0.7 to 3.3 V. The measured improvement of the low power efficiency was 140% at an output power of 16 dBm.**

***Index Terms*—Adaptive load, class-E, dynamic range, GSM, mode locking, polar transmitter.**

I. Introduction

RECENTLY, CMOS power amplifiers (PAs) have been studied assiduously, though few works have focused on CMOS PAs for polar transmitter applications. Polar transmitters are expected to be the next-generation transmitters.

An I–Q to R-θ transformer can decompose the radio frequency (RF) input of a PA for polar transmitters into a low-frequency envelope and RF phase signals. One of the input signals of the PA is the RF phase signal, the amplitude of which is constant. The other input signal, which has envelope information, is entered into a supply voltage, $V_{\rm DD}$, of the PA through a dc–dc converter. Because of the fixed power of RF phase signals, polar transmitters can use switching-mode PAs, such as class-E amplifiers, which are nonlinear but very efficient.

Two important specifications for PAs are used in polar transmitters. The first specification is the output dynamic range. In polar transmitter systems, the range of variable $V_{\rm DD}$ values determines the dynamic range of a PA. It is crucial, therefore, to determine how to get enough dynamic range in a PA for a given $V_{\rm DD}$ range in polar transmitter systems. The second specification is the level of efficiency at the low output power region. Hence, we propose an adaptive load technique as a means of increasing the dynamic range of PAs and improving their efficiency.

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II. Load Impedance Transformation

A. Dynamic Range of Class-E PAs

The relation between the parameters $R_{\rm LOAD}$ and $P_{\rm OUT}$ of a conventional class-E PA can be shown as

$$P_{\rm OUT} \propto \frac{V_{\rm DD}^2}{R_{\rm LOAD}}. \tag{1}$$

To get a high maximum output power, $P_{\rm OUT}$, we must ensure a decrease in the load impedance, $R_{\rm LOAD}$, at a high $V_{\rm DD}$ value. The dynamic range of a PA is the difference between the maximum $P_{\rm OUT}$ and the minimum $P_{\rm OUT}$ as

$$\begin{aligned}\text{Dynamic range} &= 10\log\frac{\left(\frac{V_{\rm DD\,max}^2}{R_L}\right)}{\left(\frac{V_{\rm DD\,min}^2}{R_H}\right)} \\ &= 20\log\frac{V_{\rm DD\,max}}{V_{\rm DD\,min}} + 10\log\frac{R_H}{R_L}. \end{aligned}\tag{2}$$

In (2), the parameter $V_{\rm DD\,max}$ is the maximum $V_{\rm DD}$, $V_{\rm DDmin}$ is the minimum $V_{\rm DD}$, R_L is the low $R_{\rm LOAD}$, and R_H is the high $R_{\rm LOAD}$. Assuming the values of 3.3 V for $V_{\rm DDmax}$, 0.7 V for $V_{\rm DDmin}$ and 3 Ω for R_L, we calculated that a value of 5 was the required load impedance ratio, R_H/R_L, when the dynamic range of a GSM system is 20 dB. If the $R_{\rm LOAD}$ does not change, we can get a dynamic range of 20 dB with a voltage of 0.33 V for $V_{\rm DDmin}$ and 3.3 V for $V_{\rm DDmax}$. However, a very low $V_{\rm DD}$ produces many expected difficulties, such as feed through and phase distortion.

B. Efficiency of Class-E PAs

To ensure the maximum output power in a PA reaches a high level, we need a very low level of $R_{\rm LOAD}$. However, for the low power mode, we must increase the $R_{\rm LOAD}$ of a PA in order to achieve a high level of efficiency. As shown in the following equation, if load $R_{\rm LOAD}$ increases below a certain point of the $V_{\rm DD}$, we can increase the efficiency under low output power

$$\text{Efficiency} \propto \frac{R_{\rm LOAD}}{R_{\rm ON} + R_{\rm LOAD}} \tag{3}$$

where $R_{\rm ON}$ is the on-resistance of the power transistors. Thus, to simultaneously get a high maximum $P_{\rm OUT}$ at the high power mode and a high level of efficiency at the low power mode, we need an adaptive load technique.

III. Design of the 1.9-GHz CMOS PA

A. Proposed Adaptive Load PA

Fig. 1 shows a block diagram of the proposed PA. Because the output load is shared by the first driver, the second driver and

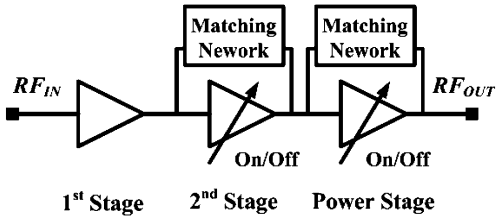

Fig. 1. Block diagram of the proposed adaptive load PA.

the power stage through matching networks, the power from the three stages is combined and transmitted into the output load. For example, if the power stage is turned off, the output power of the first and second stages becomes the output power of the PA, which is the medium power mode.

Fig. 2 shows a simplified schematic of the proposed PA. By applying a differential structure to our PA, we obtained a virtual ground. We also used a high-Q transmission line transformer as the output transformer because it has a direct influence on the output power and on the efficiency of the PAs [1], [2]. The simulated loss of the transformer for the PA is about 0.7 dB. To enable the amplifier to endure the high drain voltages, we used a cascode structure [3]. The PMOSs are used as switches, S1 and S2, to switch the second driver and power stages. The gate of M12 is connected by resistor to the $V_{\rm DD}$. The drain of S1 is connected to the gate of M22. The drain of S2 is connected to the gate of M32. For the high power mode, $V_{\rm CTRL}$ 1 and $V_{\rm CTRL}$ 2 must be zero voltage. For the medium power mode, $V_{\rm CTRL}$ 2 must be 3.3 V in order to turn off S2 and the power stage. The gate lengths are 0.35 μm for the common-gate NMOS and 0.25 μm for the common-source NMOS.

Fig. 3 shows the simplified matching network of the PA. In Fig. 3 the L_A parameter can be designed and implemented with a spiral inductor or a transmission line. The shunt capacitance, C_A, can be composed of the parasitic drain-source capacitance of the driver stage, the parasitic gate-source capacitance of the power stage and an additional MIM capacitor. With these parameters, as shown in Fig. 3(b), the output impedance is transformed to the high load impedance of the driver stage. Furthermore, as mentioned in Section II, the efficiency and the dynamic range can be increased due to the high load impedances of the second driver stage and the first driver stage. For the low power mode, we need to use S1 and S2 to turn off the power stage and the second driver stage. The proposed PA has no additional switches on the signal path for changing the operational mode. The only way to change the mode of the PA is to turn the power stage or the second driver stage off and on. Thus, our adaptive load PA suffers no power loss from additional switches. We also applied a mode-locking technique [4], [5]. With L_A, L_B, C_A, and C_B, the matching network enables the amplifier to operate as a class-E amplifier [1].

B. Self-Biased Cascode Structure

Theoretically, as shown in (2), the dynamic range of a cascode class-E PA is 13.5 dB for a $V_{\rm DD}$ range of 0.7 to 3.3 V with a fixed $R_{\rm LOAD}$. To ensure the PA can get a higher dynamic range than that, we bound the gate voltages of M12, M22, and M32 to $V_{\rm DD}$ through S1, S2 and the resistor, respectively, as shown in Fig. 2.

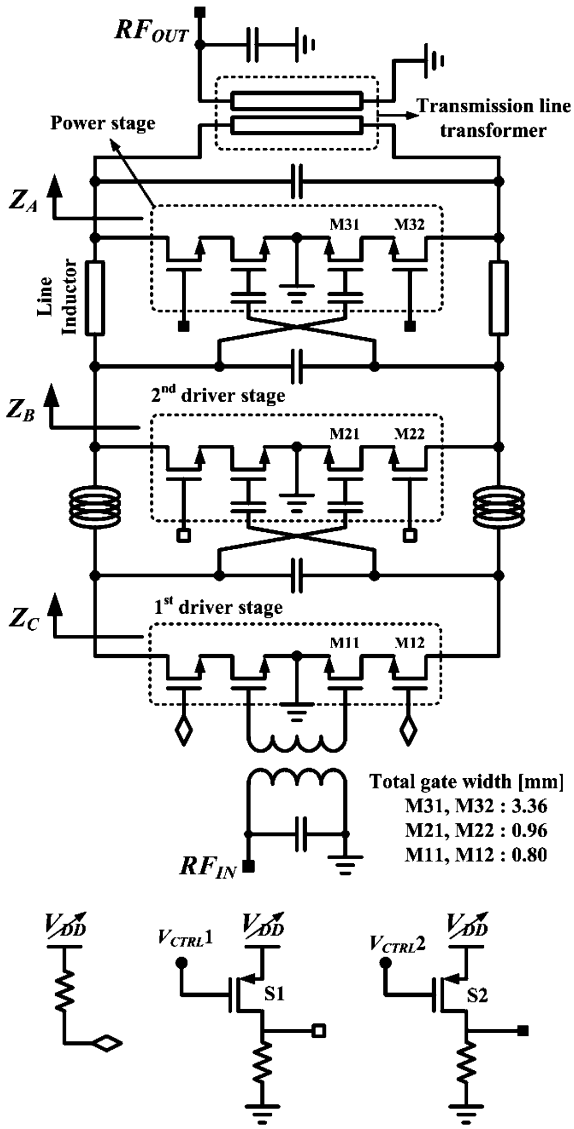

Fig. 2. Simplified schematic of the proposed adaptive load PA.

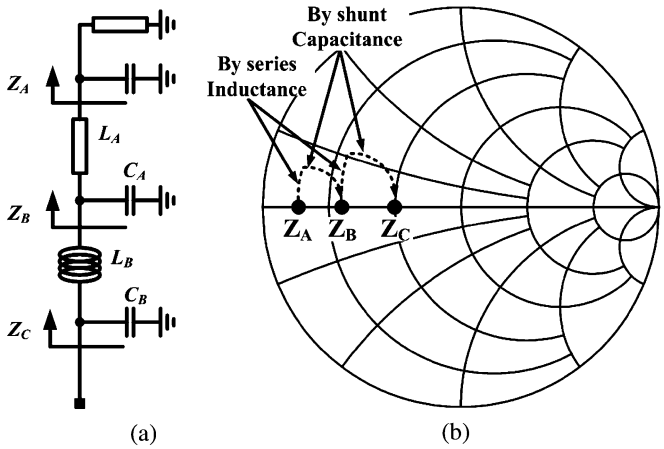

Fig. 3. (a) Simplified equivalent matching circuit and (b) contour of the load impedance transformation.

When $V_{\rm DD}$ decreases, the gate voltages of M12, M22, and M32 also decrease and the $R_{\rm ON}$ value of the power stage increases.

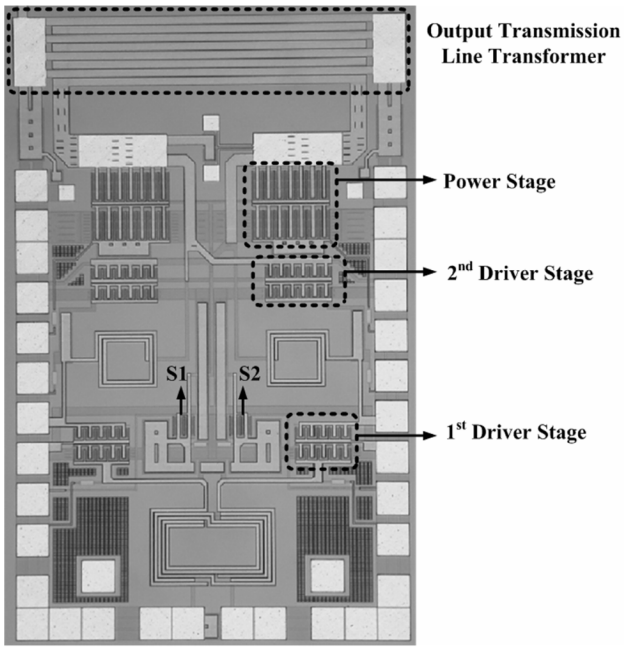

Fig. 4. Photograph of the chip in the proposed adaptive load PA.

Because the P_{OUT} value of the PA is in inverse proportion to R_{ON}, the dynamic range of the PA increases.

C. Auto-Switching Method

The auto-switching method is used in the PA to automatically change the output power mode in relation to the V_{DD} level. In the polar transmitter, the output power mode can change as it senses the V_{DD} level because the P_{OUT} value is determined by the V_{DD} level. We use S1 and S2 as an auto-switching circuit. For example, if V_{CTRL} 2 is fixed at 2 V while V_{DD} varies, the power stage turns off when V_{DD} decreases to less than $2\,V + V_{\mathrm{TH}}$. The V_{TH} parameter is the threshold voltage of S1 and S2. The levels of V_{CTRL} 1 and V_{CTRL} 2 determine the points of V_{DD} whenever the output power modes are changed.

IV. Measurement Results

Fig. 4 shows a photograph of the implemented chip. The size of the chip is 1.2 mm × 1.8 mm, including all of the pads. Fig. 5 shows the measured drain efficiency versus the output power of the PA when V_{DD} varied from 0.7 to 3.3 V. The power of $\mathrm{RF_{IN}}$ was fixed at 10 dBm because the PA was designed for polar transmitters. First, we measured the data of the high power mode when all of the power stages and driver stages were turned on. Second, when only the first driver stage and the second driver stage were turned on, we measured the data of the medium power mode. Third, we measured the data of the low power mode when only the first driver stage was turned on. Finally, we measured the data of the auto-switching mode when S1 and S2 were used as an auto-switching circuit that responded to the V_{DD} level. As shown in Fig. 5, the output power modes changed automatically in relation to the V_{DD} level. The maximum output power was 28 dBm, and the drain efficiency at the maximum output power was about 33%. The dynamic range of the PA was about 34 dB. By using the adaptive load technique, we improved the low power efficiency by 140% at an output power of 16 dBm. The flatness of the output power was 0.25 dB for an operating frequency that ranged from 1.7 to 1.9 GHz.

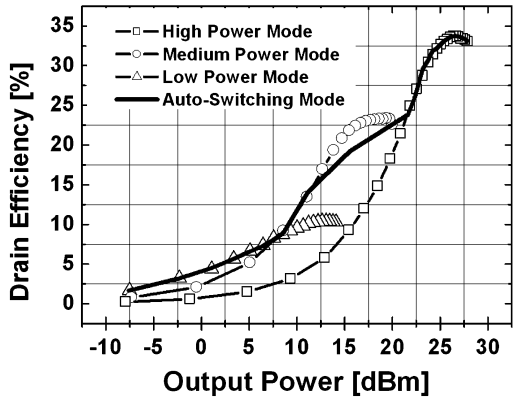

Fig. 5. Drain efficiency versus the output power of the high power mode, the medium power mode and the low power mode.

V. Conclusion

Using 0.25-μm RF CMOS technology, we designed a 1.9-GHz RF PA for polar transmitter applications. We improved the dynamic range by about 20.5 dB as a result of applying both the self-biased cascode structure and the adaptive load method. The total dynamic range was about 34 dB. Moreover, the low power efficiency improvement of the proposed adaptive load PA was 140% at an output power of 16 dBm.

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