A 1.9-GHz CMOS Power Amplifier Using Three-Port Asymmetric Transmission Line Transformer for a Polar Transmitter

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***Abstract*—A 1.9-GHz CMOS differential power amplifier for a polar transmitter is implemented with a 0.18-μm RF CMOS process. All of the matching components, including the input and output transformers, are fully integrated. The concepts of injection locking and variable load are applied to increase the efficiency and dynamic range of the amplifier. An asymmetric three-port transmission line transformer is proposed to embody the variable load effectively. The power amplifier achieved a power-added efficiency of 40% at a maximum output power of 32 dBm. The dynamic range was 20 dB at supply voltages ranging from 0.5 to 3.3 V. The improvement of the low power efficiency was 290% at an output power of 16 dBm.**

***Index Terms*—Class-E, CMOS, dynamic range, global system for mobile communication (GSM), injection locking, polar transmitter, power amplifier, transmission line transformer, variable load.**

I. Introduction

POLAR transmitters are expected to be very popular owing to their many advantages over conventional Cartesian transmitters, especially in global system for mobile communications (GSM) and EDGE systems. Accordingly, their power amplifiers based on GaAs HBTs are being studied intensively. However, few studies have focused on CMOS power amplifiers for polar transmitters. Although CMOS power amplifiers are expected to be cheaper than GaAs HBT power amplifiers and easier to integrate with other circuits, they are not considered to be a useful RF power amplifier with a watt-level output power. Recently, the potential of a CMOS power amplifier was successfully demonstrated using a distributed active transformer [1]–[3]. The distributed active transformer is considered to have the potential to lend improvements to the performance of a CMOS power amplifier [4]. In this study, the concept of the distributed active transformer is used to design a CMOS power amplifier for polar transmitter applications.

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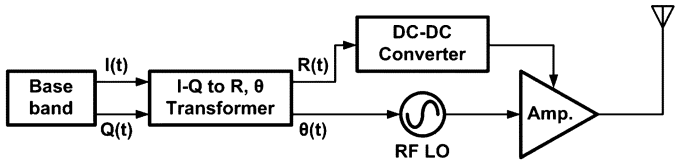


Fig. 1. Simplified block diagram of a polar transmitter.

Fig. 1 shows a block diagram of a polar transmitter. The polar transformer (I-Q to R-θ) decomposes the input of a power amplifier into two types of input signals. The first of these is an RF phase signal, which is applied to the input of a power amplifier, and the second is an envelope signal, applied as a supply voltage (V_{DD}). The supply voltage has to be applied through a dc–dc converter or a low drop output regulator circuit in order to supply sufficient power. Polar transmitters can use switching-mode power amplifiers, as the input signals do not contain envelope information. These include class-D, class-E, and class-F amplifiers, which are nonlinear, but very efficient. A CMOS power transistor is known to be viable for switching power amplifiers rather than linear amplifiers; thus, it common to study CMOS switching power amplifiers for polar transmitters [1]–[3], [5]. There are two important specifications of power amplifiers for polar transmitters. The first is the output dynamic range. It is crucial to obtain enough dynamic range with a given supply voltage range. The second specification is related to efficiency at a low output power. In general, a power efficiency close to the maximum output power is fairly high. However, the efficiency at a low output power is very low. Therefore, a stage-convertible power amplifier using a variable load method [6] is proposed as a means of increasing the dynamic range of the power amplifiers and improving the efficiency at a low output power. An asymmetric three-port transmission line transformer is also proposed to embody the variable load method efficiently.

II. Load Impedance Transformation

A. Power Efficiency of Class-E Power Amplifiers

Polar transmitters can use switching-mode power amplifiers, as mentioned in Section I. The power efficiencies of polar transmitters are, therefore, expected to be higher than those of conventional transmitters; however, in a general switching mode, power amplifiers require a driving power greater than that for linear amplifiers. In a conventional class-E power amplifier, the

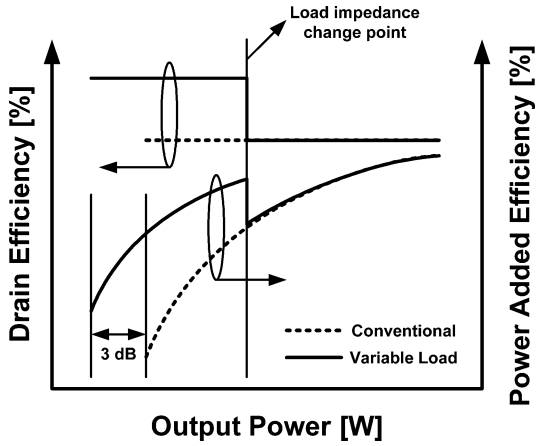


Fig. 2. Drain efficiency and PAE of a conventional and a variable load power amplifier.

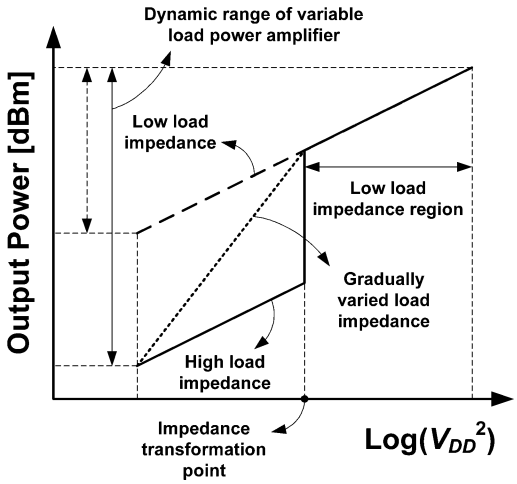


Fig. 3. Dynamic range of a power amplifier with a variable load.

power consumption of the driver stage degrades the overall efficiency severely regardless of the high drain efficiency of the power amplifier.

As the output power of a conventional class-E power amplifier is in proportion to V_{DD}^2 with a fixed input power, as shown by

$$P_{\mathrm{OUT}}(W) \propto \frac{V_{DD}^2}{R_{\mathrm{load}}} \tag{1}$$

the gain is decreased severely at a low V_{DD} [7]. Although the drain efficiency maintains a high value, the power-added efficiency (PAE) of the power amplifier is degraded as the V_{DD} decreases. The drain efficiency and PAE of a power amplifier are expressed as follows:

$$\text{Drain Efficiency} \propto \frac{R_{\mathrm{load}}}{R_{\mathrm{on}} + R_{\mathrm{load}}} \tag{2}$$

$$\mathrm{PAE} \propto \frac{R_{\mathrm{load}}}{R_{\mathrm{on}} + R_{\mathrm{load}}} \cdot \left(1 - \frac{P_{\mathrm{IN}}(W)}{P_{\mathrm{OUT}}(W)}\right) \tag{3}$$

where P_{IN} is the input power, P_{OUT} is the output power, R_{on} is the on resistance of the power transistors, and R_{load} is the load impedance of the power amplifier. Fig. 2 shows the drain efficiency and PAE versus the P_{OUT} of a conventional power amplifier, and a variable load power amplifier when the V_{DD} varies with a fixed P_{IN}. As the output power is in proportion to V_{DD}^2, as shown in (1), the drain efficiency and PAE versus P_{OUT} can be determined, as shown in Fig. 2. The dotted lines denote the drain efficiency and PAE of a conventional power amplifier. If the low load impedance is increased two times in the low output power region, the drain efficiency and PAE are increased according to (2) and (3), respectively. The drain efficiency and PAE curves with variable loads appear as solid lines in Fig. 2.

Although a low load impedance is required to obtain high maximum output power, the load impedance must be increased as V_{DD} is decreased in order to increase the efficiency. The variable load allows a high maximum output power at high power and a high efficiency at low power.

B. Dynamic Range of Class-E Power Amplifiers

The dynamic range of a power amplifier is the difference between the maximum output power and the minimum output power. As the load impedance of a conventional class-E power amplifier is fixed, the dynamic range of the conventional power amplifier for polar transmitters is determined by the variable range of V_{DD}. To satisfy the dynamic range of a GSM system, i.e., 20 dB, the minimum supply voltage must be as low as 0.33 V with a maximum supply voltage of 3.3 V. However, 0.33 V is too low to generate with a dc–dc converter. Additionally, such a low supply voltage degrades the overall efficiency of a dc–dc converter. Moreover, the phase distortion and the feed-through of the power amplifier are significant issues under a low supply voltage [8].

To solve these problems, a variable load method can be applied to the power amplifier for a polar transmitter. As the output power is in proportion to V_{DD}^2, the output power is decreased as V_{DD} is decreased. If the load impedance is increased at a low V_{DD} region, the dynamic range can be increased, as shown by

$$\begin{aligned}\text{Dynamic range} &= P_{\mathrm{OUT\,max}}(\mathrm{dBm}) - P_{\mathrm{OUT\,min}}(\mathrm{dBm}) \\ &= 10\log\frac{\left(\frac{V_{DD_{\max}}^2}{R_L}\right)}{\left(\frac{V_{DD_{\min}}^2}{R_H}\right)} \\ &= 20\log\frac{V_{DD_{\max}}}{V_{DD_{\min}}} + 10\log\frac{R_H}{R_L} \\ &= 20\log\frac{3.3}{0.7} + 10\log\frac{15}{3} \\ &\cong 20.5\ \mathrm{dB}.\end{aligned} \tag{4}$$

In this equation, the parameter $V_{DD\max}$ is the maximum V_{DD}, $V_{DD\min}$ is the minimum V_{DD}, R_L is the low load impedance for the high output power, and R_H is the high load impedance for the low output power. As shown in (4), the dynamic range can be controlled by not only the range of variable V_{DD}, but also through the ratio between R_L and R_H. Assuming the values of 3.3 V for $V_{DD\max}$, 0.7 V for $V_{DD\min}$, and 3 Ω for R_L, the required load impedance ratio R_H/R_L should be 5 for the dynamic range of a GSM system.

Fig. 3 explains (4). At a certain point of V_{DD}, the load impedance R_{load} changes from low to high. As P_{OUT} versus V_{DD}^2 decreases as R_{load} increases, as shown in (1), the dynamic

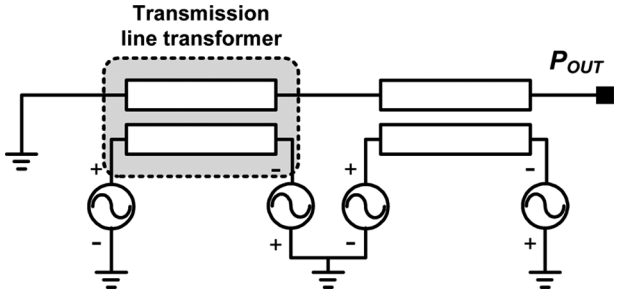


Fig. 4. Simplified schematic of the output transformer (after [1] and [2]).

range increases for a given range of V_{DD}. In Fig. 3, the dashed line shows $P_{\rm OUT}$ of a conventional power amplifier. The solid line in this figure shows $P_{\rm OUT}$ of a power amplifier with an abruptly varied load, and the dotted line shows $P_{\rm OUT}$ of a power amplifier with a gradually varied load. The dotted arrow shows the dynamic range of a conventional power amplifier and the solid arrow shows the dynamic range of a power amplifier with a variable load. It is important to note that the dynamic range can be extended using the variable load method.

III. Proposed Three-Port Asymmetric Transmission Line Transformer

A. Impedance Transformation

In contrast to GaAs technology, there is no via process in CMOS technology. Thus, a bond wire is needed to make an ac ground in RF CMOS circuits. By applying a differential structure, it is possible to obtain virtual grounds, thereby preventing the gain reductions that are induced by the bond wires.

However, in general, the antenna and filter connected to the output of the power amplifier are single-ended components. Thus, a transformer is needed to connect the differential power amplifier to the single-ended components. In this study, a high-Q transmission line transformer is used as the output transformer. The transformer significantly influences the output power and efficiency. The output matching is completed with an additional metal–insulator–metal (MIM) capacitor. Two differential pairs of a power stage are used, as shown in Fig. 4.

If the k-factor of the transformer used in Fig. 4 is 1, as is ideal, and there is no parasitic inductance in the transmission line transformer, the load impedance of 50 Ω is transformed into 12.5 Ω with an impedance transforming ratio of 1 to 4 [1], [2]. However, the inductance of the transmission line transformer plays an important role in the output matching network. To verify the role of the transmission line transformer in the output matching network, Fig. 5 shows an equivalent circuit for the output matching network, which is composed of the transmission line transformer and additional MIM capacitors C and $C_{\rm shunt}$. To simplify the analysis, the turn ratio of the transmission line transformer, which is used in the analysis, is 1, as shown in Fig. 5(a).

Fig. 5(b) shows the equivalent circuit of the output matching network shown in Fig. 5(a). L_1 and L_2 are the self-inductances. The parasitic inductances of the transmission line transformer,

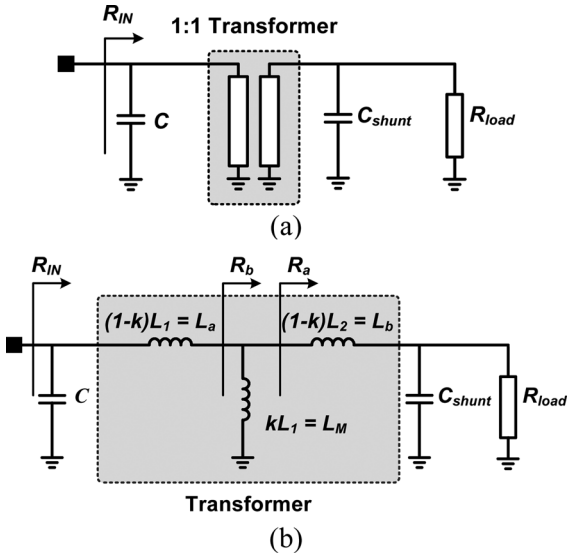


Fig. 5. (a) Output matching network. (b) Equivalent circuit for the output matching network.

e.g., L_a, L_b, and L_M in Fig. 5(b), can be used as output matching components. The following equations demonstrate the process of impedance transformation using the transmission line transformer and the additional capacitors, C and $C_{\rm shunt}$. R_a of Fig. 5 can be calculated as follows:

$$R_a = \frac{R_{\rm load}}{1+(\omega R_{\rm load}C_{\rm shunt})^2} + j\omega \cdot \frac{L_b + \omega^2 R_{\rm load}^2 L_b C_{\rm shunt}^2 - R_{\rm load}^2 C_{\rm shunt}}{1+(\omega R_{\rm load}C_{\rm shunt})^2}. \quad (5)$$

The imaginary part of (5) is equal to zero at resonance with L_b and $C_{\rm shunt}$, as described in

$$L_b + \omega^2 R_{\rm load}^2 L_b C_{\rm shunt}^2 - R_{\rm load}^2 C_{\rm shunt} = 0. \quad (6)$$

Here, L_b is expressed by

$$L_b = \frac{R_{\rm load}^2 C_{\rm shunt}}{1+(\omega R_{\rm load}C_{\rm shunt})^2}. \quad (7)$$

R_b and $R_{\rm IN}$ are calculated by

$$R_b = \frac{j\omega R_a L_M}{R_a + j\omega L_M} = \frac{\omega^2 R_a L_M^2}{R_a^2+\omega^2 L_M^2} + j\omega \cdot \frac{R_a^2 L_M}{R_a^2+\omega^2 L_M^2} \quad (8)$$

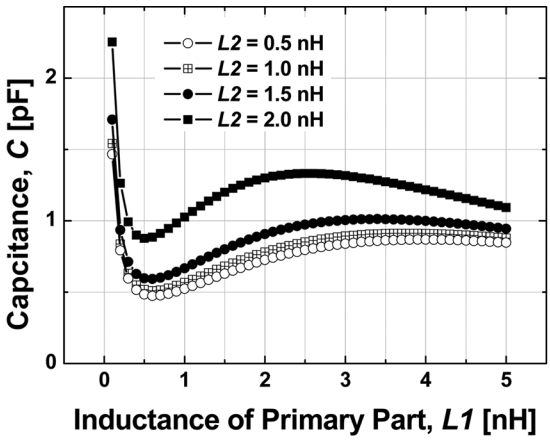
$$R_{\rm IN} = \frac{\omega^2 R_a L_M^2 + jA}{R_a^2\left\{1-\omega^2 C(L_a+L_M)\right\}^2 + \omega^2 L_M^2(1-\omega^2 L_a C)^2}. \quad (9)$$

Afterwards, the imaginary part of (9) can be equal to zero using the value C from Fig. 5, as described in

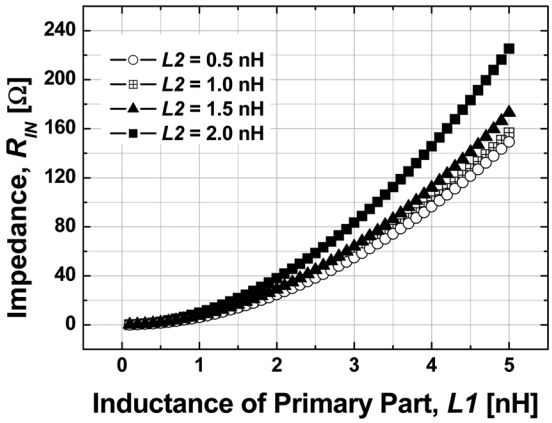
$$A = \omega^3 L_a L_M^2 + \omega R_a^2(L_a+L_M) - C\left\{\omega^5 L_a^2 L_M^2 + \omega^3 (L_a+L_M)^2 R_a^2\right\} = 0. \quad (10)$$

Following this, the value C can be expressed as

$$\therefore C = \frac{\omega^3 L_a L_M^2 + R_a^2(L_a+L_M)}{\omega^4 L_a^2 L_M^2 + \omega^2 (L_a+L_M)^2 R_a^2}. \quad (11)$$



(a)



(b)

Fig. 6. Simulation results of: (a) the capacitance C and (b) the transformed load impedance $R_{\rm IN}$.

$R_{\rm IN}$ can, therefore, be expressed by

$$R_{\rm IN} = \frac{\omega^2 R_a L_M^2}{R_a^2 \left\{1 - \omega^2 C(L_a + L_M)\right\}^2 + \omega^2 L_M^2 (1 - \omega^2 L_a C)^2}. \tag{12}$$

Assuming the k-factor is 0.5 and $R_{\rm load}$ is 25 Ω, the transformed load impedance $R_{\rm IN}$ versus the varied inductance of the primary part was simulated using (12). The inductance of the secondary part L_2 is assumed to be 0.5, 1.0, 1.5, and 2.0 nH in the simulation. Fig. 6 shows simulated C and $R_{\rm IN}$. As shown in Fig. 6(b), $R_{\rm IN}$ increases as L_1 increases. Thus, although the impedance transformation ratio of the ideal transformer is 1, the impedance transformation ratio of the transmission line transformer can be controlled by the parasitic component of the transformer. From the results shown in Fig. 6, the inductance of the primary part must be small in order to obtain the low load impedance for a high maximum output power. As shown in Section II, the inductance of the primary part must be large in order to obtain a high load impedance for a high dynamic range and a high efficiency at the low output power region.

It is interesting to note that, for a high load impedance, the k-factor of the transmission line transformer does not increase as the inductance L_1 increases. If the k-factor increases with an increase of L_1, $R_{\rm IN}$ cannot be increased effectively as L_1 increases.

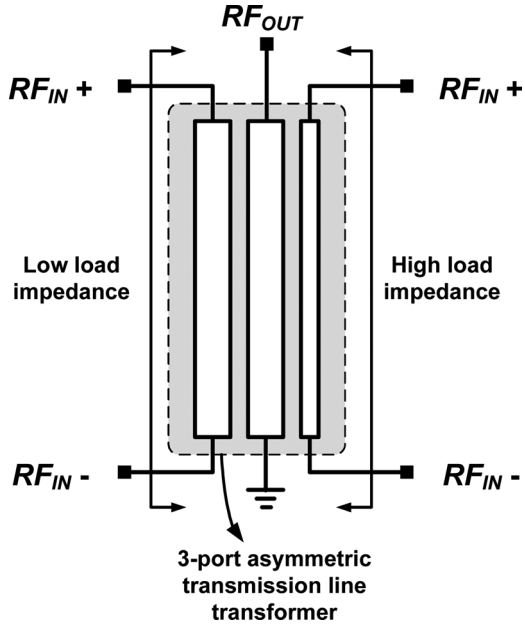


Fig. 7. Simplified schematic of the proposed three-port asymmetric transmission line transformer.

B. Implementation of a Three-Port Asymmetric Transmission Line Transformer

A three-port transmission line transformer is proposed in order to obtain a low and high load impedance with a transformer, as simplified in Fig. 7. The primary part of the transformer consists of two transmission lines, which have different inductances. The inductances can be controlled by the length and width of the slab waveguides. One of these is designed for a low load impedance to obtain a high maximum output power. The other is designed for a high load impedance in order to obtain a high dynamic range and high efficiency at a low output power. The proposed three-port asymmetric transmission line transformer, therefore, provides two load impedances.

The k-factor of the primary high-impedance transmission line to the secondary line should not exceed that of the low-impedance line in order to obtain the two load impedances effectively. If the k-factor of the high load impedance part exceeds that of the low load impedance part, the value of L_a of the high load impedance part cannot be higher than that of L_a of the low load impedance part. In this study, a three-port transmission line transformer is embodied, as shown in Fig. 8. The primary part for the low-power mode has spiral turns to increase the parasitic inductance of the transformer. The proposed three-port transmission line transformer is applied to the proposed power amplifier for a polar transmitter application in order to achieve a high maximum output power, high dynamic range, and high efficiency at a low output power region. The simulated loss of the transformer itself for a high power mode is approximately 1.7 dB.

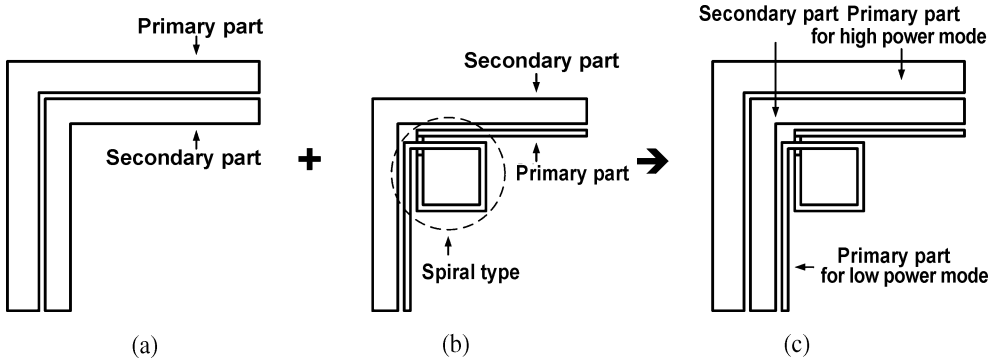


Fig. 8. Three-port asymmetric transmission line transformer. (a) Transformer for a high-power mode. (b) Transformer for a low-power mode. (c) Three-port transmission line transformer.

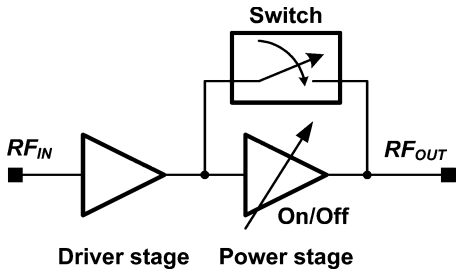


Fig. 9. Power amplifier with the bypass switch.

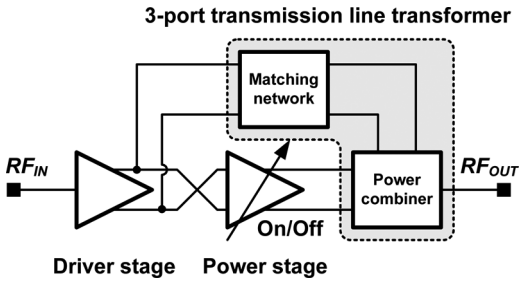


Fig. 10. Proposed stage-convertible power amplifier architecture.

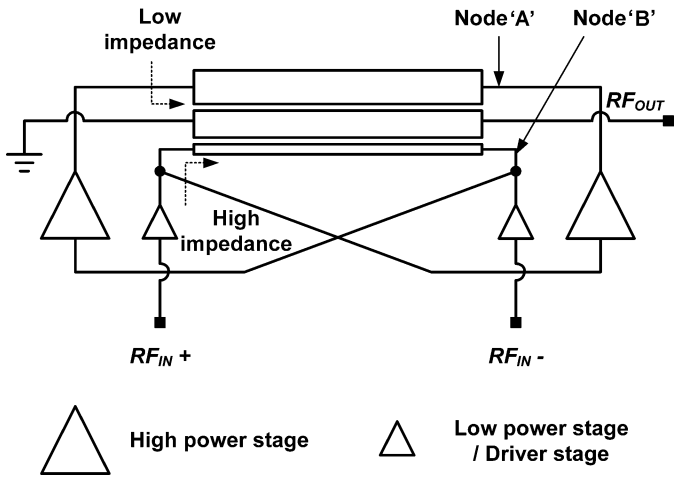


Fig. 11. Schematic of the stage-convertible power amplifier.

IV. Design of the 1.9-GHz CMOS Power Amplifier

A. Proposed Stage-Convertible Power Amplifier

The proposed stage-convertible power amplifier is a modified structure of a power amplifier with a bypass switch, as shown in Fig. 9 [9]. The switch is located parallel to the power stage, as shown in Fig. 9. The power stage is turned on and the switch is turned off to achieve the maximum gain and output power. For the low output power, the power stage is turned off and the switch is turned on to bypass the power stage. The output of driver stage then becomes the output of the power amplifier.

In the proposed power amplifier, a low-power matching network is located parallel to the power stage. The output of the power stage and the output of the matching network are combined in a power combiner, as shown in Fig. 10. For a high-power mode, the power stage is turned on and the driver stage drives the power stage. In addition, a certain amount of driver power is coupled to the output directly through the three-port transmission line transformer. The load impedance for the power stage is low to achieve a high maximum output power. For a low-power mode, the power stage is turned off and only power from the driver is transmitted into the output port through the low-power matching network. The load impedance of the driver stage must be high in order to obtain a high dynamic range in addition to a high efficiency in the low output power region. In the proposed stage-convertible power amplifier, high- and low-power modes of the power amplifier are selected by turning on, and off, respectively, the power stage. The power combiner and low-power matching network are implemented with the three-port transmission line transformer, as shown in Fig. 11. A schematic of the proposed power amplifier is shown in Fig. 11, which has a differential structure. The driver and power stages were designed as class-E amplifiers. The output of the power stage is connected to the one primary part of the transformer that has a low load impedance. The output of the driver stage is connected not only to the input of the power stage, but also to the other primary part of the transformer with a high load impedance.

For the high-power mode, all of the stages in the power amplifier are turned on to generate a high output power. For the low-power mode, the power stage is turned off and the output power is generated only by the driver stage. The output power of the driver stage is transmitted into the output while in the low-power mode. In Fig. 11, a pair of differential power stages and a pair of differential driver stages are cross-coupled to create

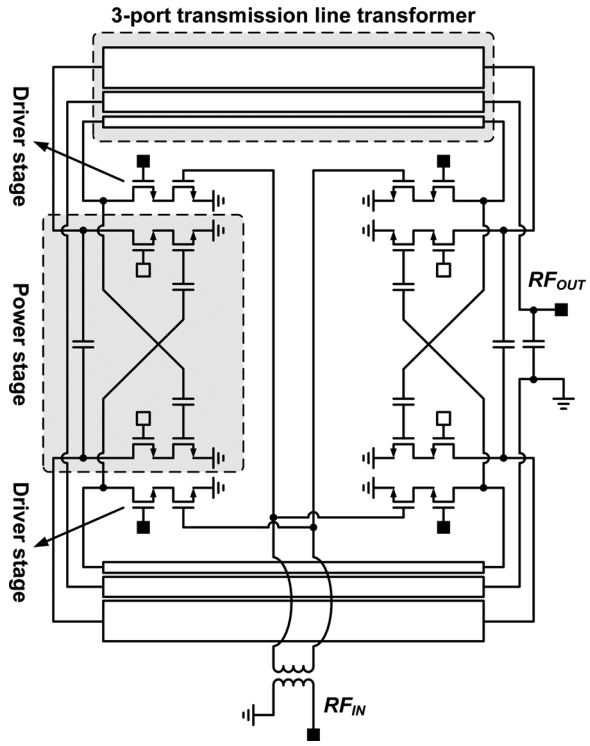


Fig. 12. Schematic of the designed power amplifier.

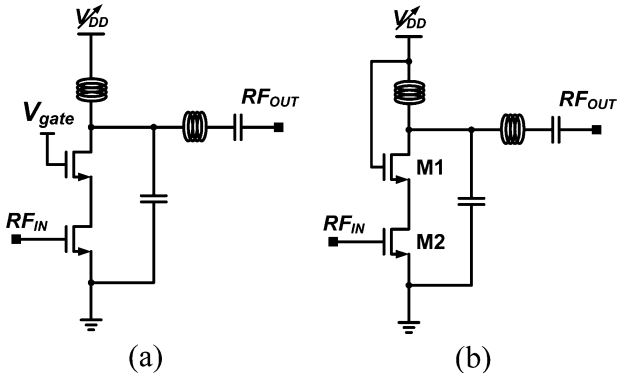


Fig. 13. Schematics of the power stages for: (a) conventional cascode structure and (b) self-biased cascode structure.

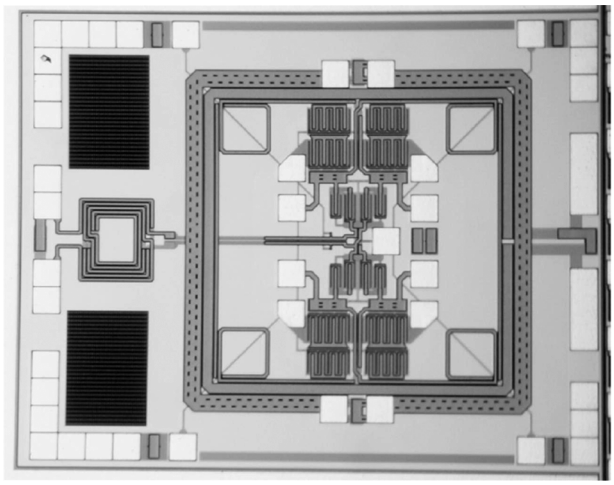


Fig. 14. Chip photograph of the implemented power amplifier.

node "A" and node "B" in the phase. In the proposed power amplifier, an additional power stage is not needed for the low-power mode. The driver stage works as the output stage in the low-power mode. The chip size is, therefore, reduced.

A schematic of the designed power amplifier is shown in Fig. 12. The concept of a distributed active transformer is used to realize the voltage-combining technique. Two differential pairs of the power stage and the driver stage are used. The output matching network of the power stage is implemented with the three-port transformers, the drain–source capacitance of the power stage, and an additional MIM capacitor. The output matching network of the driver stage is composed of the transformers, the drain–source capacitance of the driver stage, the gate–source capacitance of the power stage, and an additional MIM capacitor. The input transformer consists of a spiral-type transformer.

B. Auto-Switching Technique

An auto-switching technique is used to switch to the high- and low-power modes automatically with respect to the V_{DD} of the power amplifier, which is an amplitude signal of a polar transmitter. Therefore, an additional external control signal to change the mode of the power amplifier is not needed.

As mentioned in Section II, the output power of a polar transmitter is controlled via the variable V_{DD} of the power amplifier. The output power is, therefore, increased as V_{DD} is increased. Here, both the driver stage and power stage are turned on when the supply voltage becomes high. However, the driver stage is turned on and the power stage is turned off automatically when the supply voltage is low. A cascode structure is used in each stage to realize the auto-switching technique. A conventional cascode structure is shown in Fig. 13(a), and a self-biased cascode structure is shown in Fig. 13(b) [10]. If the supply voltage of the self-biased cascode structure is decreased, the on resistance of $M1$ is increased and the current through the power transistor of the self-biased cascode structure becomes smaller than that of the conventional cascode structure.

In this study, the conventional cascode structure is used in the driver stage and the self-biased cascode structure is used in the power stage. The power stage is programmed to be turned on or turned off automatically according to the variable supply voltage. The contribution of the power stage to the output power is decreased and the contribution of the driver stage to the output power is increased as V_{DD} is decreased. Thus, the high-power mode becomes dominant in the higher V_{DD} region and the low-power mode becomes dominant in the lower V_{DD} region.

V. Measurement Results

Fig. 14 shows the implemented power amplifier using 0.18-μm RF CMOS technology. The size of the chip is 1.2 mm $\times$ 1.8 mm including pads. All of the matching components, including the input and output transformers, are fully integrated. The area of the transformer is 1.0 mm $\times$ 1.0 mm. The metal for the transformer is 2.34-μm-thick aluminum.

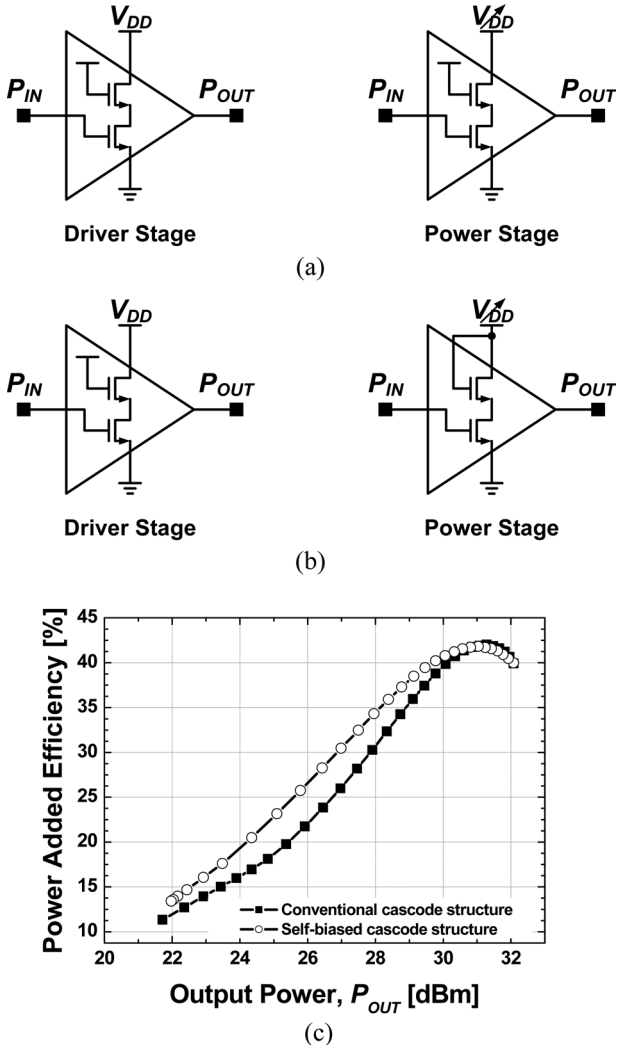


Fig. 15. Circuit configurations of: (a) conventional cascode structure, (b) self-biased cascode structure, and (c) measurement results.

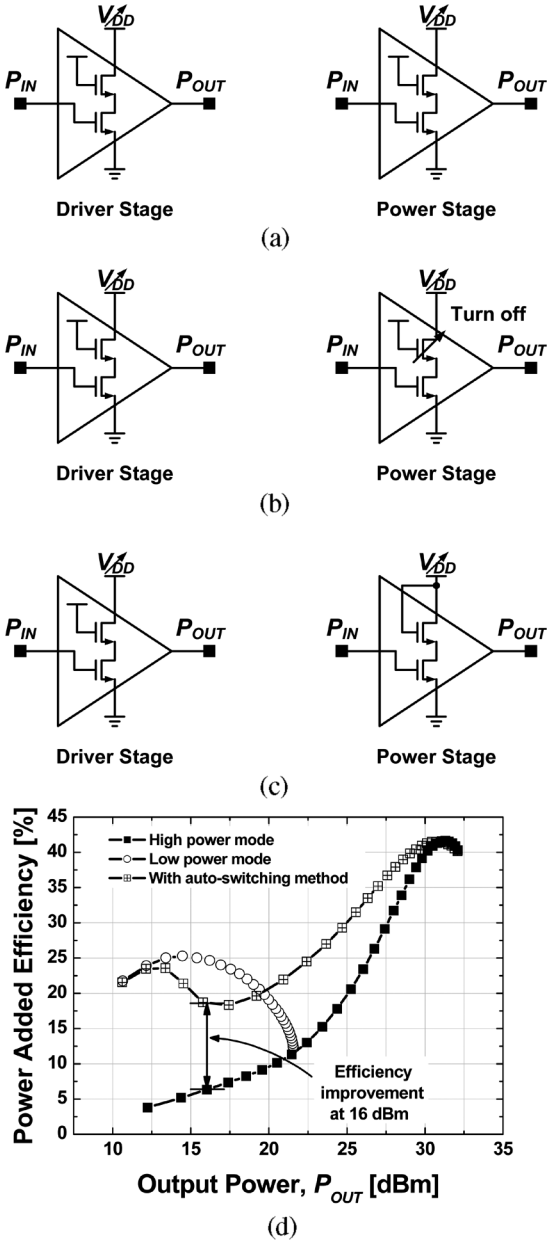


Fig. 16. Circuit configurations of: (a) high-power mode, (b) low-power mode, (c) auto-switching technique, and (d) measurement results.

The losses of the bond-wire, input transformer, and printed circuit board interconnections are included in the amplifier's measured performance. Fig. 15 shows the measured PAE versus $P_{\rm OUT}$, while V_{DD} varies from 0.5 to 3.3 V. In Fig. 15(a), conventional cascode structures are used in the power and driver stages, and V_{DD} of the power stage varies while V_{DD} of the driver stage remains fixed. In Fig. 15(a), the gate bias in the cascode transistor of the power stage is fixed at 3.3 V. If the gate bias is lower than 3.3 V, the maximum output power and PAE are degraded. In Fig. 15(b), a self-biased cascode structure is used in the power stage. The measured PAE of Fig. 15(b) is higher than that of Fig. 15(a). For the circuit configuration of Fig. 15(b), the contribution of the power stage decreases as V_{DD} decreases. The efficiency of the structures in Fig. 15(b) in the low-power region is, therefore, higher than those in Fig. 15(a). The measured dynamic range is not sufficient for a GSM specification, and the efficiency improvement in the low output power region is limited.

To extend the dynamic range and to increase the efficiency further, V_{DD} of the driver stage also varies with V_{DD} of the power stage, as shown in Fig. 16. A measurement of the high-power mode shows that the maximum output power is 32 dBm with a PAE of 40%. Theoretically, the dynamic range of a conventional class-E amplifier is approximately 16.4 dB, while V_{DD} varies from 0.5 to 3.3 V. However, the dynamic range of the high-power mode is extended to nearly 20 dB, as the input power of the power stage also decreases when V_{DD} of the driver stage decreases. For the low-power mode, the power stage is turned off by an external signal. Due to the high load impedance of the low-power mode, the efficiency in a low output power region is increased. With the circuit configuration shown in Fig. 16(c), the auto-switching technique is realized by the self-biased cascode structure in the power stage. In the low output power region, the input power of the power stage is decreased. The contribution of the power stage is, therefore, decreased and the contribution of the driver stage that has a

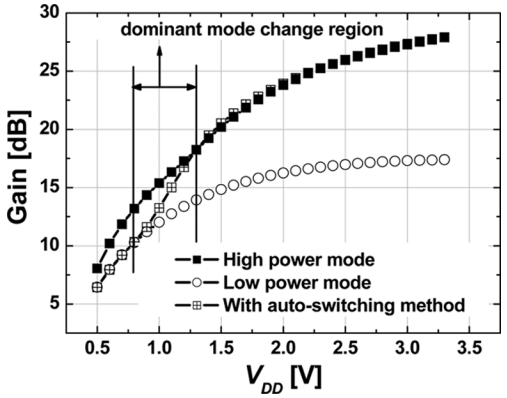


Fig. 17. Measured gains of different modes.

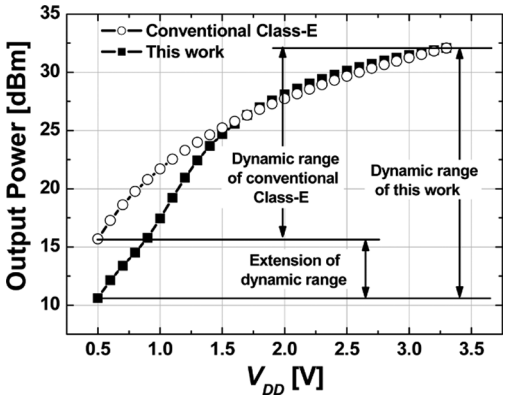


Fig. 18. Extension of dynamic range.

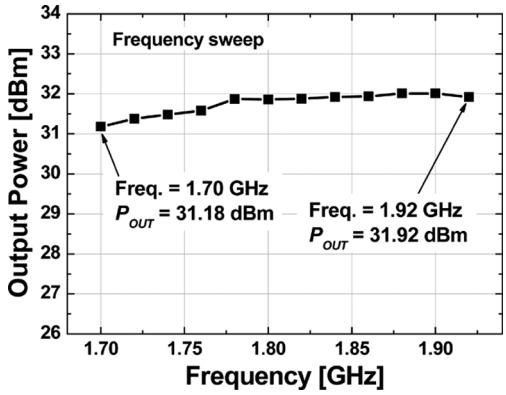


Fig. 19. Measured frequency response.

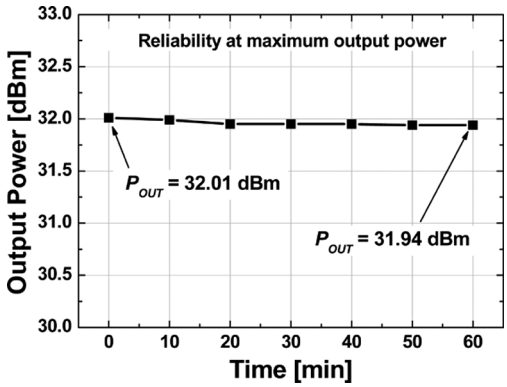


Fig. 20. Measured degradation of the output power with time.

higher load impedance is increased. Thus, the power and driver stages are always turned on. As shown in Fig. 17, the mode of the power amplifier is changed automatically and smoothly with V_{DD}. This is due to the self-biased cascode structure of the power stage.

Fig. 17 shows the measured gains of different modes. For a given V_{DD}, the gain of a high-power mode always appears higher than that of a low-power mode due to the fixed input power of the class-E amplifier. As indicated in the graph, the mode of the power amplifier with the auto-switching method is changed automatically and smoothly in the mode-change region.

Fig. 18 shows an extension of the dynamic range. The white symbols show the theoretically calculated output power of a conventional class-E amplifier. The dynamic range of a conventional class-E amplifier is approximately 16.4 dB, while V_{DD} varies from 0.5 to 3.3 V. The black symbols show the output power of the circuit configuration shown in Fig. 16(c). The measured extension of dynamic range is nearly 4 dB.

Fig. 19 shows the frequency response under the maximum output power conditions. The single-ended output power is higher than 31 dBm over a frequency range of 1.70–1.92 GHz. Fig. 20 shows the measured degradation of the output power with time under the maximum output power conditions.

The nonlinearities of a polar transmitter are mainly due to signal delay mismatches between amplitude path and phase path. There are also due to the AM–PM distortion of the amplifier. However, the nonlinearities can be solved using a digital predistorter in the polar transmitter.

VI. Conclusions

A 1.9-GHz power amplifier for a polar transmitter application has been implemented using 0.18-μm RF CMOS technology. Stage-convertible power-amplifier architecture, an auto-switching technique, and a three-port asymmetric transmission line transformer have been proposed in order to improve efficiency and dynamic range. The improvement of the dynamic range is approximately 4 dB, and the total dynamic range is nearly 20 dB. The low-power efficiency improvement of the power amplifier is 290% at an output power of 16 dBm.

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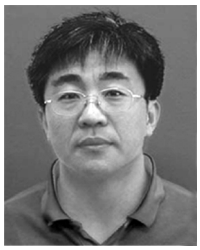

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