Noise Property of a Quadrature Balanced VCO

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***Abstract*—A quadrature balanced voltage controlled oscillator (B-VCO) with current source switching is proposed and analyzed. This letter shows analytically that the switching improves the phase noise. A switched transistor is also used as a coupling transistor to generate quadrature signals without degrading the phase noise. To investigate the effect of quadrature coupling on the phase noise, a single B-VCO and a quadrature B-VCO are implemented with identical components in an 0.18-μm CMOS process. Both VCO cores draw about 8.8 mA under a low bias voltage of 1.8 V. The oscillation frequencies are 10.21 GHz and 10.81 GHz. The measured phase noises of the single at an offset frequency of 1 MHz VCO is −114.83 dBc/Hz while that of the quadrature VCO is −116.67 dBc/Hz. The quadrature B-VCO is superior to the single B-VCO with respect to phase noise and oscillation frequency in the X-band.**

***Index Terms*—Balanced, CMOS, current switching, noise, quadrature, transformer, voltage controlled oscillator (VCO).**

I. Introduction

THE quadrature signal source is a key component in image-rejection transceivers. Recently, the many different topologies of a differential (cross-coupled) voltage controlled oscillator (VCO) have enabled many quadrature VCOs to be implemented because of the ease with which a quadrature coupling transistor can be added [1], [2].

A CMOS differential VCO with a p-MOS and an n-MOS is superior at low frequency. However, a VCO in the x-band is composed of only an n-MOS since a p-MOS is unavailable at about the x-band. The noise property of a differential VCO with only an n-MOS is inferior to that of a B-VCO in a high frequency VCO [3]. Nonetheless, a B-VCO consumes a high bias current to have a reliable start-up. To overcome the disadvantages of a B-VCO, current source switching is used [4]. However, the topology also affects the superior phase noise property of a B-VCO because the topology is similar to a differential VCO This letter shows that the switching analytically improves the phase noise and that the B-VCO is proposed to generate quadrature signals in the X-band.

II. Circuit Design

The proposed B-VCO block with current source switching consists of n-MOS transistors and a transformer composed of L_1 and L_2 as shown in Fig. 1. The capacitive voltage divider that provides a positive feedback path is formed by C_{f1} and C_{f2}.

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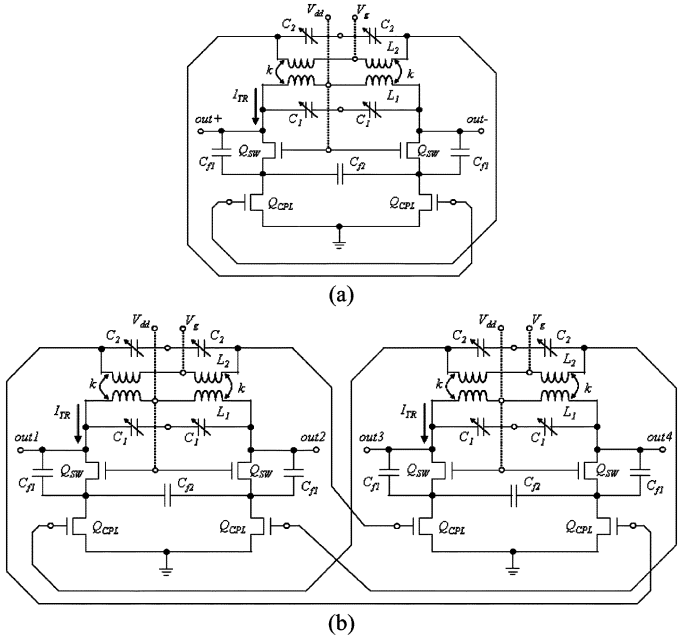


Fig. 1. Schematics of the proposed (a) single and (b) quadrature balanced VCOs.

In a conventional structure, Q_{SW} and Q_{CPL} are transistors for negative resistance and current source, respectively. However, a gate of Q_{CPL} in the proposed structure is connected to the output of L_2 and the C_2 resonator for a current source switching. The L_2 of the transformer is connected to the external bias of V_g. Thus, the gate bias of Q_{CPL} is controlled under a fixed supply voltage. It is useful to observe the effects of a bias current. The components of the VCOs that generate differential $(out\pm)$ and quadrature signals $(out1 \sim 4)$ are identical. The two VCOs differ only in the connections of the feedback signal, as shown in Fig. 1 [5].

III. Noise Analysis

A balanced topology and a differential topology have been compared analytically [3]. The transistor in this letter is a BJT. However, this analysis is useful for a MOS because the dominant noise source is a channel noise. This letter shows that the negative conductance and noise properties in the g_m cell of a balanced topology are superior to those of a differential topology at high frequency. However, a balanced topology with current switching differs from a conventional balanced topology in a phase noise property. The cross connected topology in current source switching is similar to the differential topology. In this section, we used analytic noise models to investigate the effect of the current switching.

A phase noise simulation includes harmonic balanced simulations with a nonlinear large-signal model. Although the model

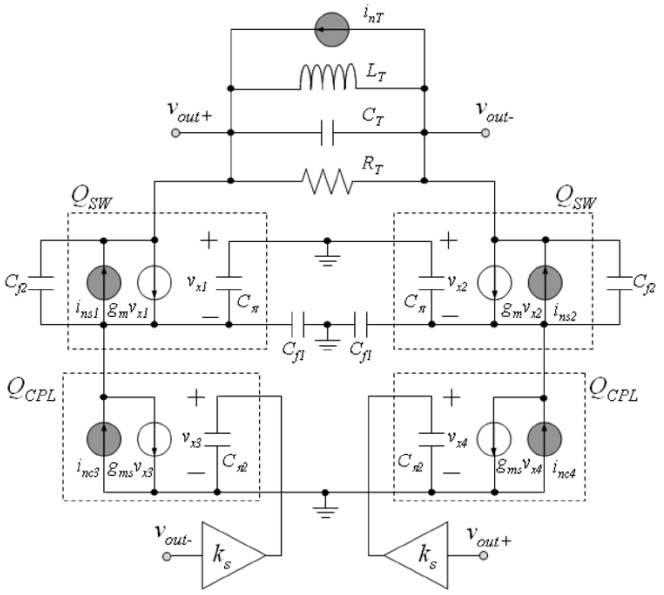


Fig. 2. Equivalent circuit of the single B-VCO with noise source.

is useful for predicting the accurate phase noise, this is too complex to help a chip-designer understand the VCO operations and phase noises. However, a linear phase noise model is simple and gives useful insight into the phase noises although the model is not accurate [3], [7].

Fig. 2 represents the linear models of single balanced topologies. The transistor model excludes the gate drain capacitance C_μ and the output resistor r_0 for simplicity. The LC thank is modeled with L_T, C_T, and R_T. The model includes a single noise source, i_{nc} or i_{ns}, which is the sum of the channel and flicker noises in a transistor. It also includes the LC tank noise i_{nT}. This analysis is similar to that of [3]. The output amplitude v_o of the LC tank is described as the superposition of all the noise sources.

The noise power of the output signal $(v_o = v_{out+} - v_{out-})$ is represented by summing up all the noise powers as follows:

$$\overline{v_o^2} = \frac{1}{2} \cdot \left(2 \cdot a_{SW}^2 \cdot \overline{i_{ns}^2} + 2 \cdot a_{CPL}^2 \cdot \overline{i_{nc}^2} + 2 \cdot a_{\text{TANK}}^2 \cdot \overline{i_{nT}^2} \right) \tag{1}$$

where a_{SW}, a_{CPL} and a_{TANK} indicate the noise contribution coefficients [3]. Each noise contribution coefficient is represented as follows:

$$a_{SW} = \frac{sC_{f1}}{2P} + \frac{\left(\frac{sC_{f1}}{2P} - 1 \right) (sC_{f1} + g_{m1})}{\frac{2P}{sC_{f1}} \cdot (sC_\sigma + g_\sigma) - (sC_{f1} + g_{m1})} \tag{2}$$

$$a_{CPL} = \frac{1}{sC_{f1}} \frac{sC_{f1} + g_{m1}}{\frac{2P}{sC_{f1}} \cdot (sC_\sigma + g_\sigma) - (sC_{f1} + g_{m1})} \tag{3}$$

where

$$C_\sigma = C_{f1} + C_{f2} + C_\pi \tag{4a}$$

$$g_\sigma = g_{m1} + k_s \cdot g_{m3} \tag{4b}$$

$$P = \frac{1}{sL_T} + \frac{1}{R_T} + s \cdot C_T + \frac{s \cdot C_{f1}}{2} \tag{4c}$$

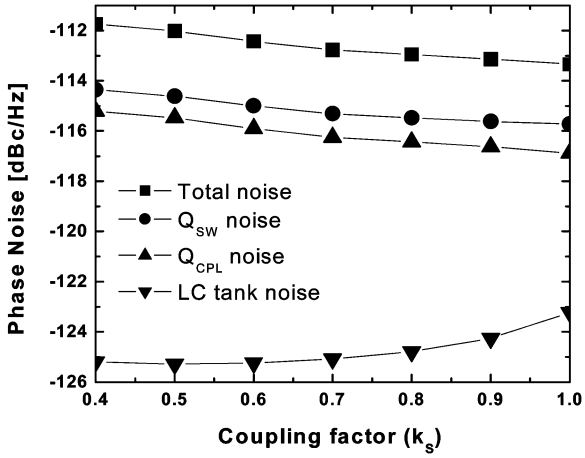


Fig. 3. Total phase noise at 1-MHz offset frequency and noise contribution of each component on a LC resonator.

and k_s is the coupling coefficient. A conventional B-VCO is $k_s = 0$. If k_s increases, the open loop gain and the effective trans-conductance g_σ increase as follows:

$$\left| \frac{2P}{sC_{f1}} \right| = \left| 1 + \frac{2}{sC_{f1}} \left(\frac{1}{sL_T} + \frac{1}{R_T} + sC_T \right) \right| > 1 \tag{5a}$$

$$\left| \frac{2P}{sC_{f1}} \cdot (sC_\sigma + g_\sigma) \right| > |sC_\sigma + g_\sigma| . \tag{5b}$$

Because of (5a) and (5b), when k_s increases, $|a_{SW}|$ and $|a_{CPL}|$ decrease. In other word, Q_{SW} and Q_{CPL} contribute less noise to the LC tank. The current switching not only increases the open loop gain but also decreases the noise contribution of the active device noise

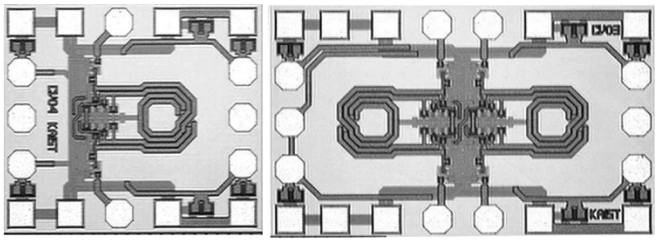
$$a_{\text{TANK}} = \frac{2}{2 \cdot P - sC_{f1} \frac{sC_{f1} + g_{m1}}{sC_\sigma + g_\sigma}} . \tag{6}$$

As shown in (6), the noise contribution of the tank a_{TANK} increases as k_s increases, whereas $|a_{SW}|$ and $|a_{CPL}|$ decrease. The parameter $|a_{\text{TANK}}|$ is not dominant in the phase noise. Thus, the total noise power decreases as k_s increases.

This analysis is supported by the harmonic balanced simulation in the Agilent ADS with BSIM3 MOS model, which is shown in Fig. 3. The model shows the phase noise at a 1 MHz offset frequency of a 10-GHz oscillation frequency with respect to the coupling factor k_s. The contribution of each noise source for k_s agrees with the noise analysis. It shows that the noise of Q_{CPL} is comparable to that of Q_{SW} when the LC tank noise is quite low. According to some reports, the current switching of a B-VCO is used to decrease the bias currents and to ensure a reliable start-up [4]. We show, however, that current switching, which is readily achieved with quadrature coupling transistors, has the advantage of reducing noise from active devices. Moreover, the low noise property of proposed VCO is available when the topology is modified to generate quadrature signals [5].

IV. Experimental Results

The presented quadrature VCO is implemented in a standard 0.18 μm CMOS process, which provided five layers of Al



(a) (b)

Fig. 4. Photographs of the fabricated (a) single (670×770 μm^2) and (b) quadrature balanced VCO (680×1100 μm^2).

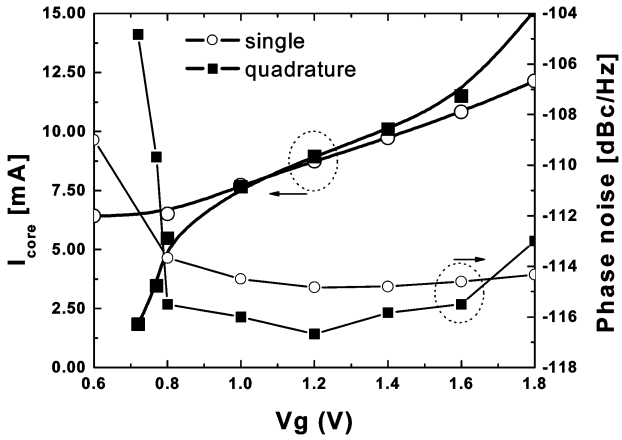


Fig. 5. Core bias currents and phase noise measurements at 1-MHz offset of single and quadrature B-VCO as bias control voltage Vg.

metal and 2-μm-thick analog AlCu metal. As shown in Fig. 4, the chip sizes of the single VCO and the quadrature VCO were 670×770 μm^2 and 680×1100 μm^2. For a comparison of phase noises, all the components in both VCOs were identical.

The VCOs are measured by on-wafer probing with Agilent HP9764E spectrum analyzer and its accompanying kit for measuring phase noises. The VCO works under 1.8 V supply voltage. The cable loss in the measurement setup was about 2 dB at 10 GHz.

The oscillation frequency of the single VCO was 10.21 GHz, while that of the quadrature VCO was 10.81 GHz. The phase noise of the single B-VCO was -114.83 dBc/Hz at a 1-MHz offset frequency. Theoretically, the quadrature coupling improves the phase noise by about 3 dB [5]. The phase noise in the quadrature VCO improved by 1.84 dB. Although the improvement is lower than 3 dB, the noise property of the proposed single B-VCO is available in the quadrature. Both VCOs showed very high figure of merit (FOM) [6] of 183 dB and 185 dB. These results show, for the first time, that the balanced structure generates quadrature signals without degrading the phase noise performance.

The phase noise at a 1-MHz offset frequency and the bias current for the oscillation condition were measured by adjusting V_g as shown in Fig. 5. The current of the quadrature VCO increased faster than that of the single VCO at $V_g > 1.2$ V. The phase difference between the gate and the drain of Q_{CPL} was about 180° in the single VCO. The difference was about 90° in the quadrature VCO because the gate was driven by the quadrature signals. When Vg increases, these properties cause the I_{SW} of the quadrature VCO to increase faster than I_{SW} of the single VCO. A part of I_{SW} should be stored in C_2 due to the phase difference between I_{CPL} and I_{SW}. Thus, the difference has effect on the initial bias current for the reliable start-up. The single VCO can oscillate until $I_{bias} = 6.5$ mA, and the quadrature VCO can oscillate until $I_{bias} = 7.5$ mA. The single VCO is superior in the start-up condition. However, if the bias of VCO is decreased after the VCO oscillates, the quadrature B-VCO does under lower bias current than that of the single B-VCO as shown in Fig. 5.

The minimum phase noise is at $I_{bias} = 8.8$ mA in both VCOs. The phase noise was almost unchanged with respect to Vg, though the bias current increased with Vg. Generally, the noise power decreases as the bias current increases. The increase in the bias current causes an increase in not only the noise power but also the g_m of the Q_{CPL}. Thus, the phase noise is almost constant. Section III shows that the noise decreases as the g_m increases.

V. Conclusion

We proposed and analyzed an X-band CMOS quadrature B-VCO. Single and quadrature B-VCOs use current switching for a reliable start-up, for reduction of active noises and for quadrature coupling. We showed analytically that current switching improves the phase noise. The phase noise of the single VCO was -114.83 dBc/Hz at the offset frequency of 1 MHz at 10.21 GHz; the corresponding value for the quadrature VCO was -116.67 dBc/Hz at the offset frequency of 1 MHz at 10.81 GHz. The VCO cores consume about 8.8 mA from a 1.8 V supply. The single VCO achieved an FOM of 183 dB, and the quadrature VCO achieved an FOM of 185 dB. Except for the start-up condition, the quadrature VCO is superior to the single VCO in the phase noise, the oscillation frequency, the tuning range, and the FOM.

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References

[1] P. Andreani, A. Bonfanti, L. Romanò, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.

[2] D. Baek, T. Song, E. Yoon, and S. Hong, "8-GHz CMOS quadrature VCO using Transformer-Based LC tank," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 446–448, Oct. 2003.

[3] D. Baek, S. Ko, J. Kim, and S. Hong, "Ku-Band InGaP/GaAs HBT MMIC VCOs with balanced and differential topologies," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1353–1359, Apr. 2003.

[4] R. Aparicio and A. Hajimiri, "A noise-shifting differential colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.

[5] S. Ko, H. D. Lee, D.-W. Kang, and S. Hong, "An X-band CMOS quadrature balanced VCO," in *IEEE MTT-S Int. Dig.*, 2004, pp. 127–272.

[6] E. Hegazi, H. Sjöland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[7] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE. J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.