Ku-Band MMIC Phase Shifter Using a Parallel Resonator With 0.18-μm CMOS Technology

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***Abstract*—A digital 5-bit phase shifter at Ku-band is presented, which is implemented with 0.18-μm RFCMOS technology. n-MOSFET switches and top metal microstrip lines with a first-metal ground allow the phase shifter to have small insertion losses. The proposed 90° phase shifter utilizing a parallel resonator exhibits broad-band characteristics. All of the circuit components are derived to obtain a minimum phase variation at the operation frequency band. A bridged-T type phase shifter is also analyzed in view of parallel resonance using an ideal equivalent-circuit model. The conditions of the circuit elements are derived in an analytic form, which are used to obtain the broad-band phase characteristics. The fabricated 5-bit phase shifter demonstrates an overall rms phase error less than 12° from 9 to 15 GHz. Insertion losses of 14.5 dB $\pm$ 0.5 dB and return losses less than 14 dB are obtained for 32 states at 12 GHz. The proposed 90° phase shifter has performed a phase shift of 92.3° $\pm$ 3.2° over 9–15 GHz.**

***Index Terms*—CMOS switches, phased-array system, phase shifter, satellite communications.**

I. Introduction

ACTIVE phased-array antenna systems are receiving increased attention for satellite communications and radars since they allow a higher channel capacity and the maximum overall SNR of receivers. A number of commercial opportunities are emerging in the broad-band wireless communications, terrestrial wireless, global positioning system (GPS), and automotive electronics markets. Recently, direct broadcast satellite (DBS) for mobile reception has been identified as a prime application and is planned in many countries. This system requires integrated phase shifters to track satellites as vehicles move through uneven terrain. However, it is critically important that a low-cost and small-size phased-array system be developed for the emerging commercial applications. This can be achieved by developing low-cost phase shifters or, alternatively, through the construction of other scanning systems without a phase shifter [1].

GaAs field-effect transistor (FET)-based phase shifters have been widely used in array systems due to their low insertion loss and low dc power consumptions [2]–[4]. Recent sub-quarter micrometer CMOS technology offers excellent microwave performances, which are comparable to those of GaAs technology with a high integration level. Moreover, an RF CMOS product can be cost effective if the volumes are sufficiently high.

A MOS is known as an excellent switching device at low frequencies. MOS switches do not require a negative control voltage and can be implemented with digital controllers in a chip. Although advanced silicon technology has improved the switching performances of MOSFETs, a silicon MOS switch still exhibits a high insertion loss at high-frequency ranges because of its high on resistance and conducting substrate. The efforts to improve the switch performances have been demonstrated for many years [5]–[8].

There has been a great deal of study to implement a phase shifter in Si technology. A phase shifter using a low-loss microelectromechanical systems (MEMS) switch has developed at frequencies through 40 GHz [9], [10]. Zarei and Allsot [11] recently demonstrated a reflective-type phase shifter using negative resonant circuits in a 2-GHz frequency range. The negative-reflective-type analog phase shifter (NR RTPS) using 180-nm CMOS improves the insertion-loss performance and phase-shifting ranges compared to the conventional RTPS. In the study by Teshiba *et al.* [12], a p-i-n diode phase shifter was realized in a silicon germanium bipolar technology. However, p-i-n diodes consume high dc power and require negative voltages. Lee *et al.* [13] reported on a 4-bit digital phase shifter using MOS switches. Some efforts to manipulate a phase distribution without a phase shifter have also been published.

This paper is organized as follows. Section II describes the investigation on the improvement of the insertion loss of the MOSFET switch with a source-body short. After which, the experimental results of the microstrip line with a first-metal ground are described. Section III discusses the analysis of the proposed 90° phase shifter using a parallel resonator. In Section IV, we have also derived the conditions of circuit elements to obtain a broad-band phase characteristic for a bridged-T-type phase shifter. Finally, the measured RF characteristics of the 5-bit phase shifter are presented.

II. MOS Switches and Microstrip Lines

A. MOS Switches

The key component of the CMOS phase shifter is a MOS switch. In silicon technologies, it is difficult to make a good switch because of the capacitive coupling of a switch transistor with a substrate. The insertion loss of the switch is affected by the source/drain junction capacitance, on-resistance, and the coupling with a conductive Si-substrate [5]. An nMOS transistor is usually used as a switch because the on resistance is an important factor for determining the insertion loss of the

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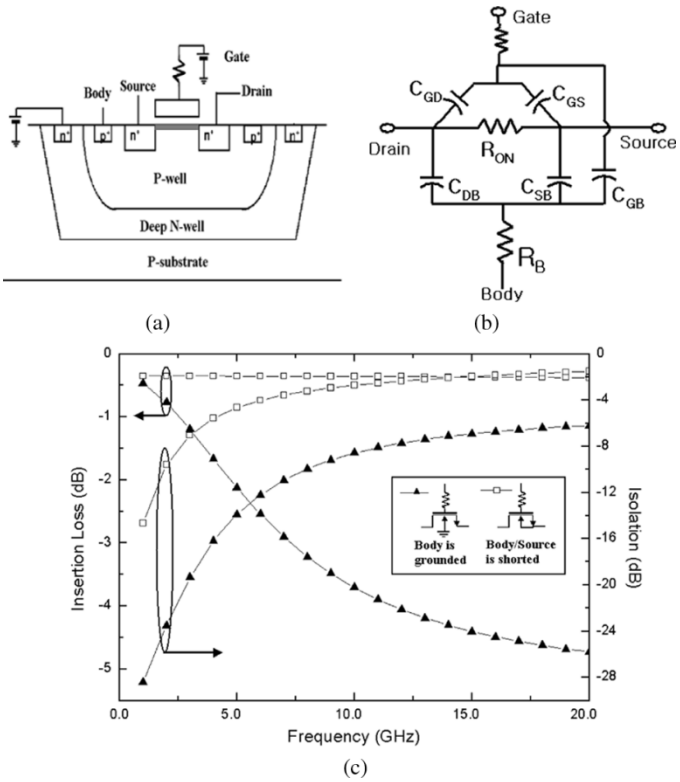

Fig. 1. (a) Cross-sectional illustration of an NMOS. (b) Equivalent-circuit diagram of the nMOS shown in (a). (c) Simulated insertion loss and isolation for the switch when the body is grounded, and the switch when the body-to-source is shorted.

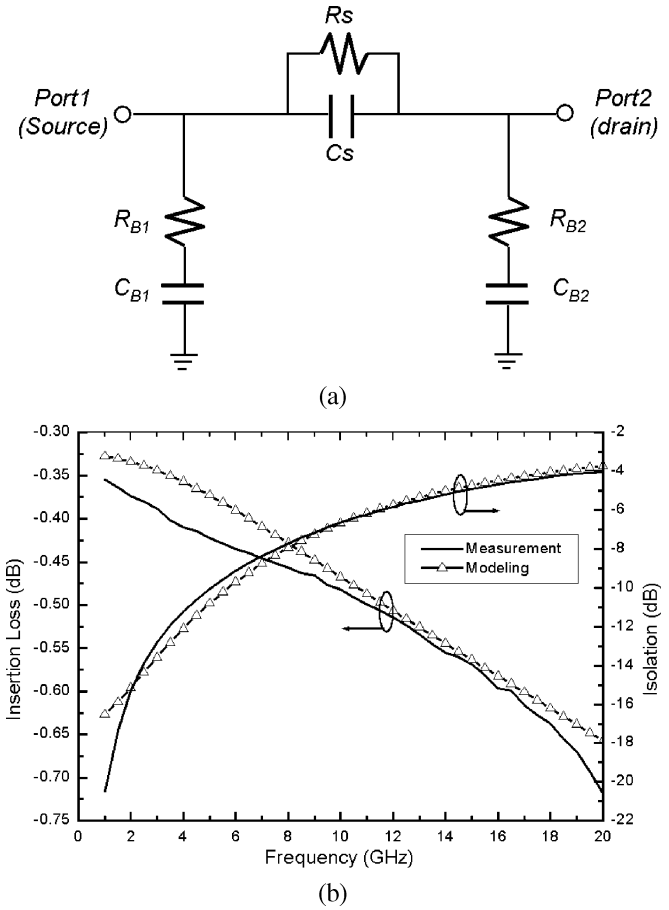

Fig. 2. (a) Equivalent circuit of the MOS switch with a source-body short. (b) Comparison of modeled data and experimental data for the switch with total gatewidth of 150 μm.

switch. The cross section of an nMOS transistor is illustrated in Fig. 1(a). The nMOS transistor is made with a deep-submicrometer triple-well CMOS technology. This technology offers the possibility of biasing the body port. A biasing resistor at the gate of the switch transistor is added. It is included to isolate the control from the signal path. A typical value of the resistor is approximately 25 kΩ. Fig. 1(b) shows an equivalent-circuit diagram of an nMOS transistor. The insertion loss is mainly determined by the on-resistance $(R_{\rm on})$ of the transistor at low frequencies. If the body is grounded, the power loss increases due to the increase of capacitive coupling with the substrate at high frequencies. When the body and source are shorted together, the insertion loss decreases by removing the ground path through the substrate resistor. In the off-state case, only one junction capacitance $(C_{\rm DB})$ can be considered because the source and body are shorted. This off-state capacitance degrades the isolation of the switch. However, it is possible to incorporate the off-state capacitance as one of filter elements. For comparative purposes, we have plotted the insertion loss and isolation using a standard TSMC model in Fig. 1(c). The switch with the source-to-body short shows dramatic improvement of the insertion loss at the sacrifice of the isolation of the switch.

The drain/body capacitance $(C_{\rm DB})$ and on resistance $(R_{\rm on})$ remain as the dominant factors of the switch. The circuit shown in Fig. 2(a) can be approximated with the model of the switch. This equivalent circuit is used in the on-state condition, as well as the off-state condition. R_{B1}, R_{B2}, C_{B1}, and C_{B2} represent the parasitic resistances and capacitances resulting from the Si substrate. The resistance R_s and capacitance C_s are the on-state resistance and off-state capacitance. This model of the switch transistor is scalable; all the model parameters are derived as functions of the finger number. The switch parameters are derived from the following analytical expressions for the Y-parameters:

$$R_s = \frac{1}{\mathrm{Re}[-Y_{12}]}$$

$$C_s = \frac{\mathrm{Im}[-Y_{12}]}{\omega}$$

$$R_{B1} = \mathrm{Re}\left[\frac{1}{Y_{11}+Y_{12}}\right]$$

$$C_{B1} = \frac{-1}{\omega \times \mathrm{Im}\left[\dfrac{1}{Y_{11}+Y_{12}}\right]}$$

$$R_{B2} = \mathrm{Re}\left[\frac{1}{Y_{22}+Y_{21}}\right]$$

$$C_{B2} = \frac{-1}{\omega \times \mathrm{Im}\left[\dfrac{1}{Y_{22}+Y_{21}}\right]}.$$

Fig. 2(b) shows the measured and modeled switch characteristics of a switch with a 150-μm gatewidth. The modeled results show good agreement with the measured results. The insertion

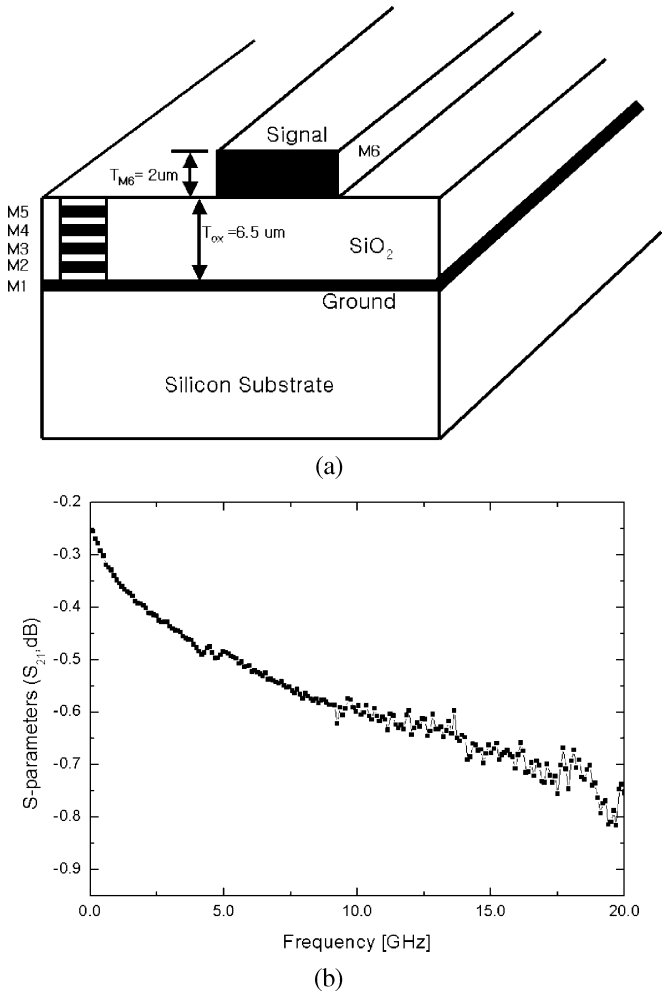

Fig. 3. (a) Cross section of the microstrip line. (b) The measured S-parameter of a 2-mm-long microstrip line.

loss is less than -0.75 dB over a 0.1–20-GHz range. The corresponding off capacitance of the switch is approximately 0.1 pF.

B. Microstrip Lines

The current CMOS technology is based on conductive silicon substrates. The microstrip line with the a first-metal ground has an advantage in propagation loss compared with other transmission lines without the first metal ground. This is because most electrical fields are confined in a silicon–oxide layer instead of the silicon substrate. The loss associated with the substrate can be obviated by a metal ground plane on the Si substrate. The microstrip line is realized by using the top metal as a signal line and the first metal as a ground in standard CMOS technology. The top metal and first metal are fabricated with 2- and 0.5-μm-thick Al metals, respectively, as shown in Fig. 3(a). The oxide thickness is approximately 6.5 μm. The bottom metal completely eliminates the electric field that penetrated through the substrate as long as the skin depth in the ground plane is not larger than the metal thickness.

The signal loss with frequency is shown in Fig. 3(b). The 8-μm-wide microstrip line results in a loss of 0.3 dB/mm at 10 GHz. This can be exploited in the design of a phase shifter, as will be shown in Sections III and IV.

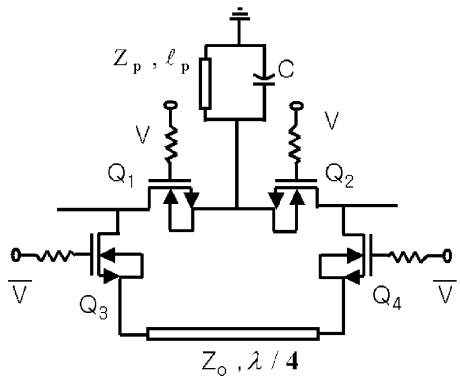

Fig. 4. Schematic of the proposed 90° phase shifter.

III. Proposed 90° Phase Shifter

Fig. 4 shows a schematic diagram of the proposed 90° phase shifter. The differential phase shift is obtained by switching the parallel transmission-line resonator with a capacitor and a $\lambda/4$ line. When switches Q_1 and Q_2 are "on" and Q_3 and Q_4 are "off," a signal transfers through the on resistances of Q_1 and Q_2, while effectively having a zero insertion phase. When the gate biases are reversed, a signal passes through a $\lambda/4$ microstrip line with a -90° insertion phase. The input admittance of the shorted line of length ℓ_p is given by

$$Y_{\ell\_\text{in}} = -jY_p \cot(\beta \ell_p.) \tag{1}$$

The transmission matrix for the parallel resonator circuit is given by

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & 0 \\ Y_{\text{in}} & 1 \end{vmatrix} = \begin{vmatrix} 1 & 0 \\ j\big(\omega C - Y_p \cot(\beta \ell_p)\big) & 1 \end{vmatrix}. \tag{2}$$

The transmission coefficient S_{21} and reflection coefficient S_{11} from the transmission matrix are given by

$$\begin{aligned} S_{21} &= \frac{2}{A + \dfrac{B}{Z_0} + CZ_0 + D} \\ &= \frac{2}{2 + jZ_0\big(\omega C - Y_p \cot(\beta \ell_p)\big)} \end{aligned} \tag{3}$$

$$\begin{aligned} S_{11} &= \frac{A + \dfrac{B}{Z_0} - CZ_0 - D}{A + \dfrac{B}{Z_0} + CZ_0 + D} \\ &= \frac{-j\big(\omega C - Y_p \cot(\beta \ell_p)\big)}{2 + jZ_0\big(\omega C - Y_p \cot(\beta \ell_p)\big)}. \end{aligned} \tag{4}$$

In (1)–(4), $Z_p = 1/Y_p$ is the characteristic impedance of the microstrip line of the parallel resonator, and β is the propagation constant of the microstrip line. Using (3), the transmission phase ϕ_R and the derivative of the phase with respect to ω can be written as

$$\phi_R = \tan^{-1}\left(\frac{Z_0}{2}\left(Y_p \cot(\beta \ell_p) - \omega C\right)\right) \tag{5}$$

$$\frac{d\phi_R}{d\omega} = \frac{\frac{Z_o}{2}\left[Y_p\frac{\beta\ell_p}{\omega}\left(-1-\cot^2(\beta\ell_p)\right)-C\right]}{1+\left[\frac{Z_o}{2}\left(Y_p\cot(\beta\ell_p)-\omega C\right)\right]^2}. \tag{6}$$

The phase shifter will be perfectly matched when $|S_{11}| = 0$ is satisfied. Using (4), we can obtain the following equation:

$$C = \frac{Y_p}{\omega_o}\cot(\beta_o\ell_p) \tag{7}$$

where ω_o is the desired frequency and β_o is the propagation constant at ω_o.

The substitution of (7) into (6) gives

$$\left.\frac{d\phi_R}{d\omega}\right|_{\omega=\omega_o} = -\frac{Z_o}{2}\frac{Y_p}{\omega_o}\left[\beta_o\ell_p\left(1+\cot^2(\beta_o\ell_p)\right)+\cot(\beta_o\ell_p)\right]. \tag{8}$$

The derivative of the transmission phase ϕ_Q of the quarter-wave transmission line is found as

$$\phi_Q = -\beta_o\ell = -\frac{\pi}{2} \tag{9}$$

$$\left.\frac{d\phi_Q}{d\omega}\right|_{\omega=\omega_o} = -\ell\frac{\beta_o}{\omega_o} = -\frac{\pi}{2\omega_0} \tag{10}$$

where ℓ is the length of the quarter-wave transmission line.

To yield a broad-band phase difference characteristic, it is required to satisfy the following conditions:

$$\phi_Q|_{\omega=\omega_o} - \phi_R|_{\omega=\omega_o} = \frac{\pi}{2} \tag{11}$$

$$\left.\frac{d\phi_Q}{d\omega}\right|_{\omega=\omega_o} - \left.\frac{d\phi_R}{d\omega}\right|_{\omega=\omega_o} = 0. \tag{12}$$

Using (8) and (10) in (12) gives

$$\frac{Z_o}{2}\frac{Y_p}{\omega_o}\left[\beta_o\ell_p\left(1+\cot^2(\beta_o\ell_p)\right)+\cot(\beta_o\ell_p)\right] = \frac{\pi}{2\omega_0}. \tag{13}$$

We can then reduce (13) to the following equation:

$$\left[\theta_p\left(1+\cot^2(\theta_p)\right)+\cot(\theta_p)\right] = \frac{Z_P}{Z_o}\pi \tag{14}$$

where $\beta_o\ell_p = \theta_p$

Equation (14) can be solved numerically. Under the assumption of $Z_p = 50\ \Omega$ and $\omega_o = 2\pi \times 10$ GHz, the following calculations can be made:

$$\theta_p = 0.6392 = 36.62^\circ \quad C = \frac{Y_p}{\omega_o}\cot(\theta_p) = 0.428\ \text{pF}.$$

The ideal phase-difference characteristic of the proposed 90° phase shifter versus frequency is plotted in Fig. 5. The differential phase shift is $90^\circ + 4^\circ$ from 6 to 13 GHz.

IV. Design of the 5-bit Phase Shifter

The phase-shifter circuit consists of five digital bits corresponding to differential phase shifts of 180°, 90°, 45°, 22.5°, and 11.25°. Each circuit has a two-state sub circuit with two complementary control lines. The circuit provides 32 phase states between 0°–360° in increments of 11.25°. The 180° phase bit circuit switches between PI and/or T-type high-pass/low-pass phase-shift networks using two SPDT MOS switches [14]. The circuit schematic of the 180° phase shifter is shown in Fig. 6. This improves the insertion loss compared with the previously designed 180° phase shifter [13]. The 90° phase bit is designed by the proposed phase shifter, as shown in Section III. The 45°, 22.5°, and 11.25° phase bits use the bridged T-type configuration and are shown in Fig. 7(a). If Q_1 and Q_2 are off and Q_3 is on, the circuit is a form of the T-type low-pass filter, as shown in Fig. 7(b), provided that the off capacitance of Q_1 is small enough to be neglected. The circuit can be analyzed using an ideal equivalent circuit. The inductance (L_1) and off capacitance (C_2) of Q_2 are determined by conditions of the impedance matching and desired insertion phase. S_{11} and S_{22} of a T-type low-pass filter using the transmission matrix are expressed as

$$S_{11} = \frac{jZ_o\left(\omega^2L_1C_2 - 2L_1 + C_2Z_o^2\right)}{\omega(j\omega L_1 + Z_o)(\omega^2L_1C_2 - 2 - jZ_o\omega C_2)} \tag{15}$$

$$S_{21} = \frac{-2}{(j\omega L_1 + Z_o)(\omega^2L_1C_2 - 2 - jZ_o\omega C_2)}. \tag{16}$$

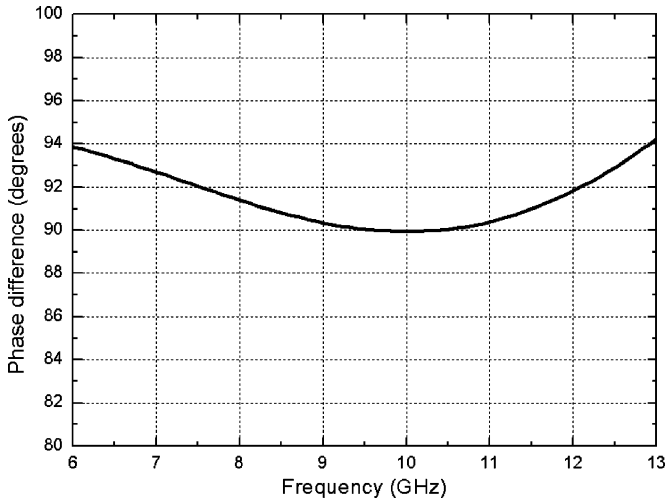

Fig. 5. Ideal phase-difference characteristic of the proposed 90° phase shifter.

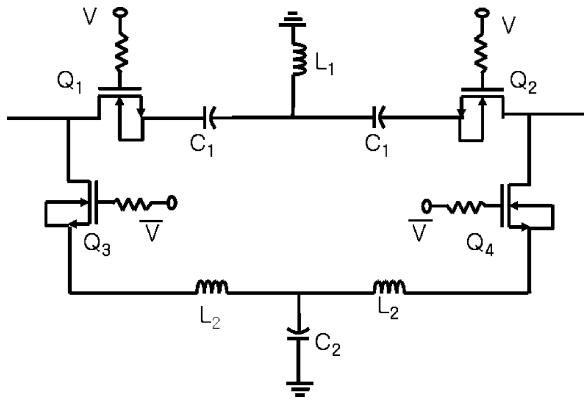

Fig. 6. Schematic of the 180° phase shifter.

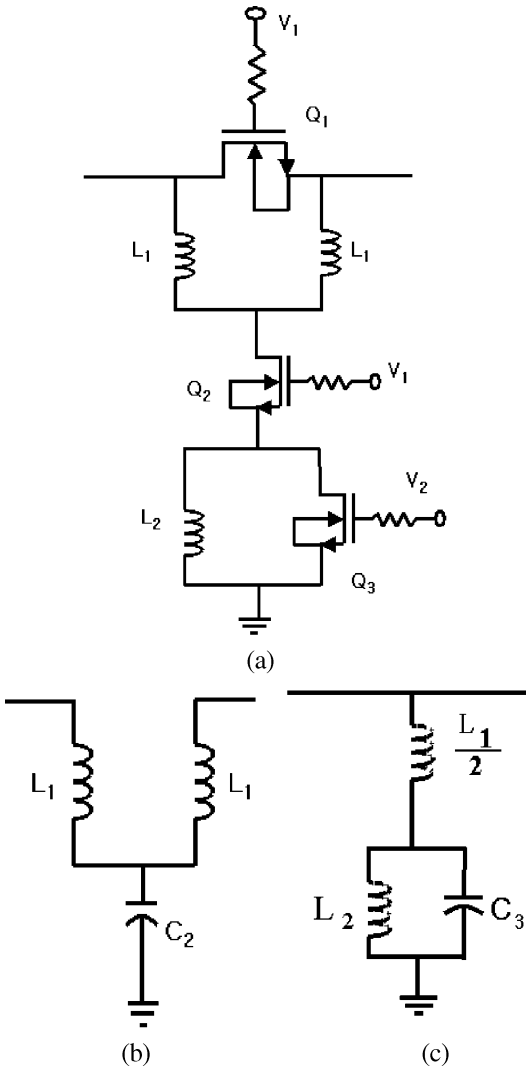

Fig. 7. (a) Schematic of 11.25°, 45°, and 90° phase shifters. (b) Approximate circuit of the low-pass state. (c) Approximate circuit of the parallel resonance state.

When the impedance-matching condition is satisfied at frequency ω_o, the inductance and capacitance required to realize the insertion phase ϕ_o are equal to the following:

$$L_1 = \frac{Z_o \tan\left(\frac{\phi_o}{2}\right)}{\omega_o} \tag{17}$$

$$C_2 = \frac{\sin(\phi_o)}{\omega_o Z_o}. \tag{18}$$

With (17) and (18) satisfied, the derivative of the insertion phase at frequency ω_o using (16) can be represented by

$$\frac{d}{d\omega}\left(-\tan^{-1}\left(\frac{Z_0\omega C_2}{2-\omega^2 L_1 C_2}\right)+\tan^{-1}\frac{\omega L_1}{Z_o}\right)\bigg|_{\omega=\omega_o} = \frac{-2L_1}{Z_o} \tag{19}$$

If Q_1 and Q_2 are on and Q_3 is off, the signal passes through Q_1 while the switch Q_3 is parallel resonated with the inductor L_2. By neglecting the on resistance of Q_1, the circuit is simplified to a parallel resonator circuit. The input admittance of the shunt elements can be written as

$$Y_{\text{in}} = -j\frac{1}{\frac{\omega L_1}{2} + \frac{\omega L_2}{1-\omega^2 L_2 C_3}}. \tag{20}$$

Substituting (20) into (2), the impedance-matching condition and the derivative of the insertion phase at ω_o can be derived in the same way as described in Section III, and expressed in (21) and (22), respectively, as follows:

$$L_2 = \frac{1}{\omega_o^2 C_3} \tag{21}$$

$$\frac{d}{d\omega}\left(\tan^{-1}\left(\frac{Z_o}{\omega(L_1+\frac{2L_2}{1-\omega^2 L_2 C_3})}\right)\right)\bigg|_{\omega=\omega_o} = -C_3 Z_o. \tag{22}$$

Using the equality of (19) and (22), it is necessary to satisfy the following condition for a broad-band phase characteristic:

$$C_3 = \frac{2L_1}{Z_o^2} = \frac{2\tan\left(\frac{\phi_o}{2}\right)}{Z_o\omega_o}. \tag{23}$$

Therefore, the circuit elements are expressed as functions of ω_o and ϕ_o. Under the assumption of $Z_o = 50\ \Omega$ and $\omega_o = 2\pi \times 10$ GHz, the ideal phase-difference characteristics versus frequency are plotted in Fig. 8. Each of the phase bits obtains minimal phase variation around 10 GHz.

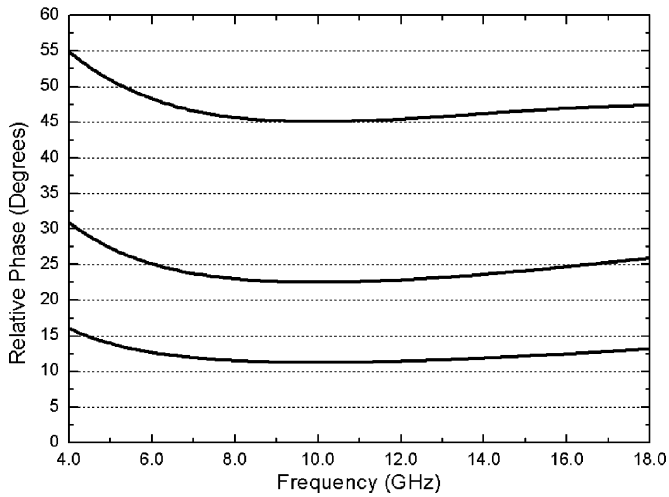

Fig. 8. Ideal phase-difference characteristics of the bridged-T-type phase shifter.

In the design of the phase shifter, each phase shifter is designed to have a minimum 20-dB return loss in order to minimize the interactions between individual bits. All phase bits are designed at the center frequency of 12 GHz.

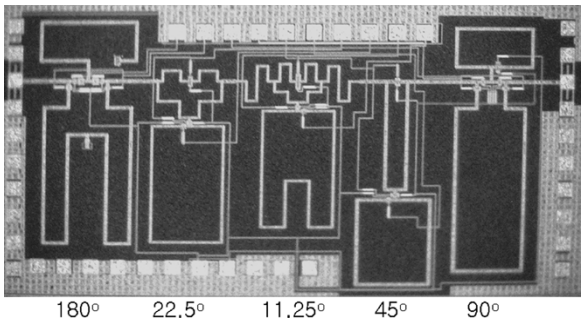

Fig. 9. Chip photograph of 5-bit phase shifter.

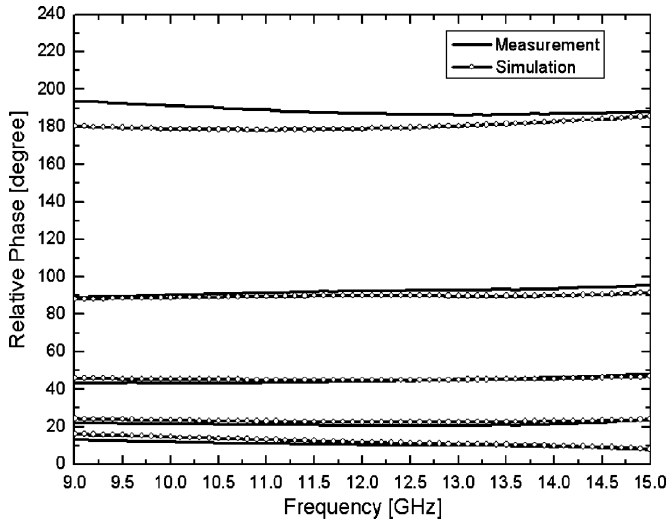

Fig. 10. Phase-difference performance of the 180°, 90°, 45°, 22.5°, and 11.25° phase bits.

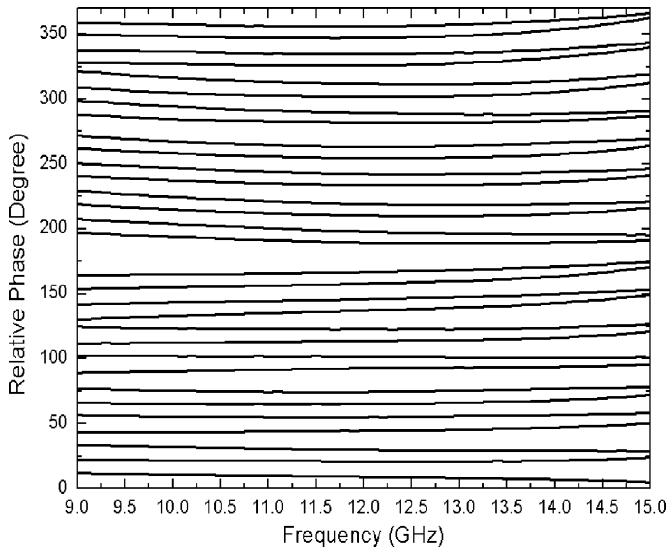

Fig. 11. Measured relative phase shift for all 32 states.

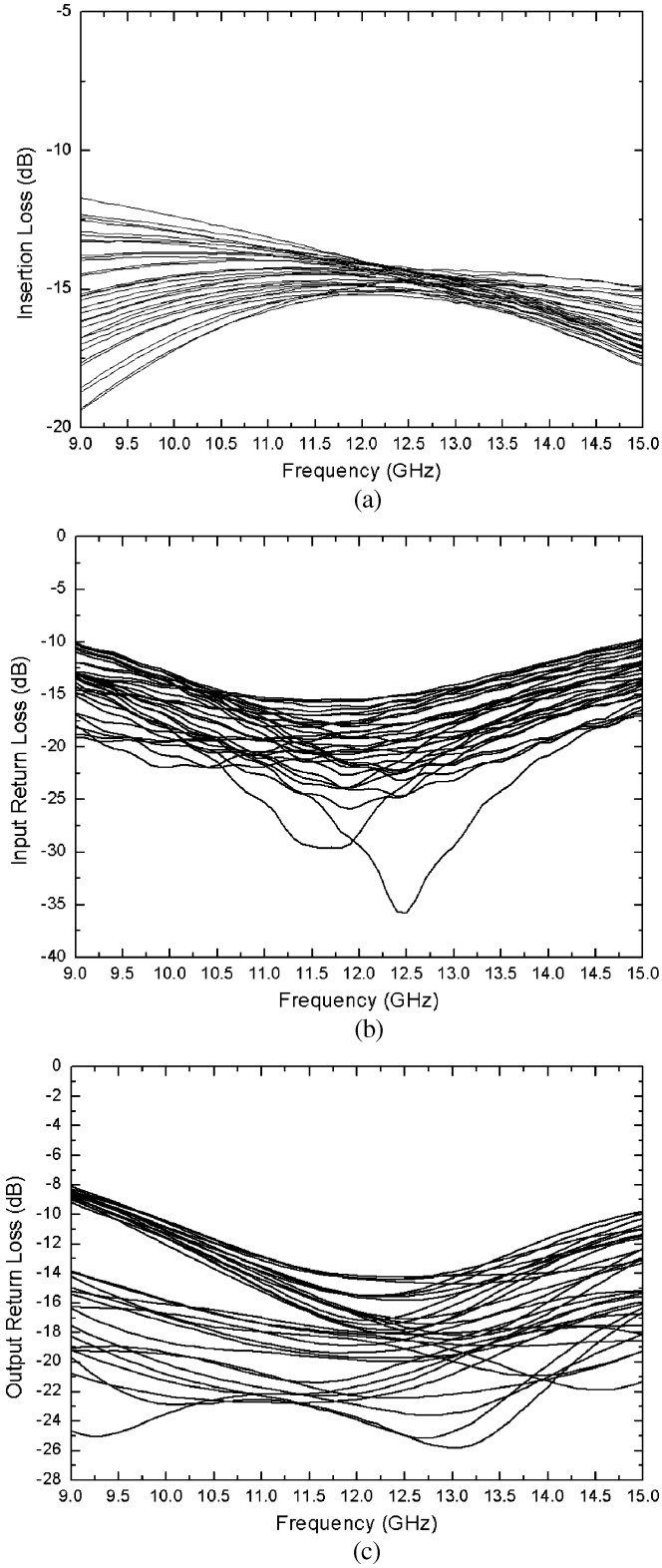

Fig. 12. (a) Measured insertion loss. (b) Measured input return loss. (c) Measured output return loss.

V. Measured Results

The phase shifter was measured using an on-wafer probing system. It was measured with a computer-controlled Agilent 8510 Vector Network Analyzer to a Cascade Microtech probe station. Fig. 9 shows a photograph of a fabricated 5-bit phase-shifter monolithic microwave integrated circuit (MMIC). The die size was 3.1 $\times$ 1.4 mm^2. Fig. 10 shows the simulated and measured relative phase characteristics of the 180°, 90°, 45°, 22.5°, and 11.25° phase bits. The measured and simulated results are in good agreement. The 180° phase shifter has a

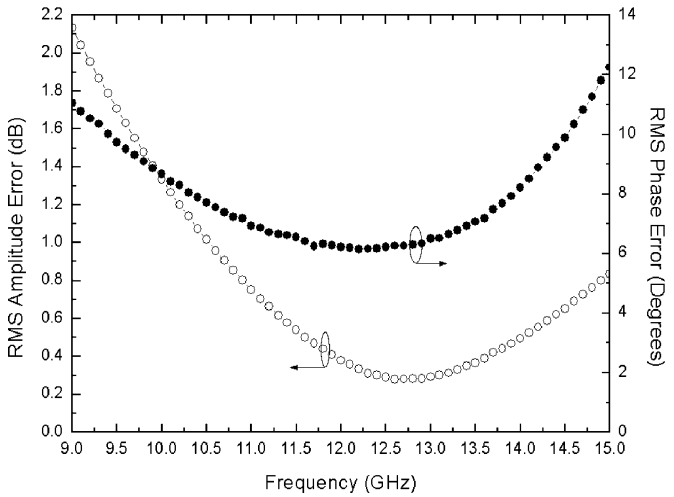

Fig. 13. Measured rms amplitude error and rms phase error.

slight phase error because the phase difference is sensitive to the capacitance or the inductance of the high-pass/low-pass filter. The measured phase difference of the proposed 90° phase shifter is 92.3° ± 3.2° over 9–15 GHz. Fig. 11 presents the relative phase response of the phase shifter for all 32 states over 9–15 GHz. Fig. 12(a) shows the measured insertion loss. The measured insertion loss for the 32 states shows significant state-to-state variation with worst case results of 15.5 dB ± 3.5 dB from 9 to 15 GHz and 16.2 dB ± 1.3 dB from 11 to 15 GHz. At the designed frequency of 12 GHz, the insertion loss is 14.5 dB ± 0.5 dB. The measured input and output return losses are plotted in Fig. 12(b) and (c), respectively. Over the 9–15-GHz band, the measured return losses show worst case results of 10 and 8 dB at the input and output ports. Fig. 13 shows the measured rms phase error and rms amplitude error. The rms phase deviation is less than 12° over the 9–15-GHz band. This error is mainly caused by the difference between the measured and simulated phase difference of the 180° phase bit. The rms amplitude deviation is less than 0.8 dB from 11 to 15 GHz.

VI. Conclusion

A Ku-band 5-bit monolithic phase shifter utilizing a parallel resonator in 0.18-μm CMOS technology has been described in this paper. We have introduced the MOS switch with a body-to-source short and the microstrip line with a first-metal ground for reducing the insertion loss of the phase shifter. A body-to-source short technique improves the insertion loss of a switch by removing the ground path through a lossy silicon substrate. Although the isolation of the switch is not good, the large off capacitance can be used as an element of the phase shifter. The first-metal ground of the microstrip line completely eliminates the field penetration through the silicon substrate, thereby enabling low-loss propagation. The proposed 90° phase shifter has broad-band phase characteristics. All circuit parameters have been derived to obtain a minimum variation of phase difference around the operating frequency. We have also derived the conditions of circuit elements to obtain a broad-band phase characteristic for a bridged-T-type phase shifter. The fabricated 5-bit phase shifter demonstrates an overall rms phase deviation less than 12° from 9 to 15 GHz. An insertion loss of 14.5 dB ± 0.5 dB and return loss less than 14 dB are obtained for 32 states at 12 GHz. The proposed 90° phase shifter has performed a phase difference of 92.3° ± 3.2° over 9–15 GHz.

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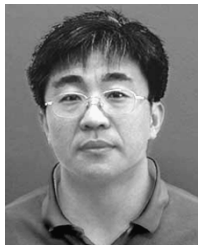

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