A Simple Flash Memory Cell Model for Transient Circuit Simulation

Yong Hoon Kang and Songcheol Hong, *Member, IEEE*

***Abstract*—A simple Flash memory cell model for circuit simulation is presented. The proposed model gives an excellent fitting of dc and transient data and does not require additional simulation time comparing with that of a MOSFET transistor. Effective control-gate voltage method and ideal current-mirror technique are introduced to calculate floating-gate voltage. These allow macro modeling of a Flash memory cell in a circuit simulator.**

***Index Terms*—Erase, Flash EEPROM, Flash memory, Flash model, macro model, program.**

I. Introduction

ONE of the important modeling issues of Flash memory cell is calculation of the floating-gate (FG) voltage. FG voltage determines all the characteristics of Flash memory cell, i.e., current–voltage (*I–V*), programming, and erase [1]. Several models have been introduced to estimate the FG voltage of Flash memory cell, which are classified into two kinds of models. One is capacitive coupling model and the other is Larcher's model. Capacitive coupling models [2] calculate the FG voltages by use of capacitors between FG and other nodes, i.e., FG to drain, FG to source, FG to channel, and FG to control gate. However, this model cannot estimate the FG voltage accurately due to its over-simplifications in the relation of FG and other nodes as fixed capacitors. In reality, the capacitances are complex functions of node voltages [3]. Larcher's model [4] utilizes the charge model of nMOSFET, which includes the effects of several node voltages. The FG voltage is calculated by applying the charge conservation law to FG. Therefore, Larcher's can evaluate more realistic FG voltage, while it requires much more parameters for the physical model of the gate charge. The accuracy in estimating FG voltage is limited by the accuracy of the gate charge model and its model parameter extractions.

In this letter, a new method is presented to calculate the FG voltage accurately without any cost of accuracy and simulation time. In addition, the proposed model itself and the parameter extractions are very simple and it is readily implemented in circuit simulators.

II. Model

A. Effective-Control-Gate (ECG) Voltage

Flash memory cell can be modeled by an equivalent nMOSFET model with the same parameter extraction procedure, although the meaning of parameters may be somewhat changed. Therefore, one can model the *I–V* characteristics of Flash memory cell which has an arbitrary threshold voltage by changing the effective gate voltage. The charge conservation law in FG is expressed by

$$Q_{\rm FG} = C_{\rm CG}(V_{\rm FG} - V_{\rm CG}) + Q_G \tag{1}$$

where $Q_{\rm FG}$ is the charge in FG, Q_G is the charge on the gate of the nMOSFET transistor, $V_{\rm FG}$ is the FG voltage, $V_{\rm CG}$ is the control gate (CG) voltage, and $C_{\rm CG}$ is the capacitance between FG and CG of the cell. By rearranging the left-hand side of (1), we obtain

$$0 = C_{\rm CG}\left[V_{\rm FG} - \left(V_{\rm CG} + \frac{Q_{\rm FG}}{C_{\rm CG}}\right)\right] + Q_G. \tag{2}$$

From (2), therefore, one can see that the effect of an arbitrary charge in FG can be absorbed in the term of CG voltage. If we express the terms of $V_{\rm CG} + Q_{\rm FG}/C_{\rm CG}$ as effective-control-gate (ECG) voltage $V_{\rm ECG}$, (1) can be rewritten by

$$0 = C_{\rm CG}(V_{\rm FG} - V_{\rm ECG}) + Q_G. \tag{3}$$

The ECG voltage of $V_{\rm ECG}$ can be realized with the equivalent circuit as is shown in Fig. 1(b). It consists of $V_{\rm CG}$, $C_{\rm CG}$, and the gate current source i_G for program/erase (P/E). In this circuit, we used the relation of $Q_{\rm FG} = \int i_G {\rm d}t$. This ECG approach is especially useful for transient simulation of Flash memory cell. To simulate time varying behavior of threshold voltage in Flash memory cell, FG charge $Q_{\rm FG}$ must be modeled as a function of time. Without this simple ECG method, one has to model $Q_{\rm FG}$ as a time varying quantity and implement the model into a circuit simulator. These are very difficult and time consuming work. The proposed macro model makes it possible to simulate the transient behavior of Flash memory cell. In previous models (e.g., capacitive coupling model and Larcher's model), one has to obtain the floating gate voltage $V_{\rm FG}$ before he/she achieves gate-current and drain-current, etc. using the voltage. In this case, the accuracy of $V_{\rm FG}$ will affect to the overall accuracy of the model very much. Therefore, to achieve accurate $V_{\rm FG}$ is a key issue of modeling Flash cell. However, the proposed model starts with the drain-current modeling of Flash memory cell using conventional BSIM3 model [denoted by MOSFET1 in Fig. 1(b)]. One can always obtain accurate drain currents at all bias conditions, which influence circuit simulations directly. Then, $V_{\rm FG}$ is obtained more accurately by using an ideal-current-mirror (ICM) technique that will be discussed later.

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The authors are with the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: kangyh@kaist.ac.kr).

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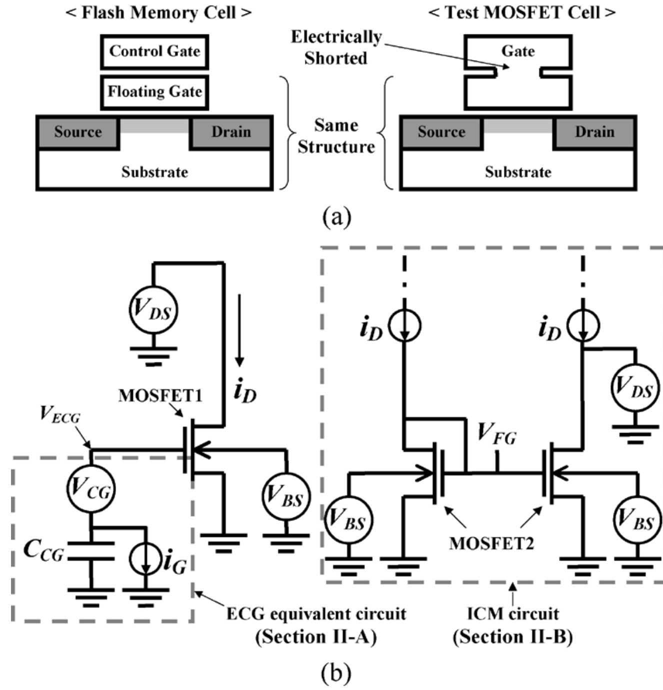

Fig. 1. (a) Sample device structures, and (b) macro circuit model which composed of the ECG equivalent circuit (see Section II-A) and the ICM (see Section II-B). MOSFET1 is the equivalent nMOSFET model of a Flash memory cell, and MOSFET2 is the model of a nMOSFET test structure which is identical with the Flash memory cell except for the electrical short between FG and CG. Both models are based on BSIM3.

B. ICM Technique

The ICM technique is also proposed to calculate the FG voltage easily as in Fig. 1(b). To use this technique, two different sets of nMOSFET model parameters are needed. One is for the Flash memory cell by considering it as an equivalent nMOSFET [named MOSFET1 in Fig. 1(b)]. Another is for a nMOSFET test structure [see Fig. 1(a)] which has an identical structure with the Flash memory cell except for the electrical short between FG and CG [named MOSFET2 in Fig. 1(b)]. And it is known that the gate voltage of MOSFET2 corresponds to the FG voltage of MOSFET1 only if each nMOSFET drives the same drain current under the same drain/body bias conditions. The key idea of this technique is that the floating gate voltage can be represented by the gate voltage of a current mirror. In reality, the drain current is firstly obtained from the nMOSFET circuit of the Flash memory cell as MOSFET1 as in Fig. 1(b). Since the drain current of a MOSFET is a function of drain and gate voltages, the gate voltage of the MOSFET2 is calculated with the same drain current obtained in Fig. 1(b). The gate voltage of current mirror becomes the FG voltage of Flash memory cell. Both current sources of i_D in Fig. 1(b) are ideal and there is no time delay between the current sources of i_D, where a current-controlled/current-source for copying i_D is used. In summary, we can obtain $V_{\rm FG}$ of Flash memory cell by using the ICM technique with additional model parameter set of a nMOSFET test structure. Note that, however, there is one requirement to use it. Two samples for ICM technique should be placed in adjacent as much as possible to exclude the effect of intra-die process variations.

C. FG Voltage in Accumulation Region

According to the previous discussion, one can obtain the FG voltage in the depletion and inversion region of the transistor, but, not in accumulation region. The FG voltage in accumulation region can also be obtained in terms of ECG voltage (in Section II-A). Thus, the same equivalent circuit for ECG voltage as shown in Fig. 1(b) can be used. To derive the equation of FG voltage in accumulation region we used the gate charge model of BSIM3 [5]

$$Q_G = W_{\rm eff,CV} L_{\rm eff,CV} C_{\rm oxe}(V_{\rm FG} - V_{\rm BS} - V_{\rm FB,CV}) \quad (4)$$

where $W_{\rm eff,CV}$ and $L_{\rm eff,CV}$ are the effective channel width and length, respectively, $C_{\rm oxe}$ is the effective capacitance per unit area associated with the tunnel oxide in Flash memory cell, $V_{\rm BS}$ is the body bias voltage with respect to the source bias voltage, and $V_{\rm FG,CV}$ is the flat-band voltage for capacitance model. By substituting (4) into (3), we obtain the FG voltage equation as

$$V_{\rm FG} = \frac{[C_{\rm CG} V_{\rm ECG} + k(V_{\rm BS} + V_{\rm FB,CV})]}{[C_{\rm CG} + k]} \quad (5)$$

where k is $W_{\rm eff,CV} L_{\rm eff,CV} C_{\rm oxe}$. To erase a Flash memory cell, it operates in the accumulation region. If the FG voltage is lower than the voltage of $V_{\rm FG,CV}$, then the FG voltage should be determined by use of (5) and the gate current starts to flow from channel to FG by Fowler–Nordheim (FN) tunneling.

III. Results

As was discussed in previous sections, The proposed model has the following advantages compared to the other models. 1) The model inherently comprehends all the elements that affect to the FG voltage and allows accurate results as long as the drain current model has sufficient accuracy. Since the model utilizes a well-developed drain current model of a MOSFET, the model includes various effects such as the short-channel (SC), narrow channel, avalanche breakdown, channel quantization, and so on. 2) This model is very simple and does not depend on the versions of the MOSFET models. It is composed of the simple circuit with three transistors. 3) The simulation time is almost the same with that of a single transistor.

For the verification of the new model, as was mentioned in Section II-B, two samples (a Flash memory cell and a comparing nMOSFET with a simple stack structure were made by 0.17 μm technology) were prepared, and we extracted the BSIM3 model parameters from the samples. From Spice simulation, it was confirmed that the ICM technique operates very well and we could reproduce the same drain current of MOSFET2 as that of MOSFET1 by applying the calculated FG voltage to the gate of MOSFET2 at the same bias condition. Therefore, it is proved that the FG voltage from ICM technique is correctly calculated. This is valid for both of the dc and transient simulation. In both simulations, however, there can be a small difference which comes from the difference of the drain currents between the MOSFET1 model and the MOSFET2 model. That is because the MOSFET2 model with the calculated FG voltage can not generate such an extremely small drain current of MOSFET1. This makes small differences between the drain current of MOSFET1 and the reproduced drain current of MOSFET2. However, this is

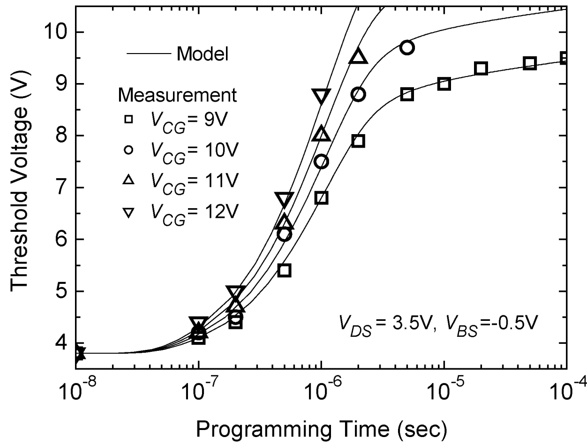

Fig. 2. Programming characteristics show threshold voltages as a function of programming time at various bias conditions. Macro model in Fig. 1 is used for the transient simulation in Spice simulator. Line is from the model and dots are from measurements.

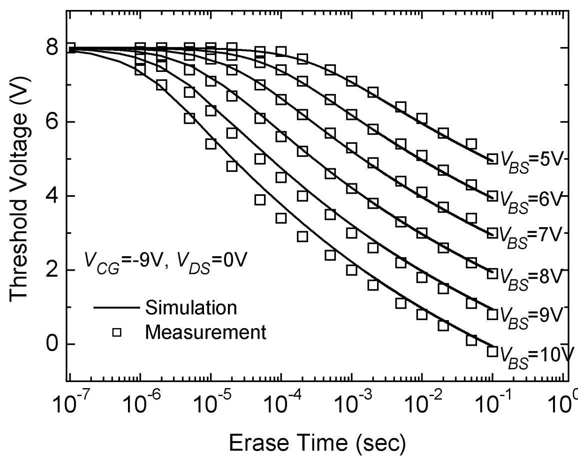

Fig. 3. Erase characteristics show threshold voltages as a function of erasing time at various bias conditions. Macro model in Fig. 1 is used for transient simulation in Spice simulator. Line is from the model and dots are from measurements.

negligible since the difference is only in the lowest current part of subthreshold region. In this letter, for programming model, we used the analytical CHE model [2], [7], [8], and we used the analytical FN tunneling model for the erase model [2], [6].

We can simulate the P/E characteristics of Flash memory cell by using both equations of (6) and (7) with the macro model as shown in Fig. 1(b). Note that, however, for erasing characteristic one must use (5) for FG voltage together with (7). In Fig. 2, we compared the program characteristics of transient simulation with that of an experiment at different CG voltages with the bias of $V_{\rm DS} = 3.5$ V and $V_{\rm BS} = -0.5$ V. We considered the parameters of $P_{\rm inj}$, λ, $V_{\rm D,hot}$, and l_d as a fitting parameter [2], resulting in 1.4×10^{-4}, 5.9×10^{-9} (m), $0.4(V_{\rm FG} - 1.4)$(V), and 6.6×10^{-8} (m), respectively, that are consistent with the previous works [7], [8]. In addition, we have one more parameter must be determined as an initial voltage at the both ends of $C_{\rm CG}$ (see Fig. 1) as $V_0 = Q_{\rm FG0}/C_{\rm CG}$, is the ECG voltage when $V_{\rm CG} = 0$ (see Section II-A), where $Q_{\rm FG0}$ is the initial FG charge before we were starting the P/E measurement of Flash memory cell. The value of $C_{\rm CG}$ was achieved from $A'\varepsilon_{\rm ono}/t_{\rm ono}$, where A' is the area of FG confronting CG, $\varepsilon_{\rm ono}$ is the permittivity of oxide-nitride-oxide (ONO) stack which is in between the CG and FG, and $t_{\rm ono}$ is the thickness of above ONO stack. The figure shows that the simulation results fit very well with the experimental result. We compared also the erase characteristics of simulation with that of measurement, in Fig. 3, at different $V_{\rm BS}$ during the bias of $V_{\rm CG} = -9$ Vand $V_{\rm DS} = 0$ V. For erase simulation, we used the parameters of $\alpha_{\rm FN}$ and m^* as a fitting parameter [2], [6] and the fit results are very good as shown in Fig. 3. After fitting we obtain $m^* = 0.5m_0$, where m_0 is the free electron mass, and $\alpha_{FN} = 8.3 \times 10^{-21}$ (A) as a reasonable value [2], [6].

In summary, we developed a simple and accurate Flash memory cell model by using the new ideas of the ECG method and ICM technique. The model is explained and confirmed with experiment results.

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