Vertically standing carbon nanotubes as charge storage nodes for an ultimately scaled nonvolatile memory application

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Vertically standing single-walled carbon nanotube (SSWCNT)-embedded transistors have been demonstrated for a flash memory application. The performance of the SSWCNT device was compared with a lying SWCNT (LSWCNT) device to verify the directional effect of immobilized SWCNTs. The SSWCNT device shows a better program/erase transient and a threefold enhanced retention characteristics over the LSWCNT device due to the high coupling ratio and the defect immunity based on the isolated distribution and vertical directionality nature of the SSWCNT. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2767211]

Nanoelectronic devices such as field effect transistors and molecular electronic devices have been currently demonstrated by utilizing single-walled carbon nanotubes (SWCNTs) with a shortened length provided as connectors and components.[1–5] Considering the explosive growth of a mobile device market and intrinsic attributes of SWCNTs, one of expected applications of SWCNTs is a nonvolatile memory (NVM) based on a complementary metal-oxide-semiconductor (CMOS) process. For the previous NVM concept using nanocrystals (NCs) embedded into the gate oxide of metal-oxide-semiconductor field-effect transistor (MOSFET), the high thermal stability and proper work function of NC materials was considered.[6–11] By using the SWCNTs as charge storage nodes replacing NCs, they not only have compatibility with a standard CMOS process due to its high thermal stability (>1500 °C) (Ref. 12) but also provide a favorable work function (the general work function of pristine CNT is 4.8 eV) (Ref. 13) in terms of its nonvolatility as a NVM device. Moreover, the work function is tunable via diameter control, chemical doping, and O_2 desorption.[14,15] As mentioned above, with the suitable properties of the SWCNTs as charge storage nodes called a floating gate, another significant factor needs to be considered, i.e., directional effect of SWCNTs on the tunneling dielectric. Two representative advantages can be expected for vertically standing SWCNTs (SSWCNTs) compared to lying SWCNTs (LSWCNTs) which are laterally connected. First one is the enhanced capacitive-coupling ratio (CR) by controlling the length of SSWCNTs. CR is defined as the ratio of the capacitance between the control gate and floating gate to the total gate capacitance, and directly related to the program efficiency. The high CR means reduced operating voltage, and therefore additional device scalability can be followed. The second advantage is an extended retention characteristic due to the high defect immunity by the discrete distribution of SSWCNTs rather than the networks of LSWCNTs. In this letter, we show a NVM structure with vertically standing and discretely dispersed SWCNTs for the extension to an ultimately minimum NVM replacing conventional flash memory.

Figure 1(a) shows the schematic of SSWCNT-embedded MOSFET device. For the fabrication of the SSWCNT device, initially a *p*-type (100) silicon-on-insulator (SOI) wafer was used. The 100 nm SOI on a 370-nm-thick buried oxide was thinned down to 30 nm by iterative oxidation and wet-etch steps to make an ultrathin body. Following this, the active area of the SOI layer was patterned by a wet etch using tetramethylammonium hydroxide (25%) for cell isolation, and a S/D junction was formed by implanting $^{15}P^{+}$ using a patterned photoresist as a mask layer. 4.5-nm-thick tunneling oxide was grown at 850 °C for 9 min, and then the SSWCNTs floating gate was formed on the tunneling oxide by using the wet chemical assembling technique. To stand SSWCNTs on the silicon oxide surface for NVM devices, there have been numerous reports on CNT growth methods on a silicon substrate.[16,17] However, these methods were not suitable for the fabrication of a CNT device due to the im-

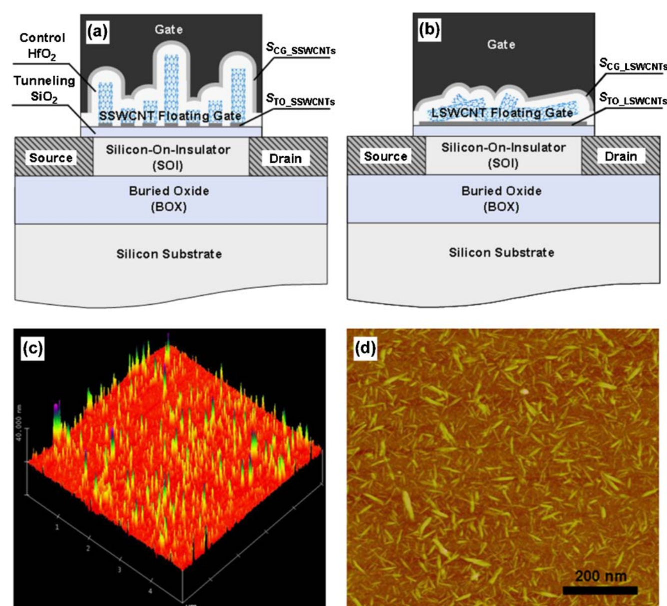

FIG. 1. (Color online) Schematic diagrams of (a) SSWCNT-embedded transistor and (b) LSWCNT-embedded transistor used in this study, and typical tapping mode AFM height images of (c) SWCNTs perpendicularly linked to a silicon oxide surface used as a tunneling dielectric and (d) the lying-down SWCNTs on the silicon oxide surface.

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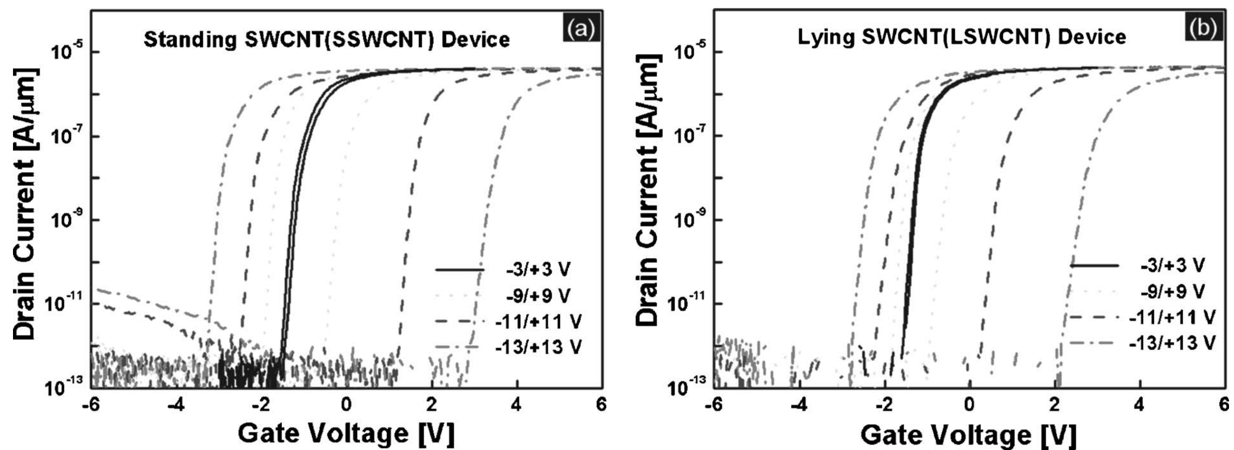

FIG. 2. Electrical memory characteristics. Double-swept I_{DS}-V_{GS} hysteresis of a vertically SSWCNT device (W/L=50/2 μm) (a) and a LSWCNT device (W/L=50/2 μm) (b) at room temperature.

purities, such as the amorphous carbon and metal catalyst particles, and due to the difficulty in the length modulation and sparse distribution for discrete storage nodes of a NVM cell. Recently, we reported that shortened SWCNTs can be organized on a silicon oxide surface vertically.[18] The commercial SWCNTs (1.1 nm in diameter, 0.5–100 μm in length, Sigma-Aldrich) were cut in an acid mixture first and shortened SWCNTs were then perpendicularly aligned on a silicon oxide surface using a wet chemical organization process by combining silanization with the condensation reaction of the carboxylic group with the amino group. The impurities can be cleanly removed by the acid mixture during the cutting process. These approaches are described elsewhere.[18] Subsequently, 30-nm-thick HfO_2 control dielectric was deposited via plasma-enhanced atomic-layer deposition using $Hf[N(CH_3)C_2H_5]_4$ as a hafnium precursor and oxygen plasma to insulate the SSWCNTs conformally by the ALD nature and to create better program/erase (P/E) efficiency considering the high dielectric constant of HfO_2 (ε_r=25). Finally, aluminum was deposited as a gate material by using a rf-sputter procedure and patterned. For comparison purpose, a LSWCNT-embedded control sample was developed to investigate the structural effect of the different SWCNT-immobilized directions on their electrical memory characteristics, as shown in Fig. 1(b).

Figures 1(c) and 1(d) shows tapping mode atomic force microscopy (AFM) (Nanoscope III, Digital Instruments, Veeco Metrology, LLC, CA) height images of SWCNTs perpendicularly linked to silicon oxide for 6 h of immobilizing time and the lying SWCNTs on a silicon oxide surface, respectively. As shown in Fig. 1(c), the isolated needlelike pattern of SSWCNT is clearly observed. The surface density can be modified by controlling the coupling time.[18] Figure 1(d) shows a LSWCNT film on a silanized silicon oxide surface. The AFM images indicate that SWCNTs are mostly in the form of several nanometer bundles, and uniform substrate coverage occurs for these two types of CNT film.

Figures 2(a) and 2(b), respectively, show typical I_{DS}-V_{GS} (I_{DS}: drain current; V_{GS}: gate voltage) curves of the SSWCNT and LSWCNT SOI nMOSFET devices (W/L=50/2 μm, W: width; L: length) under different voltage-sweep ranges from ±3 to ±13 V. For both device types, the clockwise I_{DS}-V_{GS} hysteresis stems from storing different carrier types according to the polarity of the applied voltages. After applying a positive voltage, electrons tunneling through the tunneling oxide from the inversion layer are stored in the SWCNTs, and the threshold voltage increases. For an applied negative voltage, accumulated holes are stored in the SWCNTs, and the I_{DS}-V_{GS} curve then moves in a negative direction. Regardless of the assembling directionality of SWCNTs, it was confirmed that the SWCNTs serve as good charge storage nodes.

To clearly understand the advantages of SSWCNTs devices, the P/E transient characteristics were compared between the SSWCNT and LSWCNT devices (W/L=50/2 μm), as presented in Fig. 3. We found that the SSWCNT device shows more efficient P/E transient characteristics compared to the LSWCNT device under the same program voltage (V_{program}: 11 and 13 V)/erase voltage (V_{erase}: −15 V) and time duration ($\tau_{P/E}$) of applied pulses. This result can be explained by considering the following two factors: the asymmetric electric field enhancement effect and CR. For the former factor, the more sparsely placed SWCNT array of the SSWCNT devices can enhance the electric field with comparison to the SWCNT network of the LSWCNT devices.[19,20] Thus, it shows better P/E efficiency. And, as the latter factor, CR can be expressed as following equation:

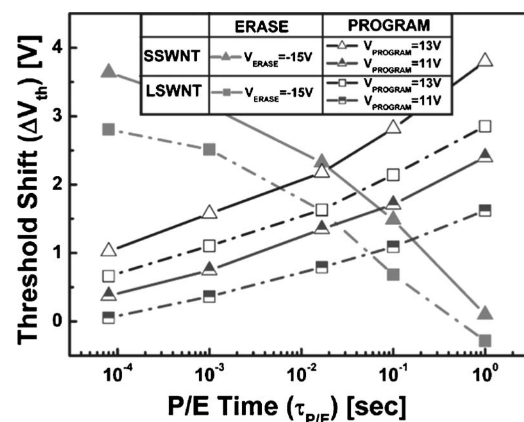

FIG. 3. Program/erase transient characteristics of the SSWCNT devices (W/L=50/2 μm) and LSWCNT devices (W/L=50/2 μm). Pulses of +11/−15 V and +13/−15 V were applied for the program/erase operations.

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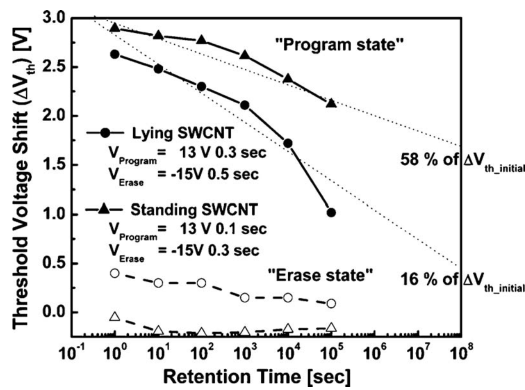

FIG. 4. Retention time characteristics of the SSWCNT devices (W/L=50/2 μm) and LSWCNT devices (W/L=50/2 μm) measured at room temperature.

$$\text{capacitive-coupling ratio(CR)} = \frac{C_{\text{FG-CG}}}{C_{\text{FG-CG}} + C_{\text{FG-sub}}} = \frac{\varepsilon_{\text{CD}}(S_{\text{CG}}/t_{\text{CD}})}{\varepsilon_{\text{CD}}(S_{\text{CG}}/t_{\text{CD}}) + \varepsilon_{\text{TD}}(S_{\text{TO}}/t_{\text{TD}})} \propto \frac{1}{1 + (S_{\text{TO}}/S_{\text{CG}})},$$

where $C_{\text{FG-CG}}$ is the capacitance between a floating gate and a control gate, $C_{\text{FG-sub}}$ is the capacitance between floating gate and silicon substrate, ε_{CD} and t_{CD} are control dielectric constant and thickness. ε_{TD} and t_{TD} are tunneling dielectric constant and thickness, S_{CG} is the surface area of SWCNTs covered by the control gate, S_{TO} is the area of SWCNTs faced with the tunneling oxide. As depicted in Fig. 1, the ratio of S_{TO} to S_{CG} of the SSWCNT device ($S_{\text{TO_SSWCNTs}}/S_{\text{CG_SSWCNTS}}$) is clearly smaller than that of the LSWCNT device ($S_{\text{TO_LSWCNTs}}/S_{\text{CG_LSWCNTs}}$), and this means that the SSWCNT device has a higher CR value than the other from the above equation. In addition, without the reduction of the gate dielectrics, room remains for an enhancement of the P/E efficiency on the foundation of the high CR by modulating the length of the SSWCNTs. This is a predominant advantage of a SSWCNT as a discrete floating gate of a NVM device.

For the nonvolatile memory, it is strictly required that the data retention time must be a minimum of ten years. We studied the retention characteristics of the SSWCNT and LSWCNT devices (W/L=50/2 μm) measured at room temperature. These data were shown in Fig. 4. After ten years, it was found that 58% and 16% of stored charges were preserved for SSWCNT and LSWCNT devices, respectively, from the extrapolation of curves. NVM devices using discrete storage nodes have a high potential to prolong the retention time compared to conventional flash memory using a continuous polycrystalline silicon layer as the floating gate, as previously explained. Although SWCNTs are discrete for both SSWCNT and LSWCNT devices, Fig. 4 shows the clearly different retention characteristics. This trend can be understood by two speculations. Firstly, in the case of SSWCNT device, the CNTs were mutually isolated, thus the SSWCNT device maintains the advantage as discrete storage nodes in a NVM device. However, the LSWCNTs made CNT networks, indicating that adjacent CNTs are bridged with one another. Therefore, in the programed state, there could be a lateral transport of stored charges by the tunneling mechanism and cause the degraded retention characteristic due to the lower level of defect immunity. Secondly, the denser SWCNTs as the charge storage can amplify any change arising from the number of electrons stored per SWCNT.[20] As a result, in a memory window, the threshold voltage difference is narrowed down more quickly in the LSWCNT devices than in the sparser SSWCNT devices. Thus, the LSWCNT devices show poor retention characteristics.

In summary, vertically standing SWCNTs has been demonstrated as discrete storage nodes of nonvolatile flash memory device. A SSWCNT device showed a better P/E transient characteristics and a threefold increase in the retention characteristics over a LSWCNT device due to the high coupling ratio and the high level of defect immunity based on the isolation and vertical directionality nature of the SSWCNT.

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