

Flip Chip Assembly on PCB Substrates with Coined Solder Bumps

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Abstract

The objective of this work is to investigate the flip chip assembly on PCB substrates with coined eutectic solder bumps. In this study, stencil printed 37Pb/Sn solder flip chip bumping and subsequent coining processes were performed on both electroless Ni/Au and OSP (Organic Solderability Preservatives) finished PCBs, and then electroplated 97Pb/Sn flip chip bumped chips were successfully assembled. The structure, assembly processes, and reliability data of this package made of high melting temperature 97Pb/Sn flip chip bumps and eutectic 37Pb/Sn PCB bumps interconnection were investigated. Reliability tests, using thermal cycling (-55 to 125 °C), PCT (Pressure Cooker Test), 85/85 (85 °C and 85 % humidity), and mechanical testing (die shear test) were performed. And daisy chain resistances were also measured to characterize the interconnections and to monitor degradation effects. Cross-section analysis was performed after reliability tests to inspect flip chip solder joints with respect to phase transformation and growing of intermetallic compounds (IMCs) at the solder/PCB interfaces. From the experimental results, it was found that the combined bumps structure of 97Pb/Sn at chip and 37Pb/Sn at PCB was very reliable, and OSP finish was as good as Ni/Au finished PCB for these applications.

1. Introduction

Flip chip technology became a popular chip interconnection technology because of its excellent electrical performance, smallest package size as chip size, and high I/Os handling capability compared with conventional wire bonding interconnection technology [1]. Because of these advantages, flip chip technology has been widely applied for various applications such as telecommunications, computers, appliances, and so on. For flip chip assembly, the need for high-density interconnects in a cost effective flip chip package was the motivation for using organic substrates. However, in order to meet the recent tight pitch demands for chip-area interconnection, it was necessary to construct a new organic package. When organic substrates are used for the recent high pin count flip chip assembly such as microprocessors, substrate bending and warpage problems should be solved to guarantee good flip chip interconnection and high assembly yield [2]. One way to solve this problem is solder flip chip bumping on organic substrates pads, and then coining the solder bumps to guarantee coplanarity of flip chip bump surface on which actual flip chip devices will be attached thereafter.

In this study, coining processes of solder bumps on PCB substrates have been introduced by a specially designed

coining machine; and 97Pb/Sn flip chip bumped devices were assembled on organic substrates with coined 37Pb/Sn solder bumps. After that, reliability was analyzed. The major focus of this work was the investigation of the reliability of 97Pb/Sn chip and 37Pb/Sn PCB combination bumps interconnection in two types of board metal finishes such as Ni/Au and OSP (Organic Solderability Preservatives).

2. Experimental

2.1. PCB substrates with coined solder bumps

The experimental procedure of stencil printing solder bumping on a micro-via PCB and coining process is shown in Fig. 1.

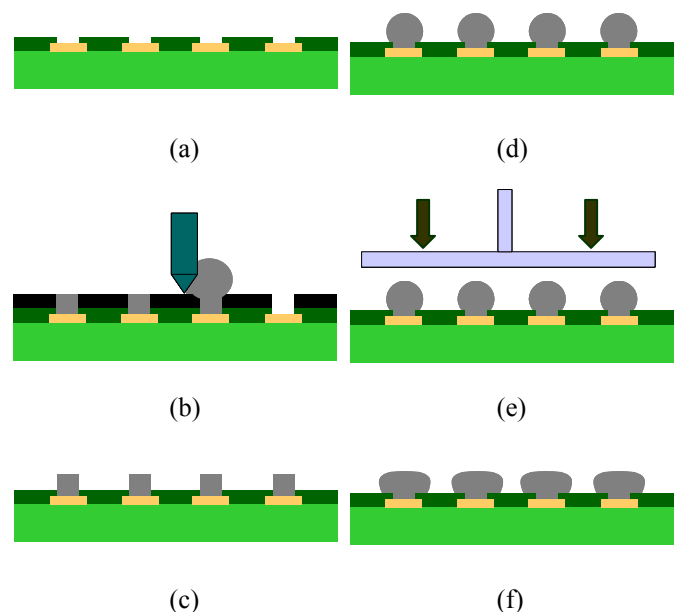


Fig. 1. Fabrication processes of coined solder bumps on PCBs. (a) PCB Board, (b) Stencil Printing, (c) Mask Remove, (d) Solder Reflow, (e) Coining, and (f) Coined Solder Bump.

Fig. 2 (a)-(c) shows PCB pads, eutectic PbSn solder bumps after reflow and flux cleaning, and coined solder bumps on PCB, respectively. The substrate was 37.5X37.5X1.0 mm and it had 2500 area arrayed pads. The opening size of solder mask and pitch of PCB metal pads were 120 μm and 240 μm respectively.

Eutectic PbSn solder paste was stencil printed on both OSP (0.3 μm) and electroless Ni (5 μm)/Au (0.1 μm) finished on electroplated Cu (18 μm) line metallurgy. Reflow steps were classified in 3 stages: flux activation zone at 120°C for 1 min, dwell zone at 220°C for 90 sec, and cooling zone for 90

seconds. After reflow, the diameter of solder bumps was 150 μm and the height above the solder mask was 55 μm .

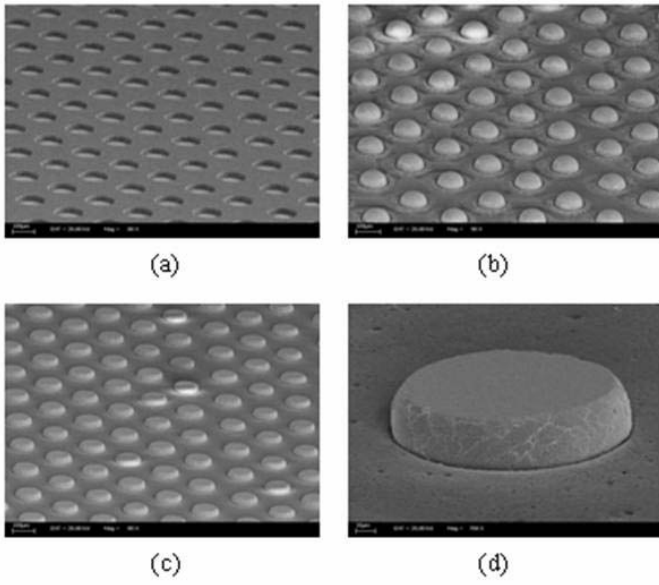


Fig. 2. SEM images of solder bumping and coining process steps. (a) PCB pads, (b) eutectic PbSn solder bumps after reflow and flux cleaning, (c) coined solder bumps on PCB, and (d) a magnified coined solder bump.

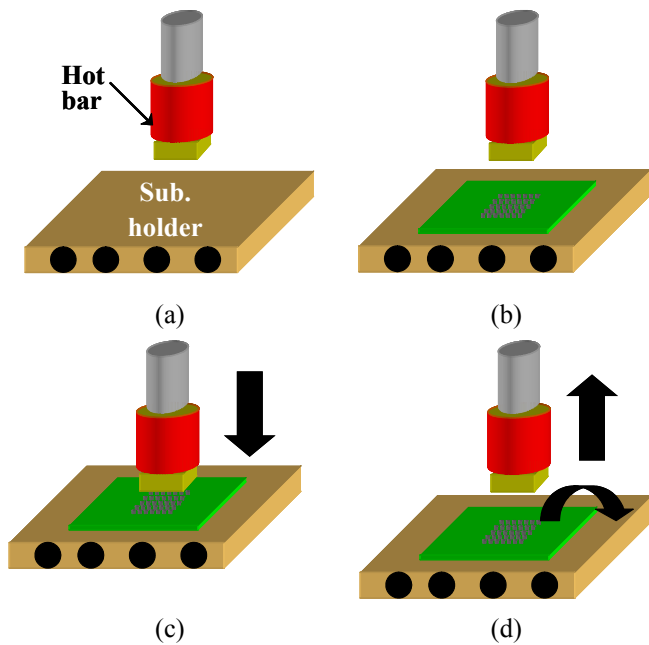


Fig. 3. Coining processes of solder bumps on PCBs. (a) Heating hot bar and substrate holder, (b) placing a substrate, (c) coining, and (d) hot bar up and removing a substrate.

After sawing and singularity of the substrates, the solder bumps on PCB substrates were coined by using a specially designed coining machine. The variables of coining processes were pressure, temperature, and time. In this study, the solder bumps on PCB substrates for flip chip assembly were coined under 100 $^{\circ}\text{C}$, because the applied coining loads become smaller as the process temperature increases for same height

deformation [3]. The coining steps used in this study were illustrated in Fig. 3.

Fig. 4 shows SEM images of coined solder bumps and IMCs at solder/PCB interface. The height and diameter of coined solder bumps were 25 μm and 110 μm respectively. The average co-planarity of coined solder bumps surfaces was about 5 μm . A definition of co-planarity was that the extent of deviation from mean plane of coined solder bumps surface. According to the SEM and EDX analysis, scallop-like smooth Cu_6Sn_5 IMCs were observed at the OSP finish interface. While polygonal shaped Ni_3Sn_4 IMCs were detected in the case of electroless Ni/Au finish.

2.2. Test chips

For test chips, 97Pb/Sn solder was electroplated on TiW (0.2 μm)/Cu (0.4 μm)/electroplated Cu (5 μm) UBM, and reflowed at furnace in hydrogen + nitrogen atmosphere with the peak temperature of 380 $^{\circ}\text{C}$. The 5 μm thick polyimide was applied as a passivation layer on Al metallization. The 15 X 15 mm size chips had 2500 area arrayed bumps of 110 μm height and $10.8 \times 10^{-4} \text{ mm}^3$ in volume.

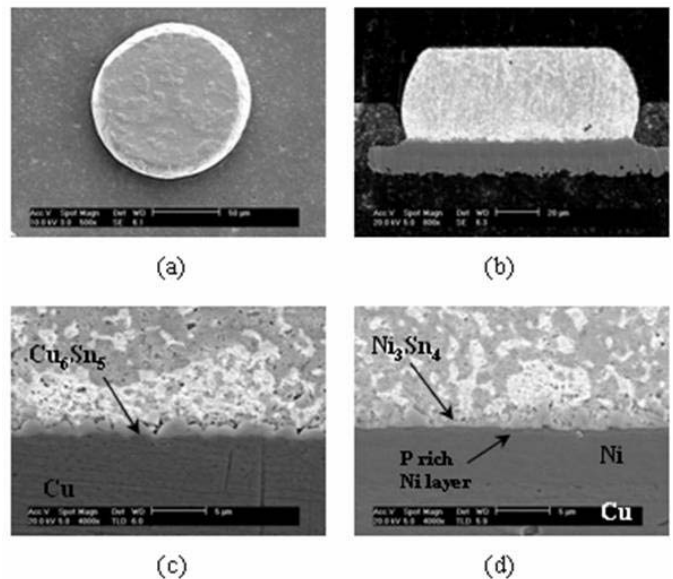


Fig. 4. SEM images of coined solder bumps on PCB substrates. (a) Top view, (b) cross section, (c) IMCs at OSP finish, (d) IMCs at Ni/Au finish.

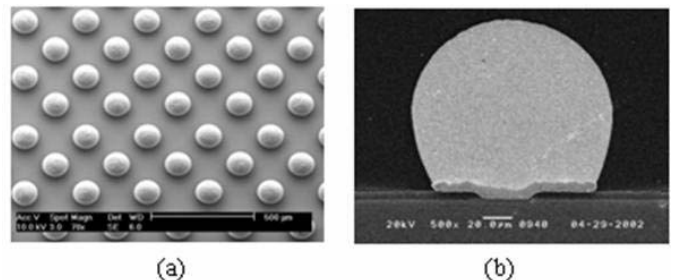


Fig. 5. SEM images of electroplated 97Pb/3Sn solder bumps on test chip. (a) Top view and (b) cross section.

The use of high melting alloys for chip provides a soldering temperature hierarchy, so that 97Pb/Sn solders at chip side do not remelt during flip chip assembly using low

melt solders such as eutectic Pb/Sn solder. The Cu UBM had reacted with the Sn of 97Pb/3Sn solder forming layer type Cu_3Sn intermetallic compound [4]. Fig. 5 shows SEM images of electroplated 97Pb/3Sn solder bumps on a test chip. The diameter of solder bumps after reflow was 135 μm with the minimum pitch of 240 μm .

2.3. Flip chip assembly

Test chip with 97Pb/Sn bumps were flip chip assembled on PCB substrates with 37Pb/Sn coined bumps. At first, a flux was applied on PCB substrates followed by chip placement. Typical reflow condition of eutectic Pb/Sn solder was applied with peak temperature of 220 °C and dwell time of 90 seconds in nitrogen atmosphere. Flux residues were rinsed away using hot solvents after assembly. Hysol FP4549 was used for underfilling. After underfilling, samples were analysed by scanning acoustic microscopy (SAM) to observed voids or delaminations at flip chip joint. Fig. 6 shows a photograph and a SAM picture of as-control flip chip assembled test chip after underfilling. Daisy chain structure for resistance change measurement was formed at the most outer two rows of total 300 bmps interconnection, and the total resistance of daisy chain structure was about 50 Ω .

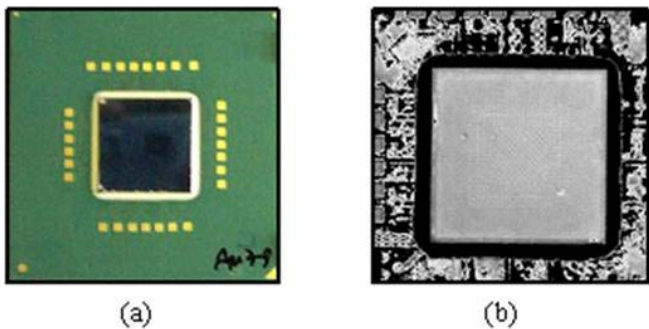


Fig. 6. (a) A photograph and (b) SAM picture of an as-control assembled test.

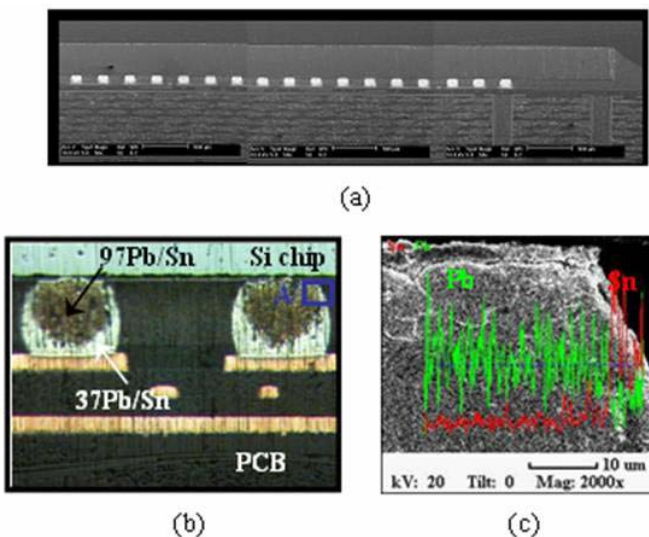


Fig. 7. Cross-section images of assembled flip chip. (a) SEM image, (b) optical image, (c) SEM line scan image of area A in (b).

Cross section analysis was made to investigate the quality of the assembled flip chip joint. Bump joints were successfully achieved resulting in molten eutectic solders on a PCB substrate wrapping around the 97Pb/3Sn solder bumps on a chip after eutectic solder reflow temperature (220°C). Fig. 7 shows cross-sectional images of an assembled package. And IMCs after underfilling were shown in Fig. 8. The thickness and shape of layer type Cu_3Sn IMCs did not change during reflow and underfilling because the melting point of 97Pb/3Sn (320°C) solder was much higher than reflow process temperature. However, the size of IMCs at PCB side increased after reflow process significantly, and the OSP finish showed a thicker Cu_6Sn_5 IMC layer than Ni/Au finish because the electroless Ni effectively limited the growth of the Ni_3Sn_4 IMC at the interface [5].

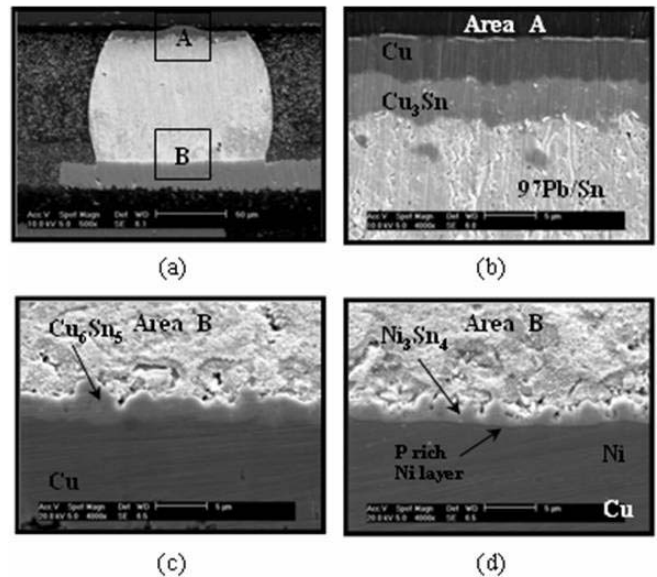


Fig. 8. (a) Cross-section of an as-control 97Pb/Sn - 37Pb/Sn solder joint, (b) IMCs at chip side (area A in (a)), (c) IMCs at OSP finish (area B in (a)), and (d) IMCs at Ni/Au finish (area B in (a)).

2.4. Reliability investigation

2.4.1. Die shear test

Mechanical shear test of assembled flip chip was performed before underfilling. The set up of the die shear test shown was Fig. 9. The PCB was clamped and shear force was applied at the edge of the chips. Cross head speed was 0.2 $\mu m/sec$.

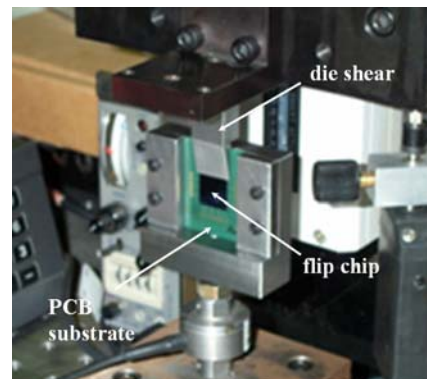


Fig. 9. Die shear tester.

2.4.2. Temperature/humidity Test

Temperature/humidity test was performed at 85°C/85% relative humidity. 10 samples for each PCB surface finishes were subjected to up to 1000 hours. The daisy chain resistance measurements were performed at least every 100 hours. Cross section analysis was made after 1000 hours test.

2.4.3. Thermal Cycling Test

10 samples for each PCB surface finishes were tested in a completely automated air-to-air thermal cycle chamber (-55 and 125 °C) with a dwell time of 15 minutes. After specified number of cycle, all samples were measured electrically.

2.4.4. Pressure Cooker Test

PCT was performed to accelerate the effects of moisture penetration at 125 °C, 2 atm pressure and 100 % humidity.

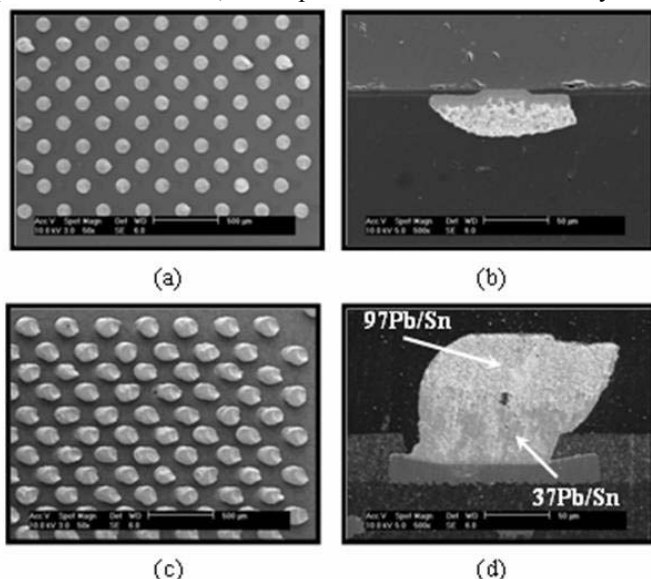


Fig. 10. SEM images of fracture surface and cross sectional images after die shear test. (a), (b) Chip side and (c), (d) PCB side.

3. Results and discussion

3.1. Die shear test

Fractured surfaces and cross sectional images after die shear test were shown in Fig. 10. The fracture occurred at the high lead solder bump itself regardless of PCB finish materials. If the failure occurred through solder interconnection, for the structure of 97Pb/Sn at chip and 37Pb/Sn at PCB combination bumps interconnection, the failure mode was soft solder breaks in high lead solders because the mechanical strength of high lead solder was lower than eutectic PbSn Solder [6].

Failure loads of OSP finished PCB were almost the same as Ni/Au finished PCB, because only ductile fracture mode was occurred through high lead solder bumps.

3.2. Temperature/humidity Test

Daisy chain resistance changes at 85°C/85% RH condition were shown in Fig. 11. All samples reached 1000 hours of temperature /humidity testing without any significant change or failures. Types of PCB metal finish had no noticeable effects on 85°C/85% RH test results.

SEM pictures in Fig. 12 show cross section of solder bumps after 1000 hours at 85 °C/85% RH. No delaminations or voids have been detected inside the sample.

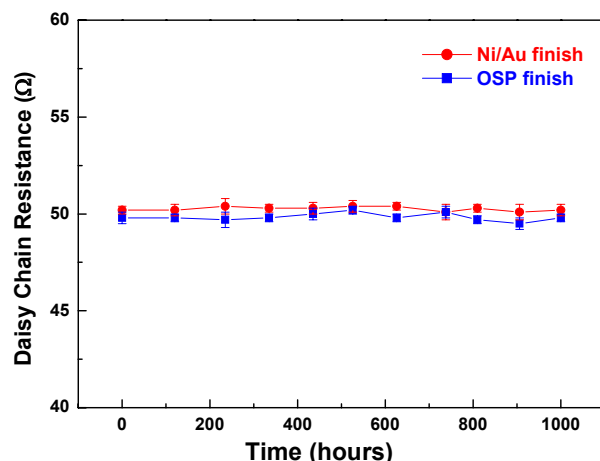


Fig. 11. Daisy chain resistance of test chip under 85°C / 85% humidity conditions until 1000 hours.

There were no changes of IMC phase in case of Ni/Au finish, but thinner layer Cu_3Sn appeared between Cu and the coarsened Cu_6Sn_5 in case of OSP finish. Since Cu_6Sn_5 was thermodynamically unstable with Cu [7], Cu_3Sn formed between Cu_6Sn_5 and Cu after 1000 hours test at 85 °C.

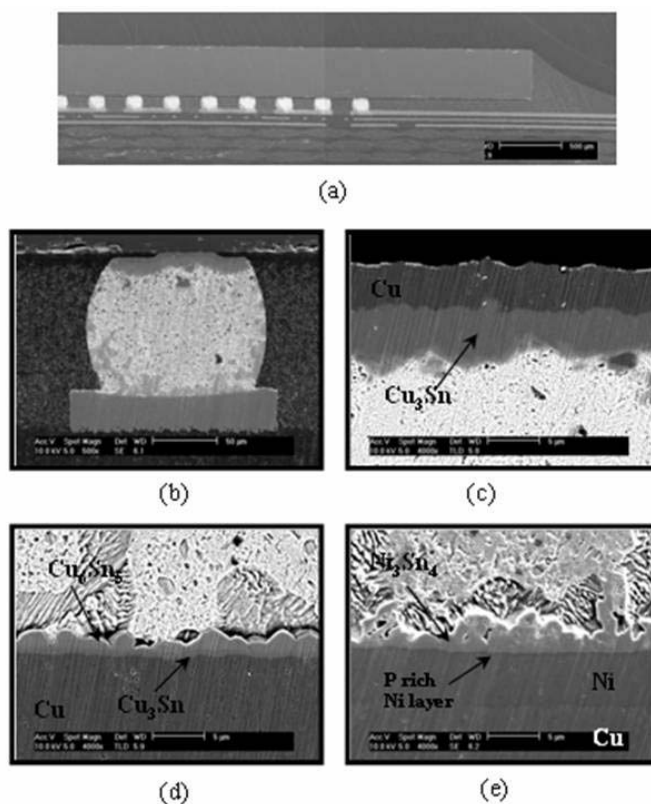


Fig. 12. Cross section of solder joint after 1000 hours 85 °C/85% relative humidity test. (a) Underfill, chip and substrate, (b) a solder joint, (c) IMCs at chip side (d) IMCs at OSP finish, and (e) IMCs at Ni/Au finish.

3.3. Thermal Cycling Test

During thermal cycling test, resistance measurements were performed at least every 100 cycles. Results of daisy chain resistance measurements of were shown in Fig. 13. All samples reached 2500 cycles without any failure or increase of the measured resistance values. It is found that 97Pb/Sn chip and 37Pb/Sn PCB combination bumps interconnection was very reliable under thermal cycle regardless of PCB finish materials.

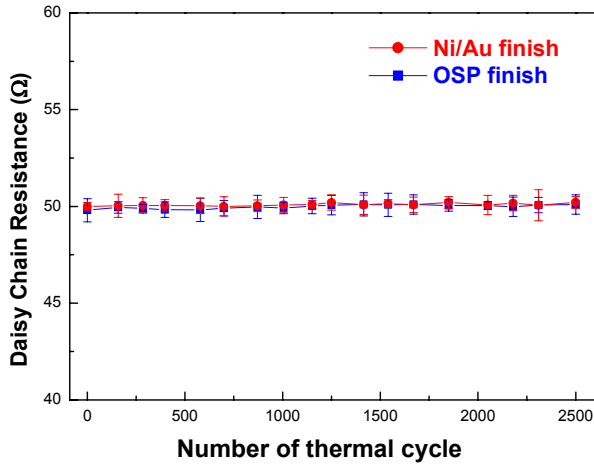


Fig. 13. Daisy chain resistance of test chip under thermal cycling conditions up to 2500 cycles.

Cross sections have been prepared after 1000 and 2500 cycles. After 1000 thermal cycles, slight increase of IMC thickness was observed at chip side UBM and PCB finishes. And about 1.5 μm thickness Cu_3Sn layer appeared between Cu and coarsened Cu_6Sn_5 in OSP finish, because there were solid state aging effects at 125 °C during thermal cycling test. However, the growing of intermetallic phases between solder bump and substrate metalization was not so significant compared to eutectic solder case [8]. Lower Sn composition of solder contacted PCB pads explained the reason why growing of IMCs on PCB side was small. Since interdiffusion of two solders (97Pb/Sn and 37Pb/Sn) was expected during thermal cycling test because of solid state aging effects at 125 °C, the Sn composition of solder contacted PCB pads was lower than initial state. However, growing of intermetallic phases between solder bump and chip UBM was not significant, because the Sn composition of solder contacted chip UBM was small.

As shown in Fig. 14 (a), it was interesting to find coarsened Sn grains in the area of high lead solder bumps. Cross sections after selective etching of Sn or Pb showed that coarsened Sn grains were located inside high lead solder bumps (Fig. 15.). Due to the solid solubility limit of Sn in Pb was 8 wt% at 125 °C [9], Sn of eutectic PbSn solder could not significantly change the composition of high lead solder. After 1000 thermal cycle test, it was found that approximately 7.8 wt% Sn was detected at the top side solder bump (area 1 in Fig. 14.(a)), which was very close to the solubility limit of Sn in Pb at 125 °C.

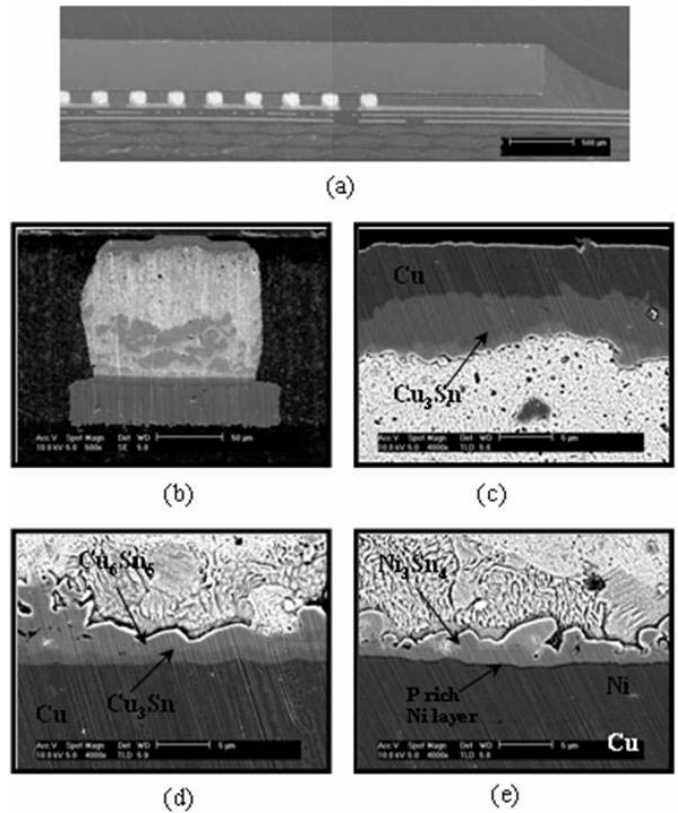


Fig. 14. Cross section of a 97Pb/Sn - 37Pb/Sn solder joint after 1000 thermal cycles (-55 °C /+125 °C). (a) Underfill, chip and substrate, (b) a solder joint, (c) IMCs at chip side (d) IMCs at OSP finish, and (e) IMCs at Ni/Au finish.

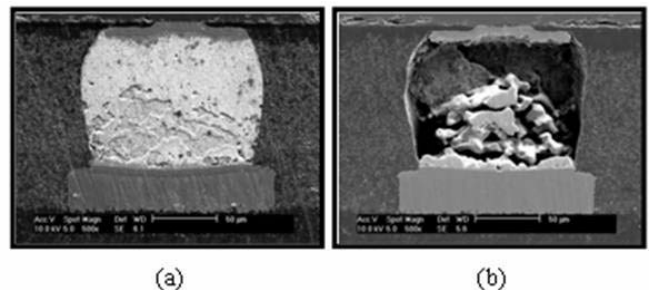


Fig.15. Cross section of a 97Pb/Sn - 37Pb/Sn solder joint after 1000 thermal cycles. (a) Sn etching and (b) Pb etching.

After 2500 thermal cycles, at the chip UBM, thick IMC layer was formed and the remaining Cu thickness was about 3.4 μm as shown in Fig.16 (b). The increase of IMC thickness was also observed at PCB side on both OSP and Ni/Au finish. Both Cu_6Sn_5 and Cu_3Sn compounds showed layer typed morphology because of Cu_6Sn_5 had changed from the scallop type to layer type, which was also observed at eutectic PbSn/Cu interface during solid state aging [10]. The scallop-type morphology was not favorable because of higher interfacial energy between solid solder and Cu_6Sn_5 . During thermal cycling test, metallurgical changes were observed in OSP finished PCB by solid state aging effects at 125 °C. However, these IMC changes at the solder/PCB interface in OSP finished PCB had no noticeable effects on failure up to 2500 thermal cycles.

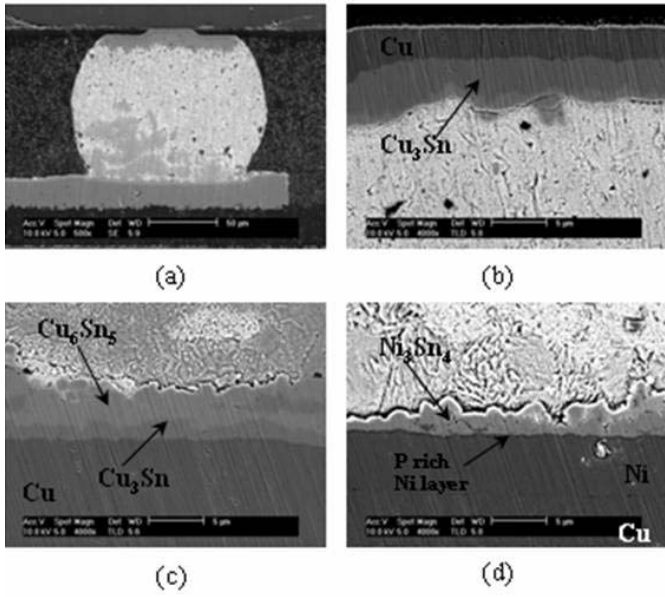


Fig. 16. Cross section of a 97Pb/Sn - 37Pb/Sn solder joint after 2500 thermal cycles (-55 °C /+125 °C). (a) A solder joint, (b) IMCs at chip side (c) IMCs at OSP finish, and (d) IMCs at Ni/Au finish.

3.4. PCT (Pressure Cooker Test)

All samples failed electrically after 168 hours of PCT. Cross section analysis was made after 168 hours PCT to investigate failure sites. Failure was mainly concentrated at the chip corners. Fig. 17 (a) shows a delamination of the underfill from the solder resist at the corner. The moisture absorption during PCT caused the delamination between underfill and solder resist on PCB. And then open circuit fail was caused by Si cratering as shown in Fig. 17 (b).

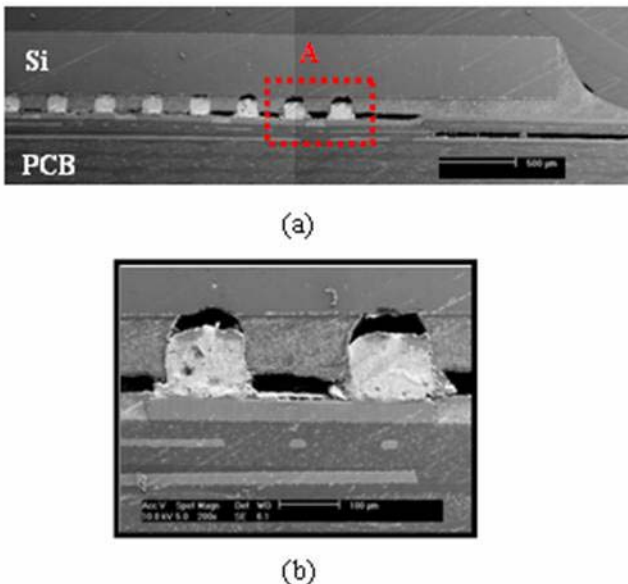


Fig. 17. (a) Cross section of a 97Pb/Sn - 37Pb/Sn solder joint after 168 hours pressure cooker test and (b) a magnified image of area A in (a).

4. Summary

Stencil printed 37Pb/Sn solder flip chip bumping on PCB substrates followed by subsequent coining processes of solder

bumps and low temperature flip chip assembly with high lead solder bumped device were successfully demonstrated as a possible solution for the problems of organic substrate warpage. For flip chip assembly, electroplated 97Pb/Sn flip chip bumped devices are successfully assembled on organic substrates with 37Pb/Sn coined flip chip bumps. The interconnection was successfully performed by the 37Pb/Sn solders on PCB substrate wrapping around 97Pb/Sn solder bumps on chip at eutectic solder reflow temperature (220°C).

For structure of 97Pb/Sn chip and 37Pb/Sn PCB combination bumps interconnection, although there were some changes in intermetallic phases during reliability test, both electroless Ni/Au and OSP finished PCBs were stable under die shear, 85 °C/85 % r.h., thermal cycling and pressure cooker test. The failure mechanism, found after die shear and pressure cooker test was not related to the intermetallic phase formed at solder/PCB interface. The difference of phase, structure, and growing of IMCs on electroless Ni/Au and OSP finished PCBs had no noticeable effects on the failure of 97Pb/Sn chip and 37Pb/Sn PCB combination bumps interconnection.

Acknowledgments

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