Wafer-Level Flip Chip Packages Using Preapplied Anisotropic Conductive Films (ACFs)

Ho-Young Son, *Student Member, IEEE*, Chang-Kyu Chung, Myung-Jin Yim, *Member, IEEE*, Jin-Sang Hwang, Kyung-Wook Paik, *Member, IEEE*, Gi-Jo Jung, and Jun-Kyu Lee

***Abstract*—Recently, wafer-level packaging (WLP) has become one of the promising packaging technologies due to its advantages, such as fewer processing steps, lower cost, and enhanced device performance compared to conventional single-chip packaging. Many developments on new WLP design, material, and process have been accomplished according to performance and reliability requirement of the devices to be packaged [1], [2]. For a lower cost, higher performance, and environmentally green packaging process, anisotropic conductive film (ACF) flip chip assembly has been widely used, such as in ultrafine-pitch flat panel display (FPD) and general semiconductor packaging applications, too. However, there has been no previous attempt on the wafer-level flip chip assembly using ACFs. In this paper, wafer-level flip chip packages using preapplied ACFs were investigated. After ACF prelamination on an electroplated Au bumped wafer, and subsequent singulation, singulated chips were flip-chip assembled on an organic substrate using a thermocompression bonding method. Au-plated bumps were well assembled on Ni/Au pads of organic substrates. The electrical, mechanical properties and the reliabilities of wafer-level flip chip assemblies (WL-FCAs) were evaluated and compared with conventional ACF flip chip assemblies using the thermocompression method. Contact resistance measurement was performed after thermal cycling, high temperature/humidity, and pressure cooker test. ACF joints between electroplated Au bumps and substrate metal pads showed stable contact resistance of 5 mΩ per a bump, strong bump adhesion, and similar reliability behaviors compared with conventional ACF flip chip joints using a thermocompression bonding. As a summary, new wafer-level packages using preapplied ACFs were successfully demonstrated for flip chip assembly. The new wafer-level packages using preapplied ACFs can be widely used for many nonsolder flip chip assembly applications such as chip-on-board (COB), chip-on-flex (COF), and chip-on-glass (COG).**

***Index Terms*—Anisotropic conductive film (ACF) prelamination, flip chip assembly, reliability, wafer-level flip chip packages, wafer-level package.**

I. Introduction

WAFER-LEVEL packages (WLPs) are defined as packages in which interconnections are fabricated on a wafer level prior to wafer dicing. WLPs merge the front-end semiconductor processing and the back-end electronic packaging together, and they are distinguished from a conventional single-chip package (SCP) accomplished by two clear steps divided into semiconductor processing and packaging [1], [2].

Therefore, WLPs have many advantages. All processing steps are performed at a wafer level resulting in reducing materials and processing cost. WLPs are truly chip-size packages (CSPs) of which package size is the same as a chip size. Therefore, WLPs are suitable for further miniaturization and lower cost fabrication of electronic packages [1]–[3].

Flip chip assembly has been widely used to mount IC chips to various substrates. In general, it is divided into two categories; solder bump flip chip and nonsolder flip chip according to their bump materials and assembly methods. Recently, WLPs using solder bumps have been already reported at various commercial applications using underfill materials [4], [5]. However, solder bump flip chip has a drawback of bumping and assembly process complexity and higher production cost, because it requires a number of processes such as solder flux coating, solder bump reflowing, flux cleaning, and underfill dispensing and curing. [6]

Currently, anisotropic conductive films (ACFs) have been widely used in flat panel display (FPD) packaging applications, such as a liquid crystal displays (LCDs) and a plasma display panel (PDPs) in forms of chip-on-board (COB), chip-on-glass (COG), and chip-on-flex (COF). And ACFs are also extensively used at general semiconductor packaging applications with low power and have the potentials for high I/O devices. Comparing with solder bump flip chip, nonsolder bump flip chips assembled with ACFs have many advantages such as lower processing temperature, environment-friendly processes with no flux and solders, fewer assembly steps, and fine-pitch handling capability. However, there has been no previous attempt using ACFs on wafer-level packages.

Conventional flip chip assembly processes using ACFs are shown in Fig. 1. At first, nonsolder bumps such as Au stud, electroplated Au, or electroless Ni/Au bumps are formed on a silicon wafer, and then the nonsolder bumped wafer is singulated into individual dies. For the flip chip assembly, ACFs are cut into a chip size, and a chip-size ACF is prelaminated on a substrate. Finally, a diced chip and an ACF-applied substrate are aligned to each other and assembled by applying heat and pressure using a flip chip bonder. Conventional flip chip assembly processes are being adopting for chip and substrate interconnections using ACFs such as FPD packaging and semiconductor packaging applications.

Fig. 2 shows the assembly processes for wafer-level package using preapplied ACFs. The Assembly process is divided into

Manuscript received October 16, 2006; revised December 24, 2006. This work was supported in part by MIC and IITA through the IT Leading R&D Support Project.

H.-Y. Son, C.-K. Chung, J.-S. Hwang, and K.-W. Paik are with the Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: hyson@kaist.ac.kr).

M.-J. Yim was with the Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea. He is now with the School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

G.-J. Jung and J.-K. Lee are with the NEPES Corporation, Chungchungbuk-do 363-883, Korea.

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Digital Object Identifier 10.1109/TEPM.2007.899151

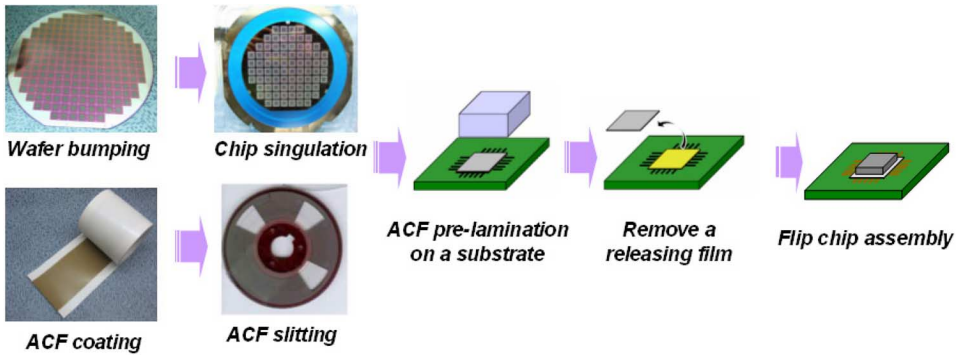

Fig. 1. Conventional flip chip assembly processes using ACFs.

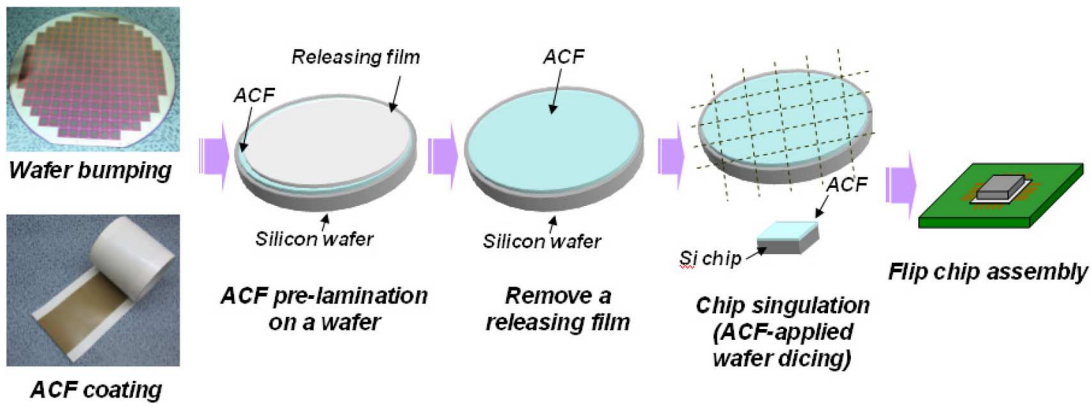

Fig. 2. Wafer-level package processes using preapplied ACFs for flip chip assembly.

three steps as follows: 1) ACF lamination on an entire wafer; 2) wafer dicing into individual dies; and 3) flip chip assembly on a substrate. Comparing with conventional flip chip assembly processes using ACFs, wafer-level flip chip assembly processes can reduce processing steps and time, so eventually it can reduce the total cost of package products.

At the first step, ACFs are laminated on an entire wafer with nonsolder bumps without voids or bubbles formation. At this stage, ACFs should be maintained at the B-stage before curing, because partially cured ACFs may result in deterioration of bump contact resistance and reliability of assembled flip chip joints. In the next step, an ACF-laminated wafer is diced into individual dies using a conventional diamond blade dicing saw. ACF delamination and silicon chipping may occur during the wafer dicing process because a B-stage ACF is much softer than silicon. Therefore, it is important to avoid ACF delamination and silicon fragmental residues on the ACF surface during the wafer dicing process. In addition, moisture absorption control is also important to maintain the reliability of flip chip assembly because of the reported moisture-related ACF failure mechanism [7]. Consequently, the fabrication process of WLP using ACFs should be optimized by modifying ACF lamination, wafer dicing, moisture drying conditions, and so on. Drying conditions are determined at the condition of complete removal of absorbed moisture without additional ACF curing.

At the flip chip assembly, ACF-laminated dies are assembled on organic substrates using a thermocompression bonding method.

WLPs using preapplied ACFs can eliminate some processing steps such as ACF slitting, chip-size ACF cutting, and ACF prelamination. In addition, number of processing steps and cost increase as the size of wafer increase in case of conventional ACF flip chip assemblies. However, they are independent of wafer size in WLPs using preapplied ACFs

In order to apply WLPs using preapplied ACFs for flip chip assembly, the assembled packages should have stable bump contact resistance, strong die adhesion strength, and equivalent reliabilities comparing with conventional flip chip assemblies. Therefore, the object of this study is to demonstrate the WLPs using preapplied ACFs for flip chip on organic boards applications.

II. Experiments

The Si test wafer had a 6-in diameter and a 625 μm thickness. After singulation, test chips had 8 mm $\times$ 8 mm size with 80 peripheral I/Os with 120 μm$\times$ 120 μm size and 1 μm thickness. Au bumps having 100 $\times$ 100 μm size and 20 μm height were electroplated on each Al I/O. Fig. 3 shows test wafers, the pattern design of test chip, and Au-plated bumps. The PCB substrate size was 25 mm $\times$ 25 mm with 8-μm-thick electroless Ni/immersion Au pads on 18 μm Cu. It had 12 Kelvin test structures to evaluate the contact resistance of a single Au bump/ACF joint. Quarter-size wafers were used in this experiment to reduce wafer loss.

ACFs were coated on a releasing film in 8 cm width and 50 μm thickness as shown in Fig. 4. ACFs consisted of polymer

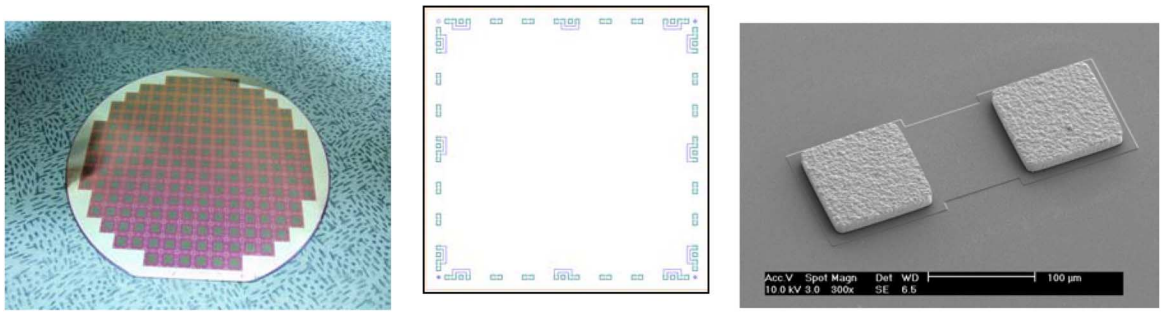

Fig. 3. (a) 6-in test wafer. (b) Test chip design. (c) 20-μm-height electroplated Au bumps.

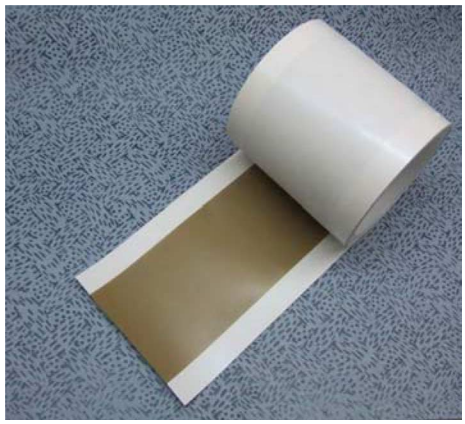

Fig. 4. Wide ACFs for wafer-level package experiment.

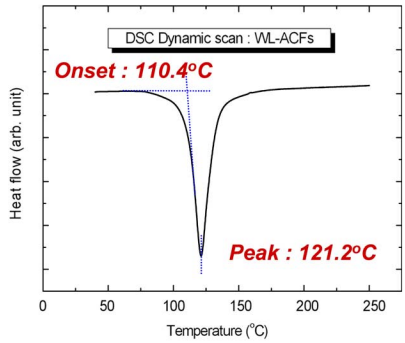

Fig. 5. DSC curing peak of ACFs for wafer-level package.

TABLE I
CURING TEMPERATURES VERSUS CURING TIMES MEASURED BY DSC ISOTHERMAL SCAN

Temperature	160°C	180°C	200°C
Curing time (sec)	26.2	18.7	15.2

resins, such as thermosetting and thermoplastic epoxies, and Au-coated polymer balls with a 5-μm diameter as conductive particles. In order to determine ACF lamination and flip chip assembly conditions, curing behavior of ACFs were investigated by dynamic and isothermal scan analysis using differential scanning calorimetry (DSC). DSC dynamic scan rate was 10 °C/min from 30 °C to 25 0°C to determine ACF curing temperature, and the isothermal scan was performed at 160 °C, 180 °C, and 200 °C to evaluate curing time at each temperature.

ACFs were laminated on test wafers having electroplated Au bumps using a vacuum laminator. The ACF prelamination on test wafers were performed using 80 psi nitrogen pressure for 1 min at 80 °C. ACF prelaminated wafer was diced into individual chips using a diamond blade dicing saw. Before wafer dicing, the releasing film on the ACFs was detached.

The next step was flip chip assembly processes of ACF-laminated chips on PCB substrates. ACF-laminated chip was bonded at 180 °C for 25 seconds with applied bonding force ranging from 20 N (25 MPa) to 80 N (100 MPa) for a chip to determine the optimal bonding force. After flip chip assembly, contact resistances of individual contacts were measured using a Kelvin method and die shear test was measured to confirm electrical and mechanical contacts between Au bumps and substrate metal pads. The reliabilities of WLPs using pre-applied ACFs were evaluated using thermal cycling (-40°C, 15 min $\sim$ $+125$°C, 15 min, 1000 cycles), high temperature/ humidity (85°C/85% RH, 1000 hours), and pressure cooker test (121°C, 2 atm, 96 hours). As a result, WLPs and conventional ACF flip chip assemblies were compared in terms of bump contact resistances and reliabilities of flip chip assemblies.

III. RESULTS AND DISCUSSION

A. Material Properties of ACFs

The understanding of curing behavior of ACFs is important for determining processing parameters. Fig. 5 shows the result of DSC dynamic scan. From the result, the curing process of ACF started at about 107.5 °C, which is the onset temperature of ACF curing. Table I shows curing times at various curing temperatures obtained by DSC isothermal scan. Based on the DSC results, ACF prelamination was performed at 80 °C, which is lower than the onset temperature, and ACF flip chip assembly conditions were determined at 180 °C for 25 s for complete ACF curing.

Thermomechanical properties of ACFs such as coefficient of thermal expansion (CTE), glass transition temperature, and modulus were measured by thermo-mechanical analysis (TMA) and dynamic mechanical analysis (DMA) as shown in Table II.

TABLE II
THERMOMECHANICAL PROPERTIES OF ACFS MEASURED BY TMA AND DMA

$\alpha 1$ (ppm/°C)	$\alpha 2$ (ppm/°C)	T_g (°C)	E' at R.T (GPa)	E' above T_g (GPa)
48	324	133.4°C	2.75	0.0723

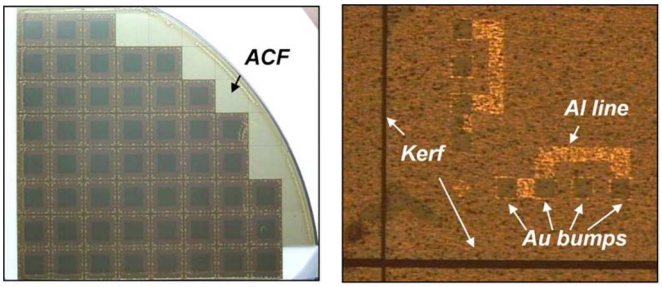

Fig. 6. Optical images of diced ACF prelaminated wafers. (a) ACFs laminated on a test wafer. (b) Void-free ACF lamination near Au bumps and scribing lines.

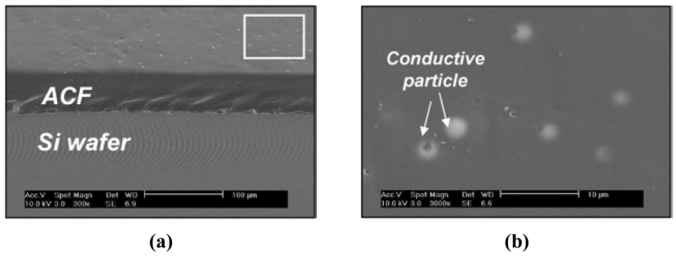

Fig. 7. (a) Tilted view of a diced chip side. (b) ACF top surface near a scribing line after dicing—magnified image of rectangular section of (a).

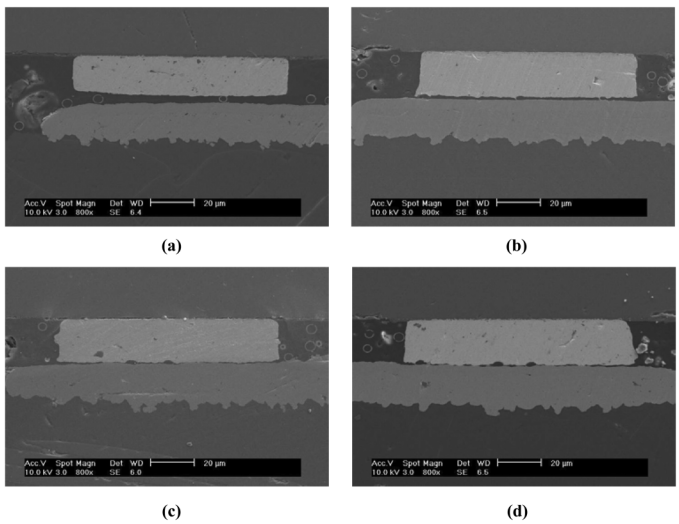

Fig. 8. ACF flip chip joints as a function of bonding forces. (a) 20 N. (b) 40 N. (c) 60 N. (d) 80 N.

B. ACF Prelamination and Wafer Dicing Processes

ACF prelamination on test wafers with electroplated Au bumps and the dicing of ACF prelaminated wafers are two key processing steps for WLPs with preapplied ACFs. In order to fabricate WLPs using ACFs, B-stage ACFs should be laminated without voids between ACF and a test wafer. During the wafer dicing step, several problems such as the moisture absorption, silicon particles residue, and ACF delamination can occur because ACFs are exposed to jet-cooling water during wafer dicing. Fig. 6 shows the optical images after dicing of ACF prelaminated wafer. ACFs were well laminated on entire wafer without voids, and successfully diced without remained silicon particles or ACF delamination. Fig. 7 shows the tilted view of a diced chip side and ACF top surface near a scribing line after the dicing of an ACF prelaminated wafer. No ACF delamination and no silicon particle residues were observed. Usually, silicon fragments frequently remain on a silicon wafer after a mechanical dicing; however, no silicon particles remained on top surface of ACFs in this study. It was presumably due to weaker static electricity between ACF material and silicon particles than that of silicon particles and a silicon wafer. Therefore, moisture absorption into ACFs was the only concern during WLP processes. The amount of absorbed moisture was about 0.5–0.7 wt% of initial weight of ACFs which may deteriorate the reliability of ACF flip chip assembly. It was reported that the glass transition temperature (Tg) of epoxy material decreased as the amount of absorbed moisture increased [8]. The Tg of polymer adhesives is an important parameter that influences thermal cycling reliability of ACF flip chip assembly [9].

C. Flip Chip Assembly Using Preapplied ACFs

A singulated ACF prelaminated chip was flip chip assembled on organic substrates using a thermocompression bonding method. The heating rate on ACF prelaminated chip was 2.8 °C/s from 40 °C to 180 °C, and then maintained for 20 s at 180 °C at various bonding forces of 20 N (25 MPa), 40 N (50 MPa), 60 N (75 MPa), and 80 N (100 MPa). The substrate heating temperature was 80 °C. Fig. 8 shows the cross-sectional views of the ACF flip chip joints as a function of the bonding force. At 20-N boding force, conductive particles were not deformed between Au bumps and substrate Ni/Au pads due to insufficient bonding force. Stable ball contacts between bumps and pads were obtained at 40 N, and then the mixed mode of balls and direct metal contact was obtained at 60 and 80 N. Fig. 9 shows the result of contact resistance measurement at various bonding forces, and this result corresponds well with cross-sectional images in Fig. 8. Above 40 N bonding force, WLPs with preapplied ACFs showed stable bump contact resistance of about 3–7 mΩ. And, as shown in Fig. 9(b), bump contact resistances of WLPs with preapplied ACFs were the same as those of conventional ACF flip chip assembly. In addition, die shear strength of both flip chip assemblies showed about 105–120 kgf/cm^2, and silicon chips were fractured during die shear test.

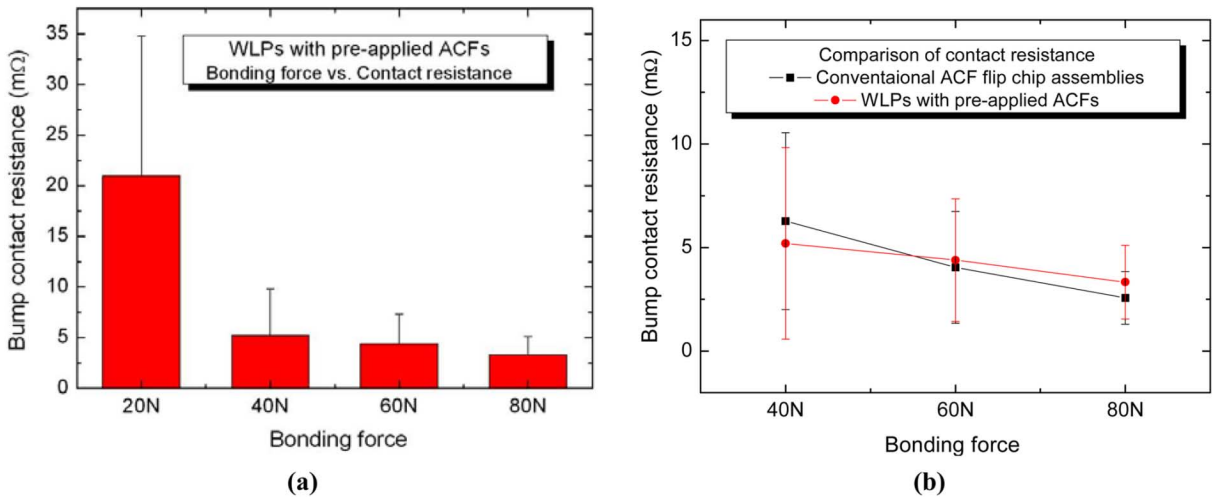

Fig. 9. Contact resistance measurements. (a) WLPs with preapplied ACFs. (b) Comparison of contact resistance between WLPs and conventional ACF flip chip assemblies.

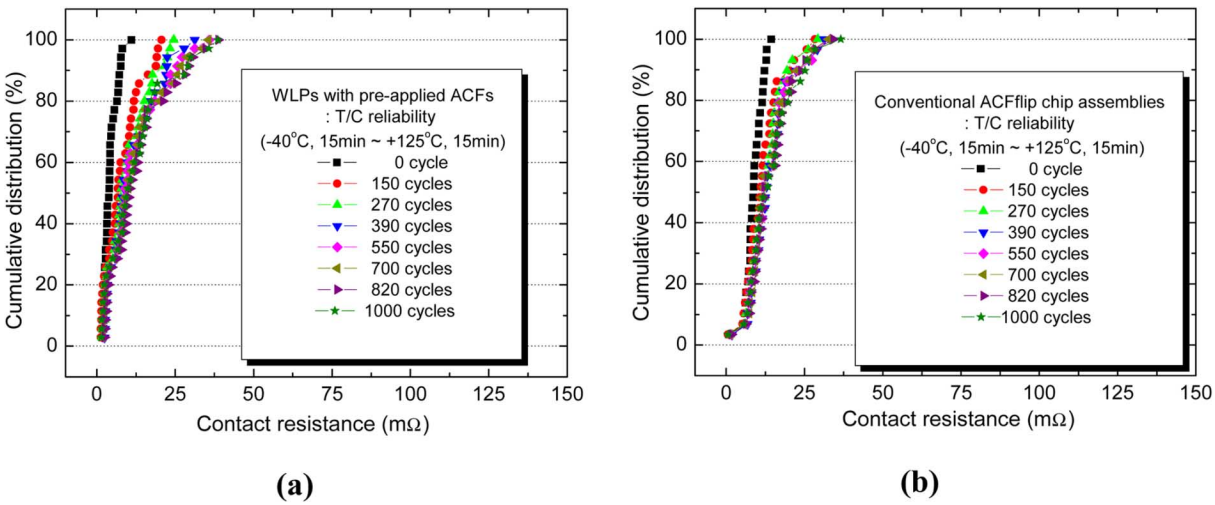

Fig. 10. Thermal cycling test results. (a) WLPs with preapplied ACFs. (b) Conventional ACF flip chip assemblies.

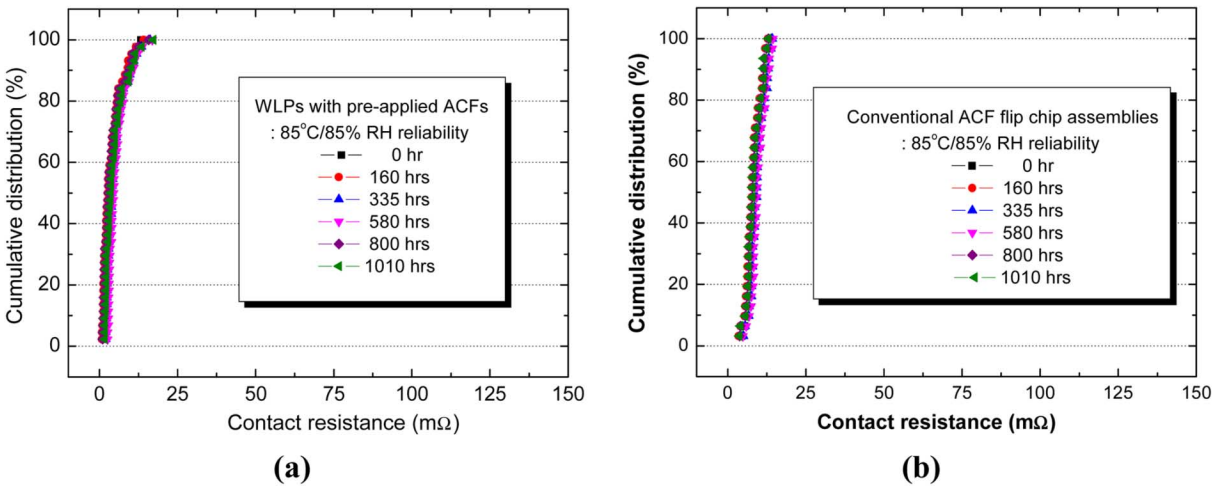

Fig. 11. 85 °C/85% RH test results. (a) WLPs with preapplied ACFs. (b) Conventional ACF flip chip assemblies.

D. Reliability of WLPs With Preapplied ACFs

For the reliability evaluations of WLPs with preapplied ACFs, thermal cycling (−40 °C, 15 min ∼ +125 °C, 15 min, 1000 cycles), high temperature/humidity (85°C/85% RH, 1000 h), and pressure cooker test (121 °C, 2 atm, 96 h) were performed and then compared with those of conventional ACF flip chip assemblies. All flip chip samples for reliability evaluation were assembled at 60-N bonding force.

Figs. 10 and 11 show thermal cycling and 85 °C/85% RH reliability test results for both types of flip chip assemblies. Thermal

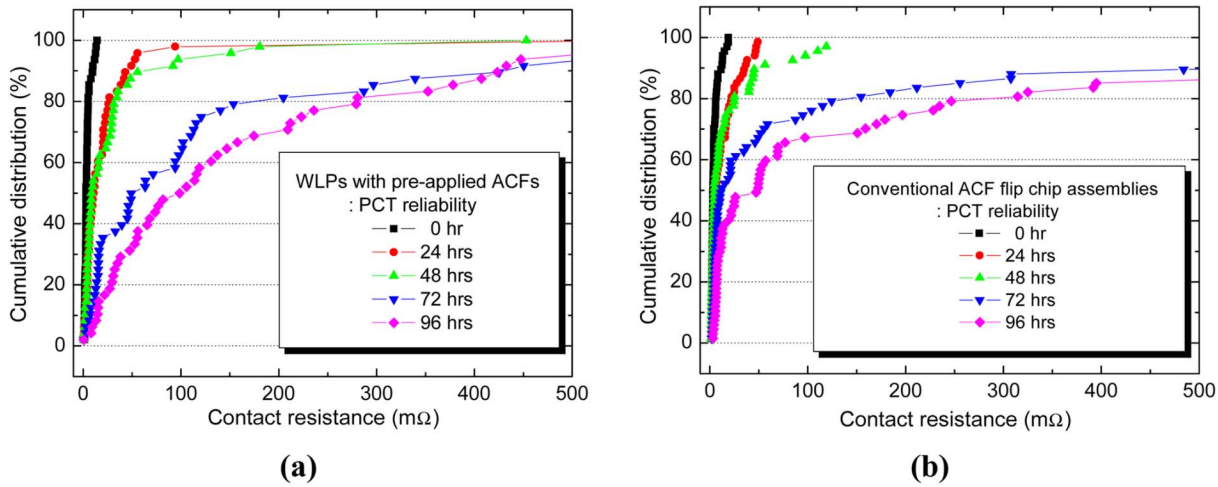

Fig. 12. Pressure cooker test results. (a) WLPs—ACFs. (b) Conventional ACF flip chip assemblies.

cycling and 8 5°C/85% RH reliabilities of WLPs with preapplied ACFs showed almost the same as those of conventional ACF flip chip assemblies. Although wafer-level flip chip assemblies (WL-FCAs) contained the moisture of 0.5–0.7 wt% of ACF weight during WLP fabrication processes, the 85 °C/85% RH reliability was not deteriorated. However, both flip chip assemblies in a pressure cooker test showed poor reliability as shown in Fig. 12. Bump contact resistances of both types of flip chip assemblies similarly increased after 48 h. It was proven that the moisture-related reliability of WLPs with preapplied ACFs was not influenced by the absorbed moisture during wafer dicing process.

IV. Conclusion

In this paper, new wafer-level packages using preapplied ACFs for flip chip assembly were developed and demonstrated. Wafer-level package processes were divided into three major steps: ACFs prelamination on a silicon wafer, ACFs preapplied wafer dicing, and flip chip assembly. In the first step, void-free ACFs were coated on an entire wafer in B-stage by applying nitrogen pressure and heat. And then, ACF preapplied wafer was singulated into a chip without silicon particle residues or ACF delamination. Finally, ACF preapplied chip was flip chip assembled on a PCB substrate by a thermocompression bonding method.

WLPs with preapplied ACFs had uniform bump contact resistance and equivalent reliabilities compared with those of conventional ACF flip chip assemblies. WLP processes using preapplied ACFs can provide cost-effective ACF flip chip assemblies by the reduction of processing steps and times because they can eliminate several processes such as ACF slitting, ACF chip-size cutting, ACF prelamination on a substrate. In addition, these wafer-level processes can be applied on glass or flexible substrates as well as rigid organic boards.

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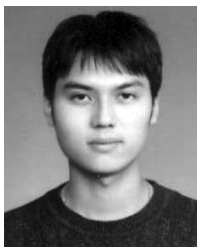
Ho-Young Son (S'06) received the B.S. and M.S. degrees in materials science and engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2001 and 2003, respectively, where he is currently pursuing the Ph.D. degree in materials science and engineering.

His research interests are fine-pitch flip chip interconnection using Cu column bumps and wafer-level package using conductive adhesives. He is a student member of the IEEE Components Packaging and Manufacturing Technology Society.



Chang-Kyu Chung received the B.S. degree in ceramic engineering from Yonsei University, Seoul, Korea, in 2003, and the M.S. degree in materials science and engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2006, where he is currently pursuing the Ph.D. degree in materials science and engineering at KAIST.

His research interests are developing of conductive adhesive materials and its reliability assessment for flip chip packaging.

Myung-Jin Yim (M'04) received the B.S., M.S., and Ph.D. degrees in material science and engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1995, 1997, and 2001, respectively.

During his Ph.D. degree, he was a Visiting Researcher at the IBM T. J. Watson Research Center, Yorktown Heights, NY, from September 2000 to February 2001 and was involved in the project on Pb-free solder and intermetallic compound study. From August 2001 to 2004, he worked at Telephus, Inc., as a Senior R&D Researcher and was in charge of the development of ACFs/ACPs for flat panel displays and semiconductor packaging applications. He was a Postdoctoral Research Associate at the Center for Electronic Packaging Materials (CEPM), KAIST, from 2004 to 2005. He is now a Postdoctoral Researcher at the School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta. He has published more than 50 technical papers in the area of electronic packaging and currently holds seven U.S. patents. His research interests are in polymer nanocomposite and thin-film materials for flip chips, RFID tags, 3-D, micromechanical systems, biopackaging, image sensors, LED devices, and system-in-package (SiP) integration through design, fabrication, performance, and reliability testing and modeling works.

Dr. Yim is a member of the IEEE Components Packaging and Manufacturing Technology Society, Surface Mount Technology Association (SMTA), and American Chemical Society (ACS).

Jin-Sang Hwang received the B.S. and M.S. degrees in polymer science and engineering from Kyungpook National University, Taegu, Korea, in 1993 and 1995, respectively, and the Ph.D. degree in materials science and engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2006.

From January 1995 to 1999, he worked at the LS Cable Corporate R&D Center, where he was involved with the R&D of materials for flat panel displays. From January 2001 to 2006, he worked at Telephus, Inc., as a Senior R&D Researcher and was in charge of the development of ACFs/ACPs for flat panel displays and semiconductor packaging applications. His interests are developing and researching of the polymer nanocomposite packaging materials for flip chips, RFID tags, 3-D, micromechanical systems, biopackaging, image sensor, LED devices, and system-in-package (SiP) integration through design, fabrication, performance, and reliability testing, and modeling works.

Kyung-Wook Paik (M'95) received the B.Sc. degree in metallurgical engineering from the Seoul National University, Seoul, Korea, in 1979, the M.Sc. degree in materials science and engineering from the Korea Advanced Institute of Science and Technology (KAIST), Seoul, in 1981, and the Ph.D. degree in materials science and engineering from Cornell University, Ithaca, NY, in 1989.

From 1982 to 1985, he was with KAIST as a Research Scientist and was responsible for various materials development such as gold bonding wire and nonferrous alloys. After the Ph.D. degree, he worked at General Electric Corporate Research and Development from 1989 to 1995, where he was involved with the R&D of materials and processes of GE high-density interconnect (HDI) multichip module technology and power I/C packaging as a member of the Senior Technical Staff. After he joined KAIST in 1995, he has been working in the Department of Materials Science and Engineering as an Associate Professor. He is currently working in the area of multichip modules, flip chip, micromechanical systems, and display packaging. He was with the Packaging Research Center, Georgia Institute of Technology, Atlanta, as a Visiting Professor from March 1999 to February 2000 and was involved in the educational and integrated passives research programs. He has published more than 60 technical papers in the area of electronic packaging and currently holds 14 U.S. patents and has four U.S. patents pending.

Dr. Paik is the Chairman of the Korean IEEE Components Packaging and Manufacturing Technology Society chapter and also a member of the IEEE and International Microelectronics and Packaging Society.

Gi-Jo Jung received the B.S. and M.S. degrees in electronic and electric engineering from Hongik University, Seoul, Korea, in 2000 and 2002, respectively.

He is an Assistant Manager of the R&D Center, Nepes Corporation, Chungchungbuk-do, Korea. His interests are in developing wafer-level packages and flip chip interconnections.

Jun-Kyu Lee received the B.S. degree in materials science and engineering from Inha University, Incheon, Korea, in 2005.

He is a Memeber of Research Staff with R&D Center, Nepes Corporation, Chungchungbuk-do, Korea. His interests are in developing and researching bumping technology and wafer-level packages.