HIGH VELOCITY N-ON AND N-OFF MODULATION DOPED GaAs/$Al_xGa_{1-x}As$ FETs

T. J. Drummond, S. L. Su, W. Kopp,
R. Fischer, R. E. Thorne and H. Morkoç

Department of Electrical Engineering
and Coordinated Science Laboratory
University of Illinois
1101 W. Springfield, Urbana, Illinois 61801
Phone (217) 333-0722

and

K. Lee and M. S. Shur

Department of Electrical Engineering
University of Minnesota
Minneapolis, MN 55455

ABSTRACT

The purpose of this work is to determine the optimum design parameters of modulation doped $Al_xGa_{1-x}As$/GaAs field effect transistors (MODFETs). An analytical model for MODFETs was developed and used to characterize several 1 μm gate transistors. Extremely high transconductances were obtained and are attributed to large electron saturation velocities in the undoped GaAs. At 300 K transconductances of 250 mS/mm and 235 mS/mm have been obtained for normally-off and normally-on devices respectively. At 77 K a transconductance of 400 mS/mm was obtained for a normally-off MODFET. Using our model to characterize these devices requires the electron saturation velocity to be about 2×10^7 cm/s at 300 K and 3×10^7 cm/s at 77 K.

INTRODUCTION

Modulation doped (Al,Ga)As/GaAs field effect transistors are being investigated for their high current per unit gate length and high transconductances. If MODFETs are to be employed in large scale integrated circuits to increase switching speed, devices should be designed to maximize the transconductance. For this purpose we have developed an analytical model to describe the transfer characteristics of MODFETs (1,2). Although MODFETs are fabricated like MESFETs, charge control by the gate is similar to that of a MOSFET due to the two dimensional nature of the charge carriers.

MODFETs are inherently superior to SiO_2/Si MOSFETs for the following reasons. Both normally-on (N-on) and normally-off (N-off) devices can be fabricated on the same wafer without the need for an implantation or diffusion. Much larger mobilities and electron saturation velocities are obtainable in the undoped GaAs (3,4). The (Al,Ga)As/GaAs heterointerface where the conduction electrons are confined is virtually free of interface states and is smoother than the SiO_2/Si interface. The enhanced low field mobilities of modulation doped structures have been found to have a relatively small effect in determining device performance. The large transconductances observed are the result of the high electron saturation velocity in the GaAs. Using our model we estimate electron velocities of about 2×10^7 cm/s at 300 K and 3×10^7 cm/s at 77 K.

To take advantage of the high electron velocity and increased transconductance, theory indicates that the separation between the gate and the two dimensional electron gas (2DEG) be minimized and charge transfer across the heterojunction be maximized. In this report we demonstrate that this can be accomplished by decreasing the thickness of the undoped (Al,Ga)As spacer layer typically left at the heterointerface.

EXPERIMENTAL

The $Al_{0.33}Ga_{0.67}As$/GaAs heterostructures were grown by molecular beam epitaxy on (100) oriented Cr-doped GaAs substrates. The structure consisted of 1 μm of undoped GaAs, a layer of undoped $Al_{0.33}Ga_{0.67}As$ of thickness d_i, and 600 Å of $Al_{0.33}Ga_{0.67}As$ doped with Si to a level of 1×10^{18} cm^{-3}. Split source field effect transistors were then fabricated with AuGe/Ni/Au ohmic contacts for the source and drain. The gate metal was aluminum. The devices had a gate width of 290 μm and a gate length of 1 μm in a 3 μm channel. Both normally-off and normally-on devices were fabricated from each wafer by controlling the depth to which the Al gate was recessed into the doped $Al_{0.33}Ga_{0.67}As$. Details of the growth and fabrication have been reported elsewhere (5,6).

THEORETICAL

When a doped (Al,Ga)As layer is grown on top of an undoped GaAs layer a 2DEG is formed at the interface due to the difference in the electron affinity of these layers. The amount of charge transfer across the interface is found by equating the charge depleted from the (Al,Ga)As to the charge accumulated in the potential well. A solution is then found such that the Fermi level is constant across the heterointerface. Such a solution has been found using the depletion approximation (7). We have found, however, that for typical doping densities this solution is not accurate enough. The reason for this is that the electrons in the (Al,Ga)As are nearly degenerate leading to a smaller space charge at the edge of the depletion layer. This results in a smaller interface electric field and interface electron density, n_{so}, than predicted by the depletion approximation. We have obtained both numerical and approximate analytical solutions for n_{so}. Our analytical solution (8)

$$n_{so} = \sqrt{N_d^2(d_i+\Delta d)^2+(2\varepsilon N_d/q)(\Delta E_c+\delta(\Delta E_c)-E_{F2})}-N_d(d_i+\Delta d) \quad (1)$$

is obtained using a linearized dependence of the Fermi level on n_{so} (see ref. 1 and 2). Here N_d is the donor density, d_i is the thickness of the undoped (Al,Ga)As layer, $\Delta d = 80$ Å is a constant related to the E_F vs. n_{so} curve (1,2), ϵ is the dielectric permittivity of (Al,Ga)As, q is the electronic charge, ΔE_c is the discontinuity in the conduction band,

$$\delta(\Delta E_c) = -(kT/q)[\ln(1+g'y)+(4/N_d')\ln(1+\tfrac{1}{4}y)] \quad (2)$$

and

$$y = [((1 - \tfrac{1}{4}N_d')^2+4g'N_d')^{\frac{1}{2}} - (1 - \tfrac{1}{4}N_d')]/2g' \quad (3)$$

where

$$N_d' = N_d/N_c, \quad g' = g\exp(q\epsilon_d/kT) \quad (4)$$

and

$$y = \exp(-qE_{F2}/kT).$$

Here E_{F2} is the energy difference between the bottom of the conduction band and the Fermi level in the (Al,Ga)As, N_c is the density of states in (Al, Ga)As, g is the donor g-factor and ϵ_d is the donor ionization energy. Comparison of the exact solution (dotted line) with our analytical expression for n_{so} (solid line) in Fig. 1 illustrates the accuracy of the approximation.

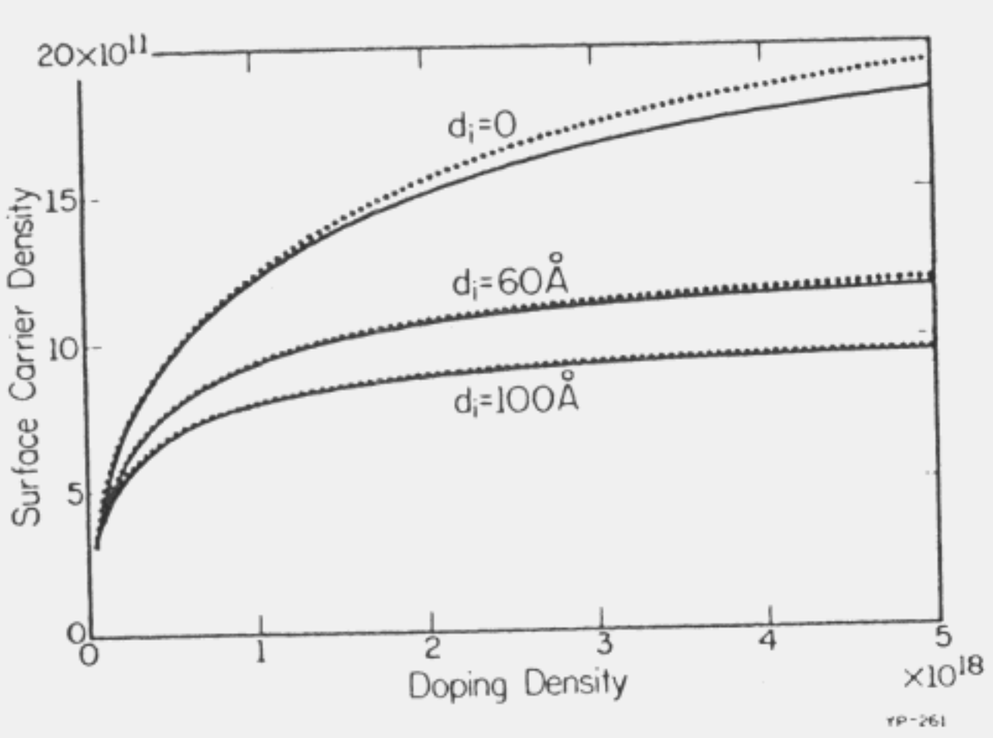

Fig. 1 Interface carrier density, n_{so}, as a function of doping density, N_d, with various undoped (Al,Ga)As layer thicknesses. The dotted line is the exact solution and the solid line is the analytical expression, eq. (1).

The expression for n_{so} given in reference (7) is recovered if one assumes $\delta \to 0$. The actual value of δ is close to -0.1 V. This may explain why the value of $\Delta E_c/\Delta E_g = 0.56$, smaller than a generally accepted value of $\Delta E_c/\Delta E_g = 0.85$ (9) was used in reference (10) for the best fit with the experimental data. These results may be used in modelling MODFETs.

Placing a Schottky gate on the (Al,Ga)As results in a certain amount of depletion beneath the gate. If the (Al,Ga)As layer is thin enough or a sufficiently large negative gate voltage is applied, the gate and junction depletion regions will overlap. The density of the 2DEG is approximately described by the modified charge control model

$$n_s = (\epsilon/q)[(V_g - V_{off})/(d + \Delta d)]$$

where $d = d_d + d_i$, where d_d is the thickness doped (Al,Ga)As layer, $V_{off} = \phi_b - \Delta E_c - \Delta E_{FO}$ where ϕ_b is the Schottky barrier height, ΔE_{FO} temperature dependent parameter of our model and $V_{p2} = qN_d d_d^2/2\epsilon$. Typically ΔE_{FO} is small the order of 20 mV).

The current-voltage characteristics were lated assuming that the current saturates whe electric field at the drain side of the gate ceeds the velocity saturation field $F_s = v_s/\mu$ longitudinal field distribution in the channe low the saturation voltage was described usin Shockley model (7,11). Analytical equations obtained describing the I-V characteristics (cluding the effects of the source resistance) two piece linear (1) and three piece linear (models for the velocity vs. electric field cu Both models take into account velocity satura in the channel. The latter model includes, i addition, the field dependence of the low fie mobility which is especially important at 77 have also calculated capacitance-voltage char istics (2).

Based on our model we have derived the fo ing expression for the maximum "intrinsic" tr conductance of the device, i.e. the transcond tance for $R_s = 0$.

$$(g_m)_{max} = (q\mu n_{so}/L)[1+(q\mu n_{so}(d+\Delta d)/\epsilon v_s L)^2]^{-\frac{1}{2}}$$

where g_m is the intrinsic transconductance pe gate length, μ is the low field mobility, v_s saturation velocity and

$$d = d_i + [2\epsilon(V_{Bi} - V_{off})/qN_d]^{\frac{1}{2}}$$

where $V_{Bi} = \phi_b - \Delta E_c$ is the effective built-i tage. One of the consequences of eqs. (6) an is higher doping of the (Al,Ga)As reduces the mum thickness of the doped (Al,Ga)As beneath gate given by the second term in the right si eq. (7), leading to a higher transconductance

Our results indicate that at small gate l the transconductance becomes nearly independe the gate length due to velocity saturation. reality, an additional enhancement of the tra ductance in short gate structures is possible to ballistic effects. For very short gate le when

$$q\mu n_{so}(d + \Delta d)/\epsilon v_s L >> 1$$

we find $(g_m)_{max}^{short} = \epsilon v_s/(d+\Delta d)$. This expres together with eq. (7) sets an upper limit for transconductance of short gate MODFETs.

At room temperature when μ is only a weak tion of d_i, the transconductance should incre both with a decrease in d_i (in agreement with imental results) and with a decrease in gate Assuming $V_{Bi} = 0.7$ V, $\Delta d = 80$ Å (7), $\mu = 7000$ Vs, independent of d_i at 300 K (3), and $v_s = 10^7$ cm/s we calculate $(g_m)_{max}$ as a function o for a 1 μm gate N-off device. The results ar shown in Fig. 2. The transconductance is cons ably larger for small values of d_i, especiall higher

doping levels. This result is in agreement with our experimental data.

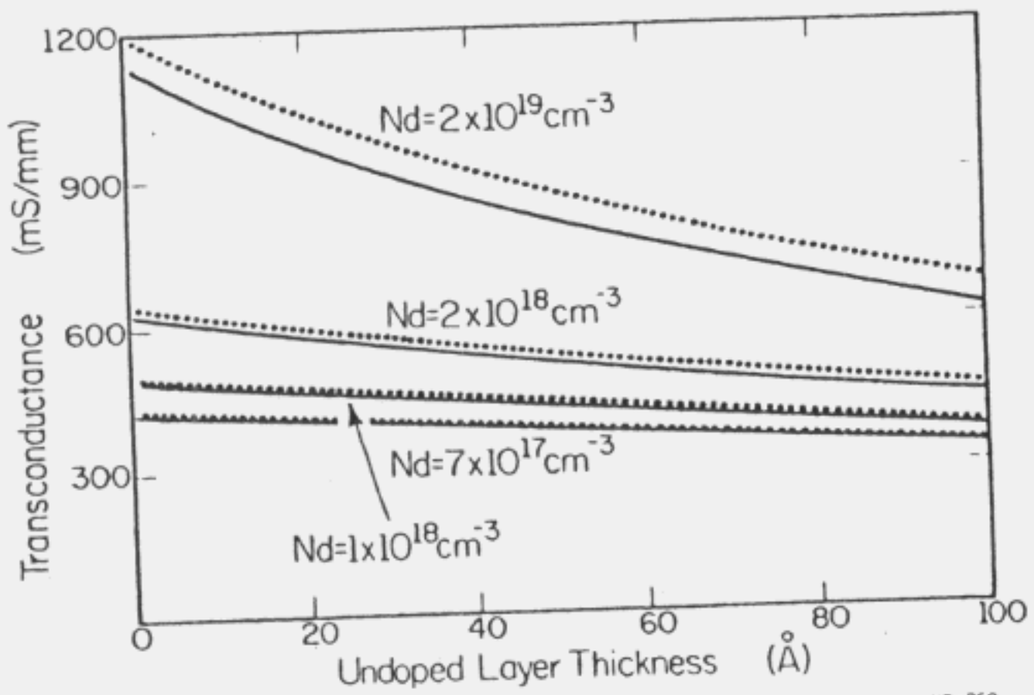

Fig. 2 Transconductance per mm gate as a function of the undoped layer thickness, V_{off} = 0.2 V, μ = 7000 cm^2/Vs, L = 1 μm. For the solid lines the degeneracy of the electrons in the (Al,Ga)As is taken into account and for the dotted lines it is neglected.

RESULTS

Field effect transistors were fabricated from heterostructures with the undoped (Al,Ga)As layer 100, 80, 60, 40 and 20 Å thick. Both current and transconductance increased by a factor of two as d_i was decreased from 100 to 20 Å. At 300 K the maximum values of transconductance were 250 mS/mm and 235 mS/mm for N-off and N-on devices respectively. The maximum currents were 131 mA/mm and 190 mA/mm respectively. The source resistance was 3.5 ohms for the N-on device and 5 ohms for the N-off device assuming an electron saturation velocity of 2 x 10^7 cm/s. The results of fitting the saturation current vs. gate voltage data with our model for a N-on and N-off MODFET are shown in Fig. 3. The data represent experimental points, the dotted and solid lines represent the fits using the two and three piece linear models respectively.

The drain I-V characteristics of a N-off device mounted on a TO-18 header at 300 K and 77 K are shown in Fig. 4. This device, with a 20 Å undoped layer, had a transconductance of 225 mS/mm and a current of 114 mA/mm at 300 K and a gate voltage of + 0.6 V. At 77 K the transconductance increased to 400 mS/mm and the current to 150 mA/mm at the same gate bias. The threshold voltage was observed to shift by about + 0.2 V at 77 K. Bulk (Al,Ga)As doped to 1 x 10^{18} cm^{-3} with Si shows a 25% freezeout of electrons which is sufficient to account for the shift in the threshold voltage. To model the saturation current vs. gate voltage characteristic of this device at 300 K a source resistance of 4 ohms and a saturation electron velocity of 2 x 10^7 cm/s were used. At 77 K the source resistance was decreased to 2.5 ohms and the

electron velocity increased to 3 x 1(

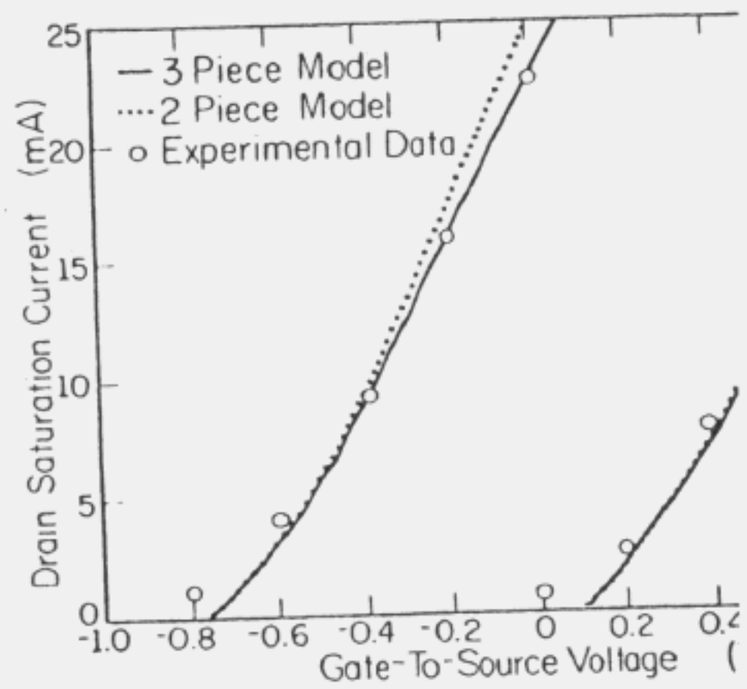

Fig. 3 Saturation current vs. gate v teristics for a N-on (d_i = 40 (d_i = 20 Å) MODFET showing th fit to the experimental data.

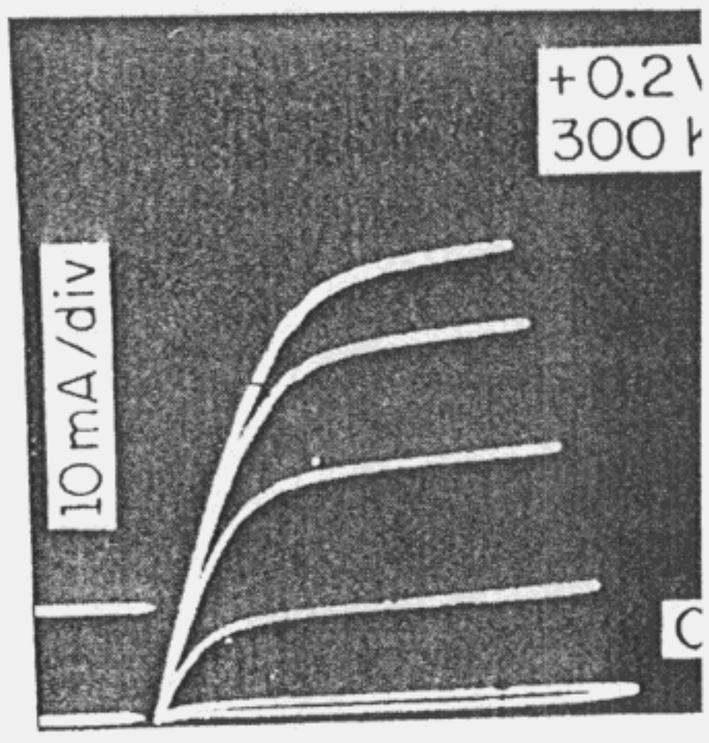

Fig. 4 Drain I-V characteristics o (d_i = 20 Å) at 300 K (top)

fit the theoretical curve to the experimental data. These velocities are in extremely good agreement with predictions based on pulsed measurements (5).

As a final note, small signal microwave measurements were performed on a normally-off MODFET with a 60 Å undoped (Al,Ga)As layer. Although a maximum available gain as high as 10.8 dB was measured at 10 GHz the typical figure was 9 dB at 8 GHz.

CONCLUSIONS

The parameters optimizing the modulation doped field effect transistors (MODFETs) have been investigated. In accordance with the predictions of an analytical model developed for MODFETs, reducing the separation between the gate and the 2DEG increases the transconductance significantly. Device performance for short gate MODFETs is then limited by the electron saturation velocity rather than the mobility. Electrons at the heterointerface exhibit saturation velocities of about 2×10^7 cm/s at 300 K and 3×10^7 cm/s at 77 K.

Fabricating a series of 1 μm gate MODFETs with progressively thinner undoped (Al,Ga)As spacer layers resulted in higher transconductances and larger currents. Maximum transconductances at 300 K were 235 mS/mm and 250 mS/mm for N-on and N-off devices respectively. At 77 K a normally-off device had a transconductance of 400 mS/mm. By using a larger mole fraction and higher doping level our theory predicts that intrinsic transconductances of over 900 mS/mm may be possible.

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