Loop-Based Inductance Extraction and Modeling for Multiconductor On-Chip Interconnects

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***Abstract*—An efficient extraction and modeling methodology for self and mutual inductances within multiconductors for on-chip interconnects is investigated. The method is based on physical layout considerations and current distribution on multiple return paths, leading to loop inductance and resistance. It provides a lumped circuit model suitable for timing analysis in any circuit simulator, which can represent frequency-dependent characteristics. This novel modeling methodology accurately provides the mutual inductance and resistance as well as self terms within a wide frequency range without using any fitting algorithm. Measurement results for single and coupled wires within a multiconductor system, fabricated using 0.13 and 0.18 μm CMOS technologies, confirm the validity of the proposed method. Our methodology can be applicable to high-speed global interconnects for post-layout as well as prelayout extraction and modeling.**

***Index Terms*—Electromagnetic coupling, inductance, integrated circuit interconnections, modeling.**

I. Introduction

With the advancement of CMOS technology into nanometer feature size and multigigahertz frequency regime, on-chip signal integrity is becoming a major concern in integrated circuit design. Increase in interconnect delay and crosstalk together with reduction of threshold voltage of transistors have significantly worsened design margins. Therefore, accurate understanding and modeling of the parasitic parameters of interconnects have become more critical than ever. For fast full-chip-level extraction and reduced design cycle, it is important to develop a compact and accurate model to estimate interconnect behavior.

On-chip inductance impacts the behavior of interconnects, especially global wires, in a number of ways [1]–[5]. Inductive signal overshoots and ringing effects result in high gate input voltages which cause thin-oxide reliability problem and circuit malfunctioning. Signal wire delays are increased and signal transition times are decreased with increasing inductance. Mutual inductance degrades signal integrity by injecting inductive noise on victim lines. Inductance in the power grid can also increase switching noise, which is proportional to the time derivative of current, and significantly impacts power supply integrity.

In addition to numerically solving Maxwell's equations, there are basically two approaches in inductance extraction and modeling, partial, and loop inductance methods [6]–[16]. The partial equivalent elements circuit (PEEC) [6] method based on partial inductances was proposed to overcome the difficulty in finding complete current loops in a real chip environment. In this approach, each conductor is segmented and for high frequencies, further subdivided into filaments. The partial self inductance for each wire filament and mutual inductances between all filaments are needed for accurate extraction and modeling. Since the PEEC model results in a huge number of circuit elements and dense inductance matrix, it requires substantial computing resources even though several techniques such as matrix sparsification and model-order reduction have been developed to alleviate the problem [7]. Loop inductance approach is preferred for fast inductance estimation for well-designed structures such as shielded clock nets [11]. Such approach is more conceptual because inductance is a loop quantity, and requires determination of the current return path in the extraction stage, which is a challenging task in real chip environments.

Several papers have introduced loop-based inductance models and yielded good results for a wide frequency range [12]–[16]. Krauter [12] and Sim [13] have considered multiple ground returns in high-speed on-chip interconnects, and efficiently modeled loop proximity effect. The models predict well the inductance behavior of a single signal wire in a realistic power/ground grid environment. Huang [14] used some fitting parameters and a simplified empirical formula for proximity effect, but the model is suitable for only up to a few gigahertz. Kleveland [15] measured S-parameters of a test circuit which mimics a real chip environment including the power grid and active drivers. The empirical formulae and circuit model were derived from measurement, and they are only applicable to that test chip. Limiting the current return path to the nearby power or ground line is another method to reduce the complexity of the problem [16], but is inaccurate except for very high frequencies. As we will show in Section III, only about 70% of return current resides in the first grid next to the signal wire,

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and thus more grids need to be taken into account for accurate extraction.

The methods mentioned thus far are all for single-wire interconnect models. Tight design margins and high packing densities, however, demand an extraction method for mutual inductance to accurately determine delay and crosstalk. Extraction and modeling of mutual inductance require inclusion of the interaction between two closed loops, making it difficult to implement in multiconductor interconnects.

The most significant advances in wide-band modeling of coupled interconnect lines have been made in a transmission line context [9], [17]–[19]. The resulting multiline transmission line methodologies are intended for pre-layout modeling as well as for CMOS technologists to evaluate various process options and optimize the process. For example, in [19], a curve fitting algorithm is used to fit the simulation results to a circuit model, and its applicability is limited to generating parameterized models for designers, which can be used in analysis only under well-defined and controlled chip environments. Another method as presented in [17] is to assign a dedicated return path next to the signal wire or ground plane, and develop semi-empirical formulas for the specific structure. It requires some restrictions such as symmetric structure and limited return area. Also no other wires are allowed above or below the signal lines. It is again applicable only to specific pre-assigned structures, and mainly intended for pre-layout extraction and analysis.

Our methodology, in contrast, can be applicable to efficient post-layout wide-band interconnect modeling. It is intended for global interconnect post-layout extraction, where inductive effects are pronounced, but can also be modified and extended for full-chip extraction. This is the first self and mutual inductance extraction and wide-band modeling method presented in the literature, outside the transmission line context. Since it is based on the physical phenomenon of current distribution in multiple returns, which changes with frequency, our model predicts well the self and mutual inductances and resistances within a wide frequency range. Our methodology also provides a lumped circuit model suitable for timing analysis, which can be conducted with any time or frequency-domain circuit simulator. This novel approach can be applied to general high-speed structures with multiple returns, asymmetric coupled wires, and multiconductor structures. Moreover, it does not require any fitting algorithm and optimization process.

This paper consists of five sections and the organization is as follows. The importance of mutual inductance and resistance is described in Section II. Section III presents the methodology to extract mutual impedance, and shows several examples and robustness of the model. The experimental method and results for single and coupled wires are presented in Section IV, followed by concluding remarks in Section V.

II. Importance of Mutual Impedance

In general, magnetic field induced by current flow has longer-range interaction compared to electric field. Therefore, many wires in a multiconductor system can influence one another, not merely the nearest neighbors, which is generally assumed in capacitance calculations. This coupling is represented by mutual inductance and resistance of which importance has been demonstrated in [20]–[22]. In this section we will discuss the impact of mutual impedance on timing analysis.

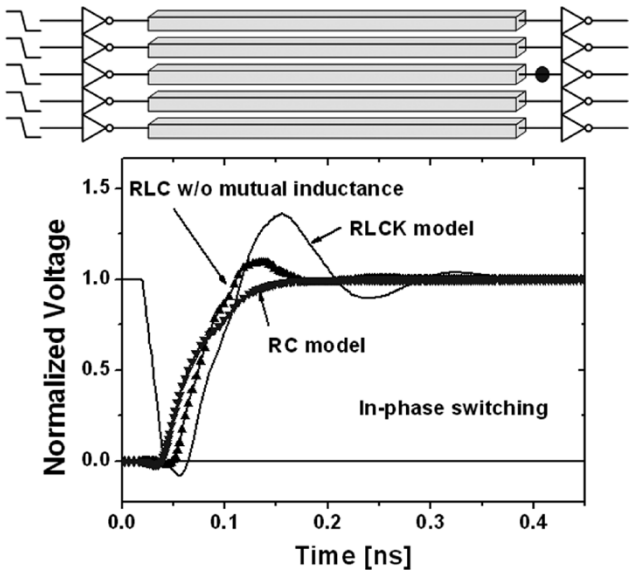

Fig. 1. Signal waveforms for in-phasing switching at the end of center wire of five 3-mm wires for *RLCK* model, *RLC* model without mutual inductances, and *RC* model. Width and spacing of wires are 1 and 0.4 μm, respectively. Signal voltage is normalized to power supply voltage $V_{\rm dd}$.

A. Mutual Inductance

In a linear multiconductor system, mutual inductance between two conducting loops is given by magnetic flux generated by the first current loop that is coupled into the second loop, and then divided by current flowing in the first loop. Its magnitude critically depends on the direction of current flow. In order to illustrate the impact of mutual inductance, signal waveforms in five coupled bus lines are studied using different interconnect models. Fig. 1 shows signal waveforms observed at the end of the middle wire of five 3-mm wires for in-phase switching condition. In-phase switching means that all the wires switch from ground to $V_{\rm dd}$ simultaneously. The width and spacing between wires are 1 and 0.4 μm, respectively. The metal is assumed to be copper. In the graph, the three curves represent results from the *RLCK* model (K denotes the inductive coupling terms), the *RLC* model ignoring mutual inductances (self inductances and mutual capacitances are included), and the *RC* model, respectively. In the case of in-phase switching, mutual capacitances do not induce capacitive coupling since all wires have the same electric potential. From the curves, inductive behavior increases as current flow is in the same direction in all conductors for in-phasing switching, thus worsening inductive ringing effect and increasing line delay. If mutual inductance is excluded in the simulation, the overshoot is as small as 9% of $V_{\rm dd}$. However, the overshoot increases up to 36% when mutual inductances are included. Delay obtained using the *RLCK* model is 28% and 63% larger than the *RLC* and the *RC* models, respectively, showing that inductive coupling will increase in multiple bus lines structures.

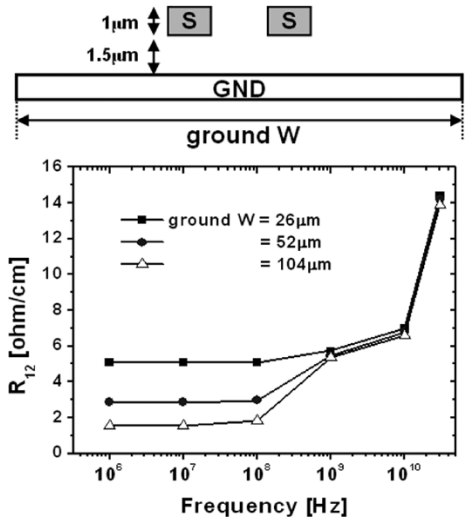

Fig. 2. Mutual resistance versus frequency characteristics for a structure shown above with various ground plane widths. The widths and spacing of signal wires are 4 and 1.5 μm, respectively.

B. Mutual Resistance

In general, a resistance matrix for two coupled wires can be expressed as a symmetric matrix due to its passivity

$$[\boldsymbol{R}] = \begin{bmatrix} \boldsymbol{R}_{11} & \boldsymbol{R}_{12} \\ \boldsymbol{R}_{12} & \boldsymbol{R}_{22} \end{bmatrix}. \tag{1}$$

The real part of the mutual impedance R_{12} is related to the return path, and is usually is ignored in the literature, especially in crosstalk modeling [23]–[25]. If we consider an ideal return path (perfect conductor or very large return area), R_{12} is very small and the resistance matrix becomes diagonal at low frequencies. However, in real chips, the return path is not perfect ground and has some resistance. An ideal return path is a good assumption for the low-frequency regime because the return current spreads throughout the entire return path or the ground plane to minimize the resistance. However, when the operating frequency increases, the return current will flow near the signal wire to reduce the impedance of the loop and induced eddy currents will be generated due to electromagnetic coupling [26], thus increasing R_{12} significantly. For example, a resistance matrix at 10 GHz for two 1-cm long coupled wires above ground plane, with 4 μm-width and 1.5 μm-spacing is given by

$$[R_{\text{two}}] = \begin{bmatrix} 67.5 & 6.9 \\ 6.9 & 67.5 \end{bmatrix} \frac{\Omega}{\text{cm}}.$$

R_{12} is approximately 10% of R_{11}, and ignoring R_{12} would result in a large error in timing analysis. Fig. 2 shows how R_{12} changes with frequency for various dimensions of the ground plane. Below 100 MHz, because the return current flows through the entire ground plane, R_{12} depends on the dimension of the ground plane. However, when the operating frequency goes above 1 GHz, the difference among the three dimensions diminishes since the current return path becomes narrower. The increased R_{12} can degrade signal integrity as in [20], [21]. Hence, the resistance of a multiconductor system should be treated in a full matrix form, and mutual resistance should be considered properly in timing analysis.

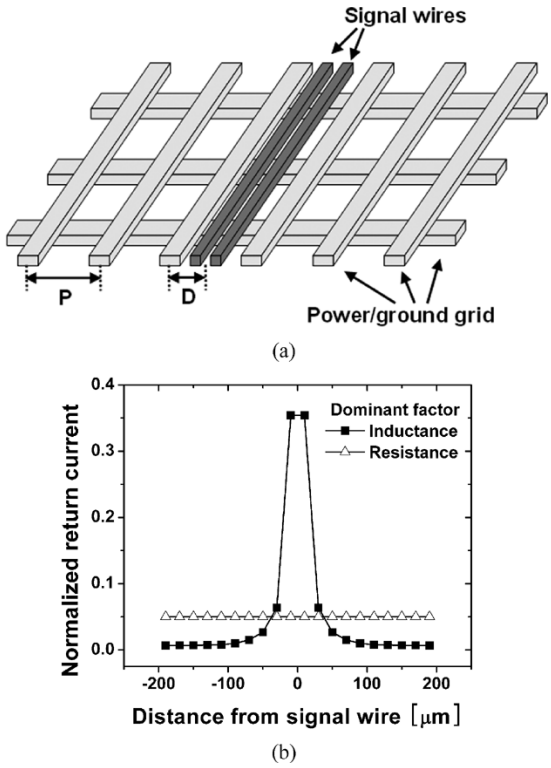

Fig. 3. (a) High-speed on-chip interconnects with power/ground grid. P and D denote the pitch of power grid and the distance between center of coupled wires and nearest power grid, respectively. (b) Return current distribution (normalized to total current) on grid for inductance and resistance dominant regimes. Dimensions used: $P = 20$ μm, $D = 10$ μm, signal wire width $= 1$ μm, power/ground wire width $= 4$ μm.

III. Inductance Modeling Methodology for Coupled Wires

Inductance of coupled wires in a multiconductor system is represented by a 2×2 matrix in the loop approach in comparison with the PEEC approach where all ground returns should be included. Self inductances, diagonal terms of the matrix, are determined by closed loop formation of current flowing, and mutual inductance depends on position and relative distance between the two loops. Although the effect of inductive coupling has increased due to tighter design rules and faster transition times, only few methods for analysis and modeling of mutual inductance have been reported. In this section, we present an inductance matrix extraction and modeling methodology including mutual inductance. Return current distribution and overall methodology are described in Sections III-A and III-B. Details of our method are shown with several examples in Sections III-C–III-E.

A. Return Current Distribution

A typical high-speed on-chip interconnect pattern with power/ground grid is shown in Fig. 3(a). To extract loop inductance, the return path (return current distribution) should be determined, which is possible at specific frequency regimes. One of the ambiguities in loop inductance extraction comes from the difficulty in determining how far the return current spreads. Elfadel [19] considered just the neighboring ground at high frequencies when calculating inductance, but in reality

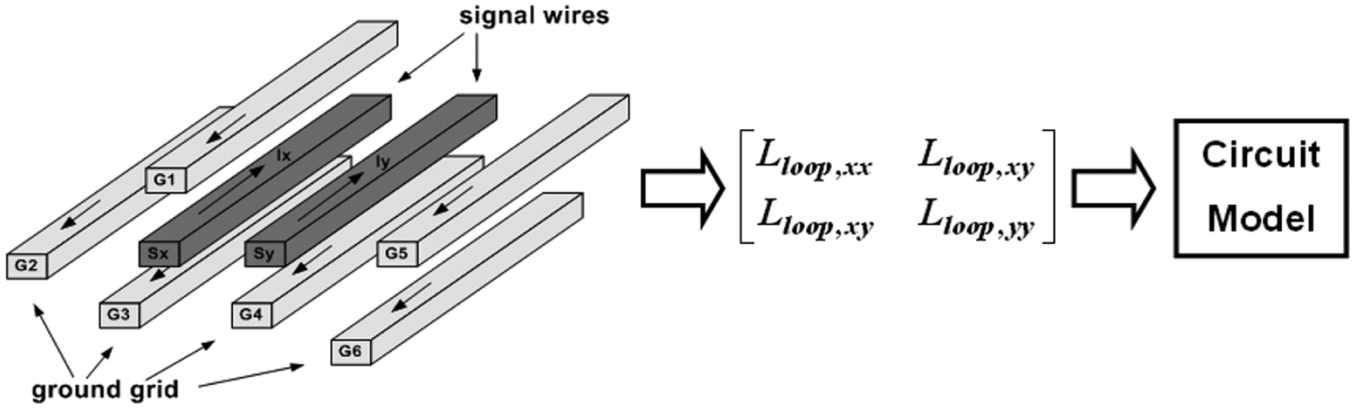

Fig. 4. Inductance modeling approach for coupled wires within a ground grid. The loop inductance is represented by a 2×2 matrix ($[L_{\rm loop}]$). Frequency-dependent circuit model consists of lumped elements only.

there is current spreading even in this regime. We investigated the current distribution in the grid structure for two extreme cases, where resistance or inductance is dominant, and the interconnects can be considered as *RC*-like or *LC*-like wires, respectively [12], [13]. For an *RC*-like wire, the normalized return current on the kth return path can be expressed as [12]

$$|I_k| = \frac{R_{\rm all\_return}}{R_k} \tag{2}$$

where $R_{\rm all\_return}$ is the parallel resistance of all return paths and R_k is the resistance of the kth return. For an *LC*-like wire, the grid currents can be calculated as [27]

$$[P]^T [L] [P] [I] = [V] \tag{3}$$

where $[P]$ is a mesh matrix and $[I]$ is the matrix of branch currents flowing through the return paths. The partial inductance matrix ($[L]$) in (3) can be calculated from Grover's inductance formulae [28] for rectangular wire to yield

$$\begin{aligned} L_{\rm km} &= 0.0002\, l \left[\ln\left(\frac{2l}{W+T}\right) + \frac{1}{2} - \ln\lambda \right], \qquad \text{for } k = m \\ &= 0.0002\, l \left[\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}}\right) - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l} \right], \quad \text{for } k \neq m. \end{aligned} \tag{4}$$

In this formula, l, W, and T are the length, width, and thickness of the wire, respectively. ln λ is a function of the ratio W/T and negligible for the case of $l > (W + T)$. d represents the geometric mean distance between two wires.

Calculated current distribution shows that in the inductance-dominant regime, the return currents concentrate in the few lines next to the signal wire to reduce the total impedance. In this example [Fig. 3(b)], 70% of total return current resides in the nearest grids and 89% flows through six grids next to the signal wire. Therefore, considering up to the third grid on either side of the signal wire will yield reasonable results. This current distribution will be used in loop inductance calculations in the next subsection. Throughout this paper, orthogonal wires in adjacent layers are ignored in inductance calculation. As pointed in [9], [19], the orthogonal magnetic field does not change the inductive properties of the signal wire.

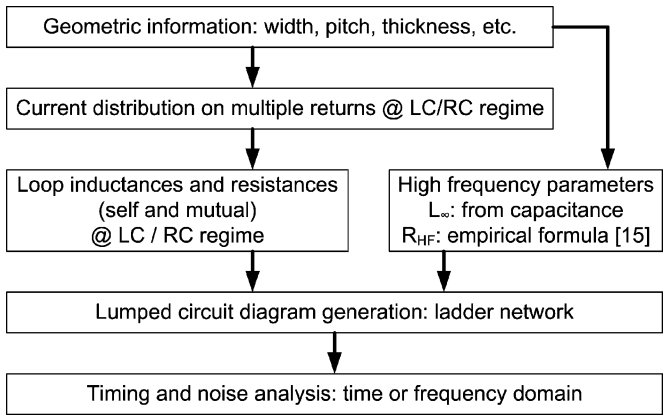

Fig. 5. Inductance extraction and modeling methodology flow.

B. Overall Extraction and Modeling Methodology

The overall extraction and modeling approach is depicted in Fig. 4. For coupled wires within a multiconductor system, the loop inductance matrix can be calculated at some specific frequency points. Since we have obtained the return current distribution in *LC* and *RC* regimes, the entire return loop and the loop inductances including self and mutual terms can be calculated in those regimes. These matrices are then incorporated into a frequency-dependent *RLC* lumped circuit model. It consists of only passive elements and can be readily incorporated into any circuit simulator.

Detailed steps of the modeling processes are shown in Fig. 5. Given geometric information such as width, spacing, and thickness of the signal and ground grids, current distribution in multiple returns in the *LC* and *RC* regimes can be obtained from (2) and (3). From return currents, the loop inductance and resistance matrices can be derived by using the equivalence of magnetic energy and power to yield

$$\frac{1}{2}\sum_{i,j} \boldsymbol{L}_{ij}\boldsymbol{I}_i\boldsymbol{I}_j = \frac{1}{2}\begin{bmatrix}\boldsymbol{I}_x \\ \boldsymbol{I}_y\end{bmatrix}^T [\boldsymbol{L}_{\rm loop}] \begin{bmatrix}\boldsymbol{I}_x \\ \boldsymbol{I}_y\end{bmatrix} \tag{5}$$

$$\sum_k \boldsymbol{R}_k\boldsymbol{I}_k^2 = \begin{bmatrix}\boldsymbol{I}_x \\ \boldsymbol{I}_y\end{bmatrix}^T [\boldsymbol{R}_{\rm loop}] \begin{bmatrix}\boldsymbol{I}_x \\ \boldsymbol{I}_y\end{bmatrix}. \tag{6}$$

Here, the left-hand side refers to the wire configuration in Fig. 4, while $[L_{\rm loop}]$ and $[R_{\rm loop}]$ are loop inductance and resistance

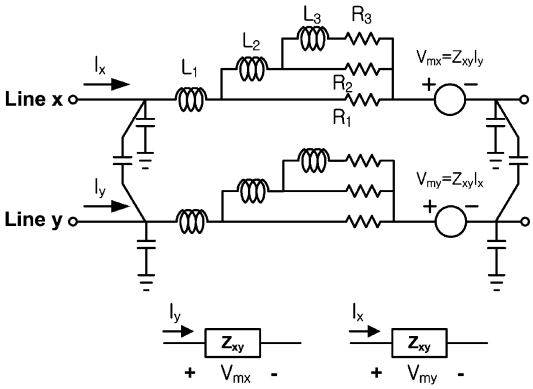

Fig. 6. One segment of Cauer-type lumped circuit model consisting of frequency-independent elements. Voltage source $V_{\rm mx}$ and $V_{\rm my}$, represent the effects of mutual impedance, $Z_{\rm xy}$. $Z_{\rm xy}$ is also represented using the same *RL* ladder model as the self terms. Hence, a total of 12 inductors and 12 resistors per segment are used in this model.

matrices for that wiring, respectively. Subscripts x and y denote the two signal wires. If a current source is applied to only one signal wire, loop self inductances ($L_{\rm loop,xx}$ and $L_{\rm loop,yy}$) can be obtained. To derive the mutual inductance ($L_{\rm loop,xy}$), current sources should be applied to both signal wires at the same time. From (5) and (6), we obtain four effective matrices, $[L_{\rm loop,LC}]$, $[L_{\rm loop,RC}]$, $[R_{\rm loop,LC}]$, and $[R_{\rm loop,RC}]$, in the *LC* and *RC* regimes. At frequencies higher than 20 GHz, the inductance matrix at infinite frequency ($[L_\infty]$) is used, which can be calculated from the capacitance matrix [14], and a modified skin-effect formula [15] is applied to extract resistance. Capacitance extraction can be performed using first-principle formulas [13] or a field solver. These matrices represent the effective inductance and resistance in each frequency regime and are used to construct the lumped circuit model.

Fig. 6 shows the Cauer-type *RL* ladder circuit representation [29] of the coupled wires within multiple returns, using our model to capture frequency-dependent behavior of interconnect parameters. Mutual inductance, usually modeled in SPICE with a coupling coefficient K, is included in the voltage sources, $V_{\rm mx}$ and $V_{\rm my}$. Since the two signal wires can be considered as a two-port network, the voltage sources are defined as

$$\begin{bmatrix} \boldsymbol{V}_x \\ \boldsymbol{V}_y \end{bmatrix} = \begin{bmatrix} \boldsymbol{Z}_{\rm xx} & \boldsymbol{Z}_{\rm xy} \\ \boldsymbol{Z}_{\rm xy} & \boldsymbol{Z}_{\rm yy} \end{bmatrix} \begin{bmatrix} \boldsymbol{I}_x \\ \boldsymbol{I}_y \end{bmatrix} = \begin{bmatrix} \boldsymbol{Z}_{\rm xx}\boldsymbol{I}_x + \boldsymbol{V}_{\rm mx} \\ \boldsymbol{Z}_{\rm yy}\boldsymbol{I}_y + \boldsymbol{V}_{\rm my} \end{bmatrix}. \quad (7)$$

Mutual impedance $Z_{\rm xy}$ has similar frequency characteristics as self impedances, and thus can also be represented by the same *RL* ladder circuit as the self terms. Hence, only 12 inductors and 12 resistors per segment are used to describe interconnect behavior over a wide frequency range for the multiconductor system. The number of segments depends on the wire length and signal wavelength.

In general, the values of the six lumped elements for each wire, as shown in Fig. 6, can be obtained from physical parameters extracted for a given interconnect structure to yield the following:

$$\begin{aligned} &\boldsymbol{L}_1 = \boldsymbol{L}_\infty, \quad \boldsymbol{R}_1 = \boldsymbol{R}_{HF} \\ &\boldsymbol{L}_2 = (\boldsymbol{L}_{\rm loop,LC} - \boldsymbol{L}_1)\left(\frac{\boldsymbol{R}_1 + \boldsymbol{R}_2}{\boldsymbol{R}_1}\right)^2, \boldsymbol{R}_2 = \left(\frac{1}{\boldsymbol{R}_{\rm loop,LC}} - \frac{1}{\boldsymbol{R}_1}\right)^{-1} \\ &\boldsymbol{L}_3 = \left[(\boldsymbol{L}_{\rm loop,RC} - \boldsymbol{L}_1)\left(\frac{\boldsymbol{R}_1 + \left(\frac{1}{\boldsymbol{R}_2} + \frac{1}{\boldsymbol{R}_3}\right)^{-1}}{\boldsymbol{R}_1}\right)^2 - \boldsymbol{L}_2\right]\left(\frac{\boldsymbol{R}_2 + \boldsymbol{R}_3}{\boldsymbol{R}_2}\right)^2 \\ &\boldsymbol{R}_3 = \left(\frac{1}{\boldsymbol{R}_{\rm loop,RC}} - \frac{1}{\boldsymbol{R}_1} - \frac{1}{\boldsymbol{R}_2}\right)^{-1}. \end{aligned} \quad (8)$$

Parameters in the *LC* and *RC* regimes, $R_{\rm loop,LC}$, $L_{\rm loop,LC}$, $R_{\rm loop,RC}$, and $L_{\rm loop,RC}$ are extracted analytically from the configuration of the signal line and multiple returns as discussed previously. For mutual impedance, the same equations are applied to obtain the lumped model elements.

This methodology allows one to extract and model self and mutual inductance and resistance from a physical layout without any fitting algorithm. The lumped ladder network is suitable for crosstalk and delay analysis, and facilitates extraction of circuit model parameters. The next subsection describes the detailed implementation and evaluation of our model for various structures.

C. Coupled Wires Within Power/Ground Grid

To illustrate the full implementation of our model, we first use the example of two signal wires within six ground returns as shown in Fig. 3(a). The dimensions of this structure are as follows: width and spacing of signal wires are 1 μm, width and pitch (P) of the ground grid are 4 and 20 μm, respectively, distance (D) between the nearest ground grid and the center of the two signal wires is 5 μm. Using (4), the partial inductance matrix is computed to yield (9), shown at the bottom of the page. The first two rows and columns are for the two signal wires and the others for the ground returns. From the inductance matrix and using (2) and (3), the current distribution in each grid can be calculated for the *LC* and *RC* regimes as discussed previously. Since the signal wires are asymmetric relative to the

$$[\boldsymbol{L}_{partial}] = \begin{bmatrix} 1.478 & 1.182 & 0.572 & 0.689 & 1.044 & 0.769 & 0.611 & 0.526 \\ 1.182 & 1.478 & 0.564 & 0.674 & 0.963 & 0.795 & 0.622 & 0.533 \\ 0.572 & 0.564 & 1.293 & 0.725 & 0.590 & 0.513 & 0.459 & 0.418 \\ 0.689 & 0.674 & 0.725 & 1.293 & 0.725 & 0.590 & 0.513 & 0.459 \\ 1.044 & 0.963 & 0.590 & 0.725 & 1.293 & 0.725 & 0.590 & 0.513 \\ 0.769 & 0.795 & 0.513 & 0.590 & 0.725 & 1.293 & 0.725 & 0.590 \\ 0.611 & 0.622 & 0.459 & 0.513 & 0.590 & 0.725 & 1.293 & 0.725 \\ 0.526 & 0.533 & 0.418 & 0.459 & 0.513 & 0.590 & 0.725 & 1.293 \end{bmatrix} \frac{\rm nH}{\rm mm}. \quad (9)$$

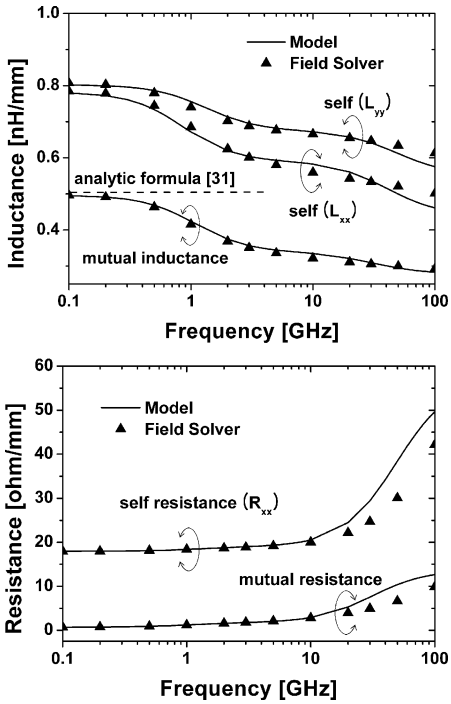

Fig. 7. Inductances and resistances of our model compared with field-solver results. R_{yy} (not shown) is nearly equal to R_{xx} due to the equal wire widths and negligible difference in contributions from proximity effect. Dimensions used: $P = 20\ \mu$m, $D = 5\ \mu$m, width and spacing of signal wires $= 1\ \mu$m, power/ground wire width $= 4\ \mu$m.

ground grid, the current distribution and inductances will also be asymmetric. Loop inductance and resistance matrices in the *LC* and *RC* regimes are computed using (5) and (6) as follows.

$$[\boldsymbol{L}_{\text{loop,LC}}] = \begin{bmatrix} 0.596 & 0.341 \\ 0.341 & 0.681 \end{bmatrix} \left[\frac{\text{nH}}{\text{mm}}\right]$$
$$[\boldsymbol{R}_{\text{loop,LC}}] = \begin{bmatrix} 18.94 & 1.701 \\ 1.701 & 18.94 \end{bmatrix} \left[\frac{\Omega}{\text{mm}}\right]. \quad (10)$$
$$[\boldsymbol{L}_{\text{loop,RC}}] = \begin{bmatrix} 0.787 & 0.497 \\ 0.497 & 0.807 \end{bmatrix} \left[\frac{\text{nH}}{\text{mm}}\right]$$
$$[\boldsymbol{R}_{\text{loop,RC}}] = \begin{bmatrix} 17.96 & 0.718 \\ 0.718 & 17.96 \end{bmatrix} \left[\frac{\Omega}{\text{mm}}\right]. \quad (11)$$

Using the empirical formula given in Kleveland [15], high-frequency matrices are also computed.

$$[\boldsymbol{L}_{\infty}] = \begin{bmatrix} 0.440 & 0.278 \\ 0.278 & 0.551 \end{bmatrix} \frac{\text{nH}}{\text{mm}}, [\boldsymbol{R}_{HF}] = \begin{bmatrix} 56.81 & 13.57 \\ 13.57 & 56.81 \end{bmatrix} \frac{\Omega}{\text{mm}}. \quad (12)$$

The six matrices given by (10) – (12) provide the resistance and inductance for the three frequency regimes. These values are used to construct the lumped circuit model with elements calculated using the six formulas in (8).

In Fig. 7, our model is compared with a quasi-static field solver [30]. Since the loop area of line y is larger than line x due to the asymmetry, L_{yy} is greater than L_{xx}. In Fig. 7(a), the mutual inductance obtained analytically [31], shown for comparison, cannot capture the frequency-dependent behavior. Self and mutual inductances show rapid decrease in the range $0.2 \sim 5$ GHz. Decrease in inductance reflects change in return current

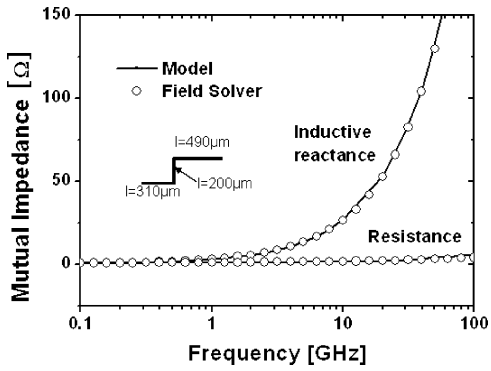

Fig. 8. Mutual impedances for concatenated wire with three different segments.

distribution in the power/ground grid, which effectively reduces the total loop impedance experienced by the signal. Resistances slightly increase in the range where proximity effect is important, and then rapidly increase due to skin effect. As can be seen in Fig. 7, the results of our model match well with those from the field solver. The discrepancy of mutual impedance between our proposed model and the field solver is close to 3.5% at 20 GHz.

In a typical interconnect structure a long wire can meander through several layers of the chip. Some researchers have reported that each bend in the wire has a small effect on the total parasitics [17], [32] due to small size of the bend compared to the total wire length and signal wavelength. Another concern for such a long wire is the scalability of the model. In Fig. 8, we compare our model with the field solver for a wire with three different segments. Each segment is modeled using our methodology, and then the models of each segment are concatenated to construct the final model for the entire wire. Comparison with a field solver demonstrates good scalability of our model for the concatenated wire.

D. Two Signal Wires With MultiLayer Returns

In high-speed on-chip interconnects, power/ground grids are present in several metal layers to supply power with minimal energy loss, and these can also serve as return paths. The effect of the local power grid in metal 1 and metal 2 was studied in [15], and significant reduction of the inductance was shown from measurement on test structures. For a single wire with parallel ground returns in an adjacent layer, a complex hybrid ladder model was used [12], based on the assumption that parallel returns affect loop impedance at high frequencies only. Generally for a complex structure, a field solver is used to extract interconnect parameters at specific frequencies [19], which requires extensive computational effort. In our model, multilayer returns can be modeled without loss of consistency and computational efficiency. Fig. 9(a) shows typical global interconnects implemented in the top-most layer on a chip. To consider general wiring, we investigate asymmetric signal wires having multilayer returns where the widths of the signal wires are 1 μm and 2 μm. Wires in the $(N-1)$-layer are orthogonal to those in the N and $(N-2)$-layers, and are ignored in inductance calculations. As seen in Fig. 9(b), our model shows good agreement with the field solver.

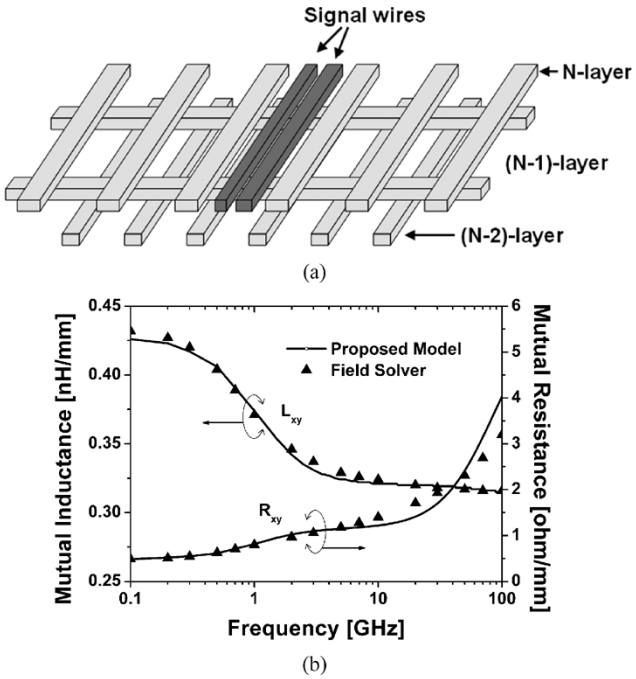

Fig. 9. (a) Global interconnects in top-most layer. Wires in the $(N-1)$-layer are orthogonal to those in the N and $(N-2)$-layers. (b) Mutual inductance and resistance curves. Widths of signal wires are 1 and 2 μm, and spacing is 1 μm.

E. Multiple Signal Wires Distributed Within Multiple Power Bays

In previous subsections, we have focused on coupled wires in simple structures to explain the concept of proposed modeling methodology. A high-speed on-chip interconnect system is very complex. Some of the features include power/ground network, multiple coupled bus lines, and meandering structures using more than two metal layers. For the proposed model to be adequate for highly packed on-chip interconnects, multiple signal wires distributed within multiple power bays are considered as depicted in Fig. 10(a). For this example of 20 signal wires and four power bays, the proposed methodology is then applied to estimate the frequency characteristics of parasitics. It should be noted that when one considers the mutual inductance between two conductors in multiconductor systems since eddy current and capacitive coupling to random signal wires are negligible up to a few gigahertz [33], all other conductors do not affect the estimation of mutual inductance in those regions. The results of proposed model and field solver are shown in Fig. 10(b) and (c). The graph shows the impedance of signal wire #12 at 20 GHz, and the overall error is about 5.1%. As expected, as the distance from signal line #12 becomes larger, the mutual impedance decreases. It is clearly seen that for the wires on other side of the wide power/ground grid the mutual parasitics are dramatically reduced and can be ignored. In this example, the amount of mutual impedance from signal line $\#6 \sim \#10$ and $\#16 \sim \#20$ is less than 6% of total impedance of signal line #12. These results provide us with a guideline that can be used to limit the area in which the mutual parasitics effect has to be considered.

A complex on-chip interconnect system can be partitioned and then reduced to some typical simpler cases which have been considered in this work. Some partitioning methodologies can

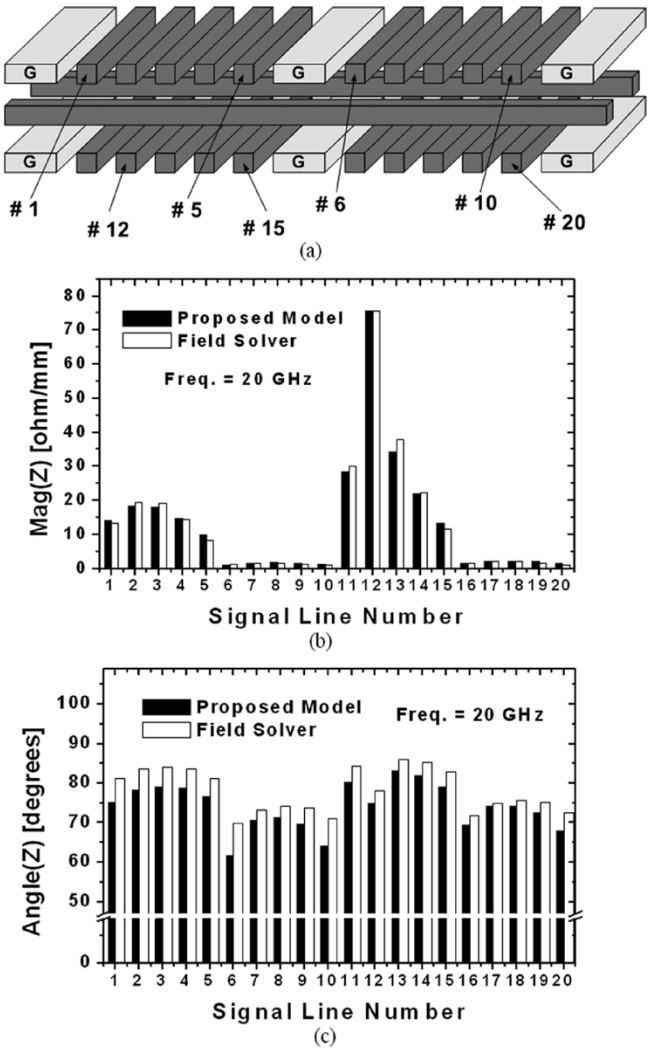

Fig. 10. (a) Twenty signal wires within a power/ground network. The numbers indicate the signal line number used in (b) and (c). Dimensions used: width and spacing of signal lines $=$ 1 μm, width of power/ground line $=$ 4 μm. (b) Magnitude of the impedance of signal line #12 for proposed model and field solver at 20 GHz. For example, #1 on x axis denotes the mutual impedance between signal line #12 and #1 while #12 on x axis gives the self term of signal line #12. (c) Phase of the impedance at 20 GHz.

be found in [16], [19], [34]. For example, in [16], each wire is fractured into a set of segments whenever the interaction environment as defined by the power/ground lines changes. Parasitic extractions were performed at each segment and then the results were concatenated to represent the whole wire. Examples in this work can constitute the typical cases, and we believe that the proposed modeling methodology can be effectively applied for inductance extraction of on-chip interconnects.

Computational times of the proposed model are compared with a field solver [30] and FastHenry [35] for the three examples, as shown in Table I. Although FastHenry and the field solver compute inductance values at only 16 frequency points compared to 200 points for our model, their simulation times are two or more orders of magnitude longer.

IV. Measurement Results

In the previous section, our modeling methodology was compared to field solver simulation for various structures. To con-

TABLE I
COMPUTATIONAL TIME COMPARISON FOR THREE METHODS

	FastHenry	Field Solver	Proposed Model
Example 1	366 s	272 s	Less than 5 s
Example 2	1775 s	1768 s	Less than 5 s
Example 3	$2.16\text{x}10^4$ s	$1.73\text{x}10^4$ s	Less than 10 s

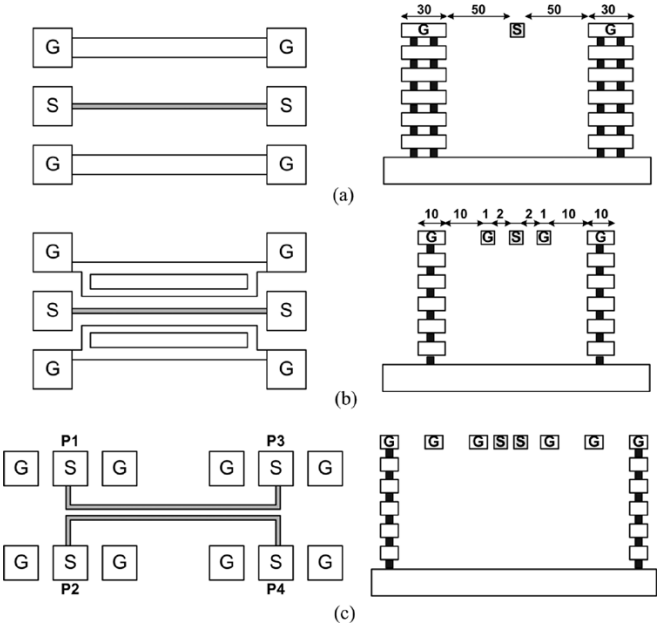

Fig. 11. Simplified measurement structures, fabricated in 0.13- and 0.18-μm CMOS technologies, having signal wires in the metal 6 layer; (a) and (b) for single signal lines, and (c) for coupled lines. Numbers in the structure represent dimensions in micrometers. The widths of all signal lines are 1 μm, and the width and pitch of ground grid in (c) are 2 and 20 μm, respectively.

firm its accuracy further, we fabricated typical test structures on a silicon substrate and measured their S-parameters, so that a one-to-one comparison can be made with simulation and/or modeling results. These structures have been fabricated with 0.13- and 0.18-μm CMOS technologies consisting of six metal layers. Fig. 11 shows some of the test structures that have signal wires and parallel ground returns, which are connected to the substrate. Each pattern in Fig. 11(a) and (b) consists of a single signal wire with two or more return paths in the same layer. Each signal wire is 1 μm wide and in the metal-6 layer. For multiple-loop returns such as the structure in Fig. 11(b), return currents vary with frequency due to proximity effect, resulting in significant inductance variations from low to high frequencies. On the other hand, for the single-loop return as shown in Fig. 11(a), no proximity effect exists, and the inductance variation is expected to be small. Fig. 11(c) shows a test structure with coupled wires, which can be considered as a four-port terminal coupler. It has three ground returns on either side of the signal wires and the spacing between the signal wires is 0.44 μm.

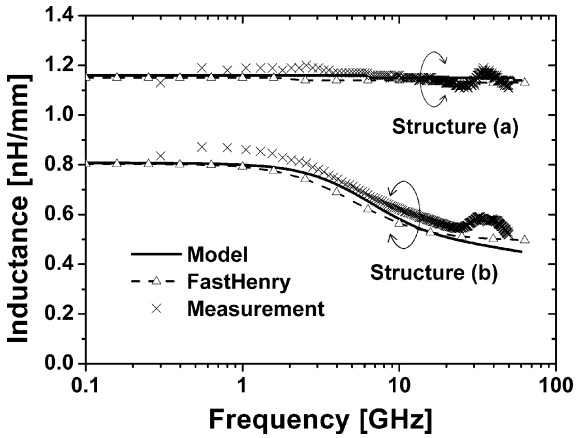

Fig. 12. Inductance curves for single line test structures shown in Fig. 11(a) and (b). The results from model, FastHenry, and measurement are shown for each test structure.

We measure the S-parameters for those structures up to 50 GHz with a vector network analyzer and ground-signal-ground high-frequency probes. After line-reflect-reflect-match (LRRM) calibration using commercial software, S-parameters were measured for each structure. Generally, LRRM calibration is preferred to short-open-load-thru method for frequencies above 20 GHz to obtain better stability and accuracy. Dummy patterns with no signal wires are used to de-embed the shunt parasitics of the probing pad via Y-parameter extraction. The interconnect parameters of a single signal line are deduced using the procedure described in [36]. For coupled wires [Fig. 11(c)], which have four ports, measurements are made with a two-port network analyzer. S-parameters are measured for each of the six two-port combinations, and the 4×4 S-parameter matrix is then constructed using the Gamma-R method [37]. The reflection coefficient for the unused port is calculated from results of measurements on a dedicated dummy pattern.

The measurement results for single-signal-wire structures are shown in Fig. 12, together with those from our model and FastHenry simulation. Using our model, the *RL* ladder circuit (Fig. 6) is constructed for each test structure to yield the frequency-dependent characteristics. As can be seen in Fig. 12, and as we expect, pattern (b) shows a large inductance decrease as frequency increases due to proximity effect of multiple return loops. At high frequencies, a large portion (79% in this case) of the return current will flow through the nearest ground lines, resulting in smaller inductance values due to smaller loop area. Pattern (a) shows little frequency-dependency since it has only one return loop and has no proximity effect. Our model matches well with both measurement and FastHenry simulation. The overall discrepancy is about 3.4% up to 20 GHz and the maximum is 8.6% between measurement and our proposed model. The small peaks at 35 GHz in both inductance curves are due to half-wavelength resonance.

Fig. 13 shows the results of measurements and our model for coupled wires. $|S_{21}|$, which is related to crosstalk, increases sharply up to 10 GHz and then stays fairly constant. Transmitted signal, $|S_{31}|$, decreases monotonically up to 50 GHz as a result of resistive loss which in turn increases with frequency due

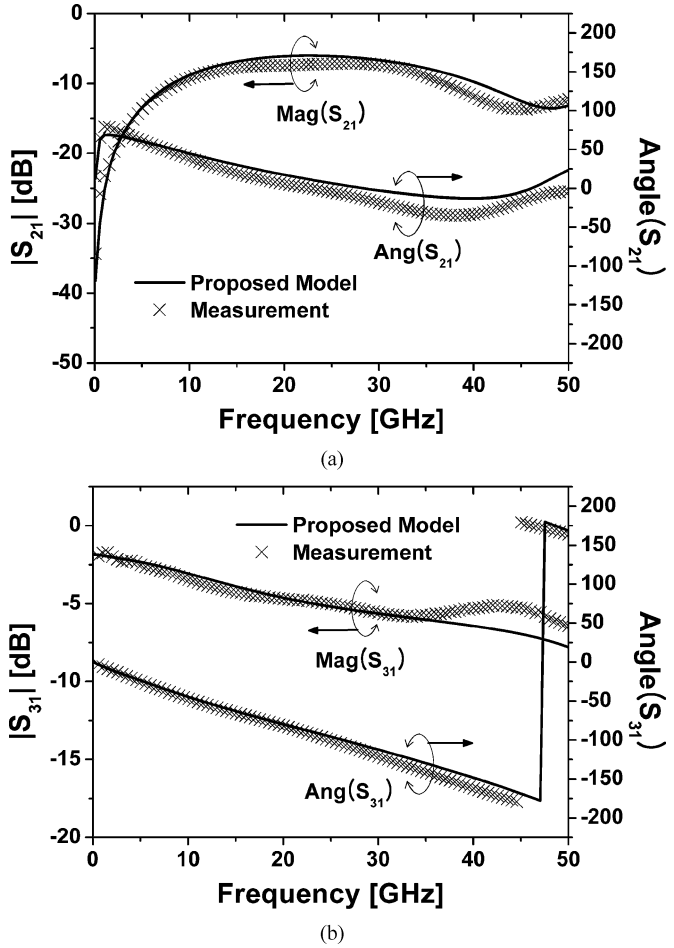

Fig. 13. S-parameters of coupled wires shown in Fig. 11(c) from measurement and proposed model. Port notations refer to Fig. 11(c). (a) Magnitude and angle of S_{21}. (b) Magnitude and angle of S_{31}.

to skin effect. Excellent correlation between measurements and our model confirms the validity of our extraction methodology.

V. Conclusion

In this paper, we proposed an efficient self and mutual inductance extraction and modeling method for high-speed on-chip interconnects. This wide-band model is based on physical layout considerations and current distribution on multiple returns, and predicts well the self and mutual inductance and resistance within a wide frequency range without any fitting algorithm or an optimization process. Some examples are presented to verify our model: asymmetric coupled structures having different positions with respect to ground grid, concatenated wires, and structures having multilayer returns. Measurement results for typical interconnects in silicon technology with single and coupled wires show excellent correlation with our model, confirming its accuracy and utility. This paper represents a comprehensive effort to model mutual impedance using a loop-based approach for high-speed on-chip interconnects. It can be used for pre-layout inductance extraction and modeling, and provides a methodology for fast full-chip post-layout extraction.

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References

[1] Y. I. Ismail, "On-chip inductance cons and pros," *IEEE Trans. Very Large Scale (VLSI) Integr. Syst.*, vol. 10, no. 6, pp. 685–694, Dec. 2002.

[2] R. Ho, K. W. Mai, and M. A. Horowitz, "The future of wires," *Proc. IEEE*, vol. 89, no. 5, pp. 490–504, May 2001.

[3] S. S. Wong, P. Yue, R. Chang, S.-Y. Kim, B. Kleveland, and F. O'Mahony, "On-chip interconnect inductance – Friend or foe," in *Proc. ISQED*, Mar. 2003, pp. 389–394.

[4] Y. Massoud, S. Mayors, J. Kawa, T. Bustami, D. MacMillen, and J. White, "Managing on-chip inductive effects," *IEEE Trans. Very Large Scale (VLSI) Integr. Syst.*, vol. 10, no. 6, pp. 789–798, Dec. 2002.

[5] S. V. Morton, "On-chip inductance issues in multiconductor systems," in *Proc. DAC*, Jun. 1999, pp. 921–926.

[6] A. E. Ruehli, "Inductance calculation in a complex integrated circuit environment," *IBM J. Res. Develop.*, vol. 16, pp. 470–481, 1972.

[7] K. Gala, D. Blaauw, J. Wang, V. Zolotov, and M. Zhao, "Inductance 101: Analysis and design issues," in *Proc. DAC*, Jun. 2001, pp. 329–334.

[8] M. W. Beattie and L. T. Pileggi, "On-chip induction modeling: Basics and advanced method," *EEE Trans. Very Large Scale (VLSI) Integr. Syst.*, vol. 10, no. 6, pp. 712–729, Dec. 2002.

[9] G. V. Kopcsay, B. Krauter, D. Widiger, A. Deutsch, B. J. Rubin, and H. H. Smith, "A comprehensive 2-D inductance modeling approach for VLSI interconnects: Frequency-dependent extraction and compact circuit model synthesis," *EEE Trans. Very Large Scale (VLSI) Integr. Syst.*, vol. 10, no. 6, Dec. 2002.

[10] Y. Cao, X. Huang, D. Sylvester, T.-J. King, and C. Hu, "Impact of on-chip interconnect frequency-dependent $R(\mathrm{f})L(\mathrm{f})$ on digital and RF design," *IEEE Trans. Very Large Scale (VLSI) Integr. Syst.*, vol. 13, no. 1, pp. 158–162, Jan. 2005.

[11] N. Arora, L. Song, and V. Chang, "Modeling and characterization of on-chip inductance for sub 100 nm Cu CMOS process," presented at the Proc. Compact Modeling Symp., Santa Clara, May 7, 2004.

[12] B. Krauter and S. Mehrtra, "Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis," in *Proc. DAC*, 1998, pp. 303–308.

[13] S.-P. Sim, S. Krishnan, D. M. Petranovic, N. D. Arora, K. Lee, and C. Y. Yang, "A unified *RLC* model for high-speed on-chip interconnects," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1501–1510, Jun. 2003.

[14] X. Huang, P. Restle, T. Bucelot, Y. Cao, T.-J. King, and C. Hu, "Loop-based interconnect modeling and optimization approach for multigigahertz clock network design," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 457–463, Mar. 2003.

[15] B. Kleveland, X. Qi, L. Madden, T. Furusawa, R. W. Dutton, M. A. Horowitz, and S. S. Wong, "High-frequency characterization of on-chip digital interconnects," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 716–725, Jun. 2002.

[16] K. L. Shepard and Z. Tian, "Return-limited inductances: A practical approach to on-chip inductance extraction," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 4, pp. 425–436, Apr. 2000.

[17] D. Goren, M. Zelikson, T. C. Galambos, R. Gordin, B. Livshitz, A. Amir, A. Sherman, and I. A. Wagner, "An interconnect-aware design methodology for analog and mixed signal design, based on high bandwidth (over 40 GHz) on-chip transmission line approach," in *Proc. DATE*, Mar. 2002, pp. 804–811.

[18] A. Deutsh, H. H. Smith, C. W. Surovic, G. V. Kopcsay, D. A. Webber, P. W. Coteus, G. A. Katopis, W. D. Becker, A. H. Dansky, G. A. Sai-Halasz, and P. J. Restle, "Freqeuncy-dependent crosstalk simulation for on-chip interconnects," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 292–308, Aug. 1999.

[19] I. M. Elfadel, A. Deutsch, H. H. Smith, B. J. Rubin, and G. V. Kopcsay, "A multiconductor transmission line methodology for global on-chip interconnect modeling and analysis," *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 71–78, Feb. 2004.

[20] S. V. Morton, "On-chip signaling," in *Proc. IEEE ISSCC*, Feb. 2002, pp. 554–557.

[21] S. Yu, D. M. Petranovic, S. Krishnan, K. Lee, and C. Y. Yang, "Resistance matrix in crosstalk modeling for multiconductor systems," in *Proc. ISQED*, Mar. 2004, pp. 122–125.

[22] M. H. Chowdhury, Y. I. Ismail, C. V. Kashyap, and B. L. Krauter, "Performance analysis of deep sub micron VLSI circuits in the presence of self and mutual inductance," in *Proc. IEEE ISCAS*, vol. 4, May 2002, pp. 26–29.
[23] T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 118–124, Jan. 1993.
[24] J. A. Davis and J. D. Meindle, "Compact distributed *RLC* interconnect models—Part II: Coupled line transient expression and peak crosstalk in multilevel network," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2078–2087, Nov. 2000.
[25] Y. Eo, S. Shin, W. R. Eisenstadt, and J. Shim, "Generalized traveling-wave-based waveform approximation technique for the efficient signal integrity verification of multicoupled transmission line system," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 12, pp. 1489–1497, Dec. 2002.
[26] J. E. Bracken, "Mutual Resistance in Spicelink," Ansoft Corporation, Pittsburgh, PA, 2000.
[27] B. Young, *Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages*. Englewood Cliffs, NJ: Prentice-Hall, 2001.
[28] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*. New York: Dover, 1946.
[29] A. Budak, *Passive and Active Network Analysis and Synthesis*. Boston, MA: Houghton Mifflin, 1974.
[30] *Maxwell Q2D/Q3D Parameter Extractor User's Guide*, Ansoft Corporation, Pittsburgh, PA, 2003.
[31] T. Lin, M. W. Beattie, and L. T. Pileggi, "On the efficacy of simplified 2-D on-chip inductance models," in *Proc. DAC*, Jun. 2002, pp. 757–762.
[32] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60 GHz applications," in *Proc. IEEE ISSCC*, Feb. 2004, pp. 440–448.
[33] S.-P. Sim, K. Lee, and C. Y. Yang, "High-frequency on-chip inductance model," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 740–742, Dec. 2002.
[34] Y.-C. Lu, M. Celik, T. Young, and L. T. Pilleggi, "Min/max on-chip inductance models and delay metrics," in *Proc. DAC*, Jun. 2001, pp. 341–346.
[35] M. Kamon, M. J. Tsuk, and J. K. White, "FASTHENRY: A multipile-accelerated 3-D inductance extraction program," *IEEE Trans. Microw.Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, Sep. 1994.
[36] W. R. Eisenstadt and Y. Eo, "S-Parameter-based IC interconnect transmission line characterization," *IEEE Trans Compon., Hybrids, Manufact. Technol.*, vol. 15, no. 4, pp. 483–490, Aug. 1992.
[37] J. C. Rautio, "Techniques for correcting scattering parameter data of an imperfectly terminated multiport when measured with a two-port network analyzer," *IEEE Trans. Microw. Theory Tech.*, no. 5, pp. 407–412, May 1983.

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