Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET

Jin-Woo Han, Jiye Lee, Donggun Park, and Yang-Kyu Choi

Abstract—The body thickness dependence of impact ionization for a multiple-gate fin field-effect transistor (FinFET) is presented. It is found that the nonlocal effect and series resistance are distinct features of reduced impact ionization in the multiple-gate FinFET, and these effects become more pronounced as the body thickness decreases. The impact ionization constant B_i is newly extracted by considering the series resistance and nonlocal carrier heating effect. A refined analytical substrate current model is developed from the previous model and revamped for multiple-gate devices. The new substrate current model is then compared with measurement data, and good agreement is observed.

Index Terms—Characteristic length, fin field-effect transistor (FinFET), impact ionization, multiple-gate MOSFET, nonlocal effect, substrate current, trigate.

I. INTRODUCTION

WITH SCALING OF CMOS into sub-45-nm technology nodes, suppression of short-channel effects (SCEs) becomes difficult in a planar single-gate (SG) MOSFET. As devices scale down to the sub-10-nm range, a multiple-gate (MG) MOSFET is considered to be the most promising structure due to its enhanced gate controllability on the channel. MG structures are featured by an ultrathin-body thickness, which is a critical parameter characterizing SCE.

With device scaling, hot-carrier effects (HCEs) have been a prominent issue for the past three decades. It is commonly accepted that the substrate current I_{Sub} arising from the impact ionization process near the drain edge can provide important guidance in estimating device reliability. While numerous studies have been conducted for HCE modeling with a focus on planar SG MOSFETs [1]–[3], a model for an MG MOSFET has not been developed. Thus, the modeling of HCE for an MG MOSFET is timely as well as essential.

There have been a few studies on HCE in a double-gate fin field-effect transistor (FinFET) [4]–[6]. These studies attempted to investigate the dependence on fin width, as this is an important parameter to govern SCE. While they all presented results demonstrating that a narrower fin is more immune to hot-carrier degradation than a wider fin, the mechanisms are still under debate. A major difficulty in analysis lies in measurement of I_{Sub}. As the FinFET is typically fabricated on a silicon-on-insulator substrate, I_{Sub} cannot be measured due to its floating-body. However, in our previous work, a special structure called by body-tied FinFET was developed on a bulk wafer, making measurement of I_{Sub} possible because the Si body of the device is tied to the substrate [6]. We argued that the significant source/drain (S/D) resistance plays a major role in the enhanced hot-carrier immunity of narrow-fin devices. In this letter, however, we suggest that a combination of a nonlocal effect and series resistance is important in the hot-carrier mechanism of the FinFET. Finally, a refined and improved analytical model considering these effects is developed and verified with measurement data.

II. RESULTS AND DISCUSSION

In this letter, all the simulations were performed using ATLAS from SILVACO. In this simulation, undoped channel, n^+ polysilicon, and abrupt junctions were used. The quantum mechanical effect was not included. MG ultrathin-body FinFETs can suffer from high parasitic resistance due to the narrow width of their S/D extension regions [7]. For a device biased at high drain voltage, the effective drain voltage drops across the thin extension region from the contact to junction. As shown in Fig. 1(a), simulation predicted that a narrower fin exhibits a larger peak electric field E_{peak} than a wider fin for distances between the junction to contact (d_{JC}) below 30 nm. As d_{JC} increases, however, E_{peak} of the narrower fin reduces more rapidly than that of the wider fin, and in turn, the E_{peak} values are crossed. This implies that the increment of parasitic voltage drop may reduce hot-carrier generation. Fig. 1(b) shows the electric field across the channel for various fin widths, with d_{JC} providing the same E_{peak}. According to the nonlocal energy balance model, the energy of electrons lags behind the electric field under a rapidly increasing electric field [3], [8], [9]. Assuming an exponential field in the high-field region, $E(x) \propto \exp(x/\lambda)$, the nonlocal effect must be serious for small λ, which is a characteristic length, $\lambda^2 = (\varepsilon_{\text{si}}/\varepsilon_{\text{ox}})t_{\text{ox}}(W_{\text{Fin}}/2)$, because it is clearly related to the shape of the field. In this letter, characteristic length from $\lambda = 7$ nm to $\lambda = 15.1$ nm is used for fin width from $W_{\text{Fin}} = 20$ nm to $W_{\text{Fin}} = 100$ nm, with 1.7-nm gate oxide. Because λ decreases as the body thickness is reduced, $E(x)$ can increase more rapidly. Because the gradient

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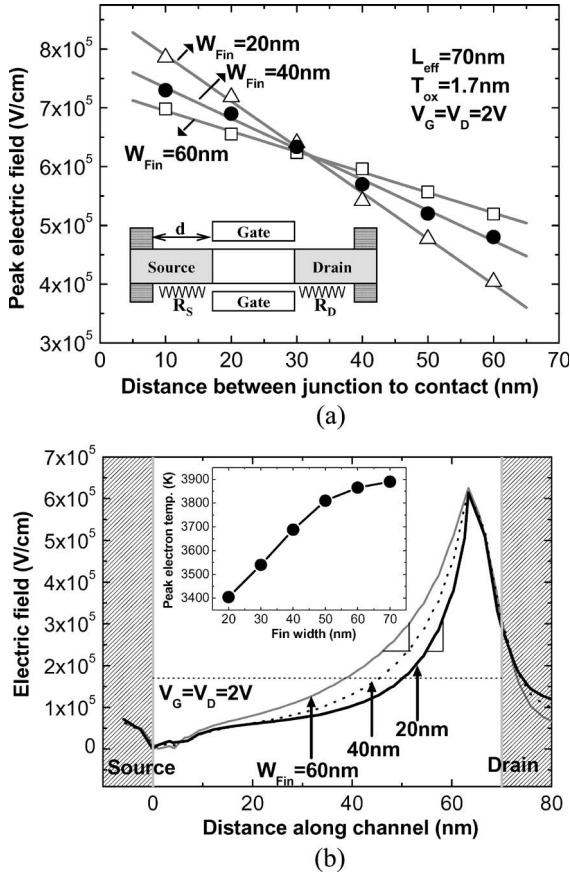
(a)

(b)

Fig. 1. Electric field and electron temperature prediction from a Silvaco simulation. To investigate the impact of parasitic series resistance on the peak electric field, the peak electric field was predicted for various distances between the junction to contact, as shown in the inset of (a). (a) E_{peak} of the narrower fin is larger at $d_{\mathrm{JC}} < 30$. However, this trend is reversed as d_{JC} increases. (b) Electric field distribution along the channel at a distance of 5 nm from the interface. Although E_{peak} is the same, the peak electron temperature reduces as the fin width decreases due to the influence of the nonlocal effect.

of the field is larger in the case of a narrower fin, the peak electron temperature reduces as the fin width decreases [shown in the inset of Fig. 1(b)]. As a result, the electron temperature of the narrower fin can be reduced despite the similar E_{peak}. Consequently, the parasitic resistance and nonlocal energy balance become the dominant factors governing the HCE in the narrower width FinFET.

In a MOSFET under a high electric field, the impact ionization rate $\alpha(x)$ based on the assumption that the electron is in thermal equilibrium with the lattice (local impact ionization) exponentially increases with the electric field, i.e.,

$$\alpha(x) = A_i \cdot \exp\left[-\frac{B_i}{E(x)}\right] \tag{1}$$

where A_i and B_i are impact ionization constants. An earlier study [3] introduced the concept of the effective electric field $E_{\mathrm{eff}}(x) = E(x)/(1 + \lambda_e/\lambda)$, where λ_e is the energy relaxation length, in order to explain the lagged electron temperature caused by the nonlocal effect. $\alpha(x)$ was then revised by replacing $E(x)$ and B_i in (1) to $E_{\mathrm{eff}}(x)$ and B_0, respectively, i.e., $\alpha(x) = A_i \exp[-B_0/\{E(x)/(1 + \lambda_e/\lambda)\}]$. Rearranging
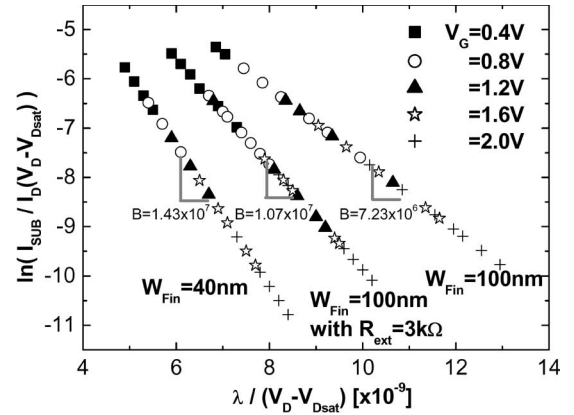

Fig. 2. Experimental determination of the impact ionization constant B_i in a body-tied FinFET for 100-nm gate length, 100-nm fin height, and 1.7-nm thermal oxide. The larger B_i of the narrower fin width implies less hot-carrier generation. To determine the impact of parasitic series resistance, extrinsic resistance $R_{\mathrm{ext}} = 3$ kΩ was serially connected to the S/D of $W_{\mathrm{Fin}} = 100$ nm (3 kΩ corresponds to a series resistance of $W_{\mathrm{Fin}} = 60$ nm extracted from measurement). B_i increases with the series resistance, thus implying that the HCE is suppressed with series resistance.
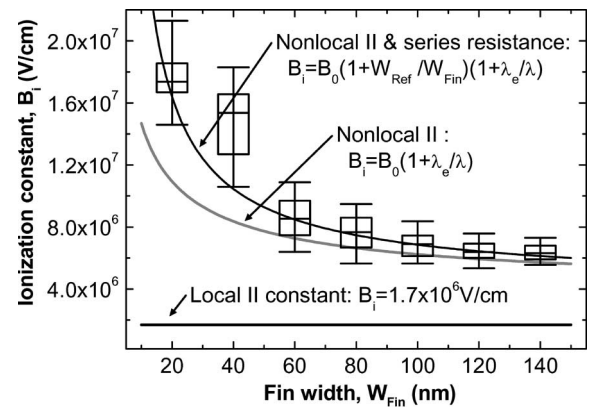

Fig. 3. Impact ionization parameter B_i as a function of fin width for (dot) measurement and (lines) models. For the model, $B_0 = 1.1 \times 10^6$ V/cm and $\lambda_e = 61$ nm were used [3]. B_i model considering the nonlocal effect deviated extensively from the measurement data at a fin width of less than 60 nm. However, the model considering both the nonlocal effect and series resistance corresponded well with the measurement data.

this equation, the reduced field can be treated as the increased ionization constant [from $B_i = B_0$ and $E_{\mathrm{eff}}(x) = E(x)/(1 + \lambda_e/\lambda)$ to $B_i = B_0(1 + \lambda_e/\lambda)$ and $E_{\mathrm{eff}}(x) = E(x)$]. According to the previous I_{Sub} model, $\ln(I_{\mathrm{Sub}}/I_D(V_D - V_{\mathrm{Dsat}}))$ versus $\lambda/(V_D - V_{\mathrm{Dsat}})$ yields one straight line for all biases, and a constant B_i can be extracted from the slope of the graph [2]. However, in the case of the FinFET, the plots yielded straight lines, but B_i is not a constant but a function of the fin width, as shown in Fig. 2. To explain the impact of parasitic voltage drop, extrinsic resistance $R_{\mathrm{ext}} = 3$ kΩ was intentionally connected to the S/D of $W_{\mathrm{Fin}} = 100$ nm. It was found that B_i of $W_{\mathrm{Fin}} = 100$ nm was increased as the parasitic resistance was increased. Therefore, the parasitic voltage drop results in increased B_i. In Fig. 3, B_i gradually increases and then rapidly increases below $W_{\mathrm{Fin}} = 60$ nm. B_i from the nonlocal impact ionization model deviates from the measured value. The origin of this deviation is the effects of the series resistance, and thus, a new B_i
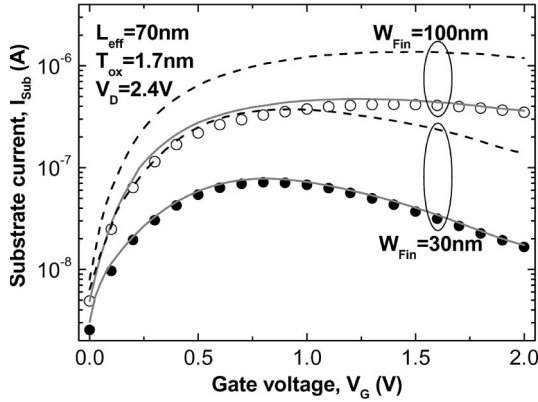
Fig. 4. Substrate current versus gate voltage for (dot) measurement, (dashed line) calculation from [3], and (solid line) calculation from (3). In the case of the model derived from the revised impact ionization rate, excellent agreement was achieved for various fin widths and bias conditions. $A_i = 2.45 \times 10^5$ /cm was used.

model combined with $R_{S/D}$ was developed. The dimensionless parameter ξ is introduced to B_i as

$$B_i = B_0 \cdot \xi \cdot \left(1 + \frac{\lambda_e}{\lambda}\right), \qquad \text{where} \quad \xi = \left(1 + \frac{W_{\text{Fin,ref}}}{W_{\text{Fin}}}\right) \tag{2}$$

where $W_{\text{Fin,ref}}$ is a reference fin width. However, it should be noted that $W_{\text{Fin,ref}}$ will vary according to the fabrication processes such as doping or the junction profile. For $W_{\text{Fin,ref}} = 10$ nm, good agreement between (2) and measurement data was achieved. Assuming a box-shaped uniformly doped abrupt junction of S/D, the series resistance is approximately proportional to the inverse of W_{Fin}. Therefore, the effect of a reduced electric field due to the potential drop by $R_{S/D}$ can reflect the increased B_i. It is worthwhile to note the fact that the series resistance effect degrades substrate current as well as drain current. Because a drain current is linearly reduced while substrate current is exponentially decreased due to the parasitic voltage drop caused by series resistance, at $V_G = V_D = 2$ V, although the drain current is reduced from $I_D = 138$ μA to $I_D = 89$ μA, impact ionization rate is lowered from $I_{\text{Sub}}/I_D = 4.3 \times 10^{-4}$ to $I_{\text{Sub}}/I_D = 3.7 \times 10^{-6}$ as the fin width is reduced from $W_{\text{Fin}} = 100$ nm to $W_{\text{Fin}} = 20$ nm. Furthermore, the suppression of the impact ionization rate can be intensified by nonlocal effect with the fin narrowing.

The new substrate current was obtained by integrating the revised $\alpha(x)$ over the channel by the following widely used circuit-level models [1]–[3]

$$I_{\text{Sub}} = \frac{A_i}{B_0} I_D \frac{\lambda}{\xi(\lambda + \lambda_e)} (V_D - V_{\text{Dsat}}) \exp\left(-\frac{B_0 \xi(\lambda + \lambda_e)}{V_D - V_{\text{Dsat}}}\right). \tag{3}$$

Fig. 4 shows the experimental substrate current. The previous model considering only the nonlocal effect (dashed line [3]) deviates from the measured results. However, excellent agreement between (3) and measurement data is achieved for various fin widths and bias conditions. Thus, a combination of the nonlocal carrier heating and series resistance is critical to govern the impact ionization characteristics in an MG FinFET. It should be noted that the proposed model is applicable for fin width larger than 20 nm. At the fin width thinner than 20 nm, additional factors such as carrier scattering and energy quantization are expected to strongly affect the impact ionization behavior. Therefore, advanced research should be needed for the sub-20-nm regime.

III. CONCLUSION

The hot-carrier characteristics for a multiple-gate FinFET were investigated. It was found that the nonlocal effect and series resistance are distinct features for the suppression of impact ionization in the narrow fin of the FinFET. The impact of the nonlocal effect and series resistance on impact ionization becomes stronger as the fin width decreases. Therefore, hot-carrier generation is reduced, and thus, the reliability is improved with fin width scaling. This, in turn, can allow for more aggressive scaling. From the conventional substrate current model, a refined analytical impact ionization model capturing the nonlocal effect and series resistance was developed and verified with measurement data.

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