An Intelligent Power Amplifier MMIC Using a New Adaptive Bias Control Circuit for W-CDMA Applications

Y. S. Noh, *Student Member, IEEE,* and Chul S. Park, *Member, IEEE*

***Abstract*—A high-linearity and high-efficiency MMIC power amplifier is proposed that adopts a new on-chip adaptive bias control circuit, which simultaneously improves efficiency at the low output power level and linearity at the high output power level. The adaptive bias control circuit detects the input power level and supplies a low quiescent current of 16 mA at the low output power level and an increased current up to 90 mA according to the increased power level adaptively. The intelligent W-CDMA power amplifier using the adaptive bias circuit exhibits an improvement of average power usage efficiency of more than 1.93 times, and an adjacent channel leakage ratio by 4 dB at the output power of 28.3 dBm.**

***Index Terms*—Adaptive bias control, heterojunction bipolar transistor (HBT), high efficiency, high linearity, MMIC, power amplifier, wide-band code-division multiple access (W-CDMA).**

I. Introduction

WIDE-BAND code-division multiple access (W-CDMA) is one of the leading standards for the third-generation (3G) wireless communication systems and adopts a spectrally efficient hybrid phase shift keying (HPSK) as a digital modulation scheme. But the nonconstant envelope of a W-CDMA signal requires the power amplifier to operate with a large amount of back-off to achieve high linearity. Also, power amplifiers require a high efficiency over a wide output power range for the overall power efficiency, because the most frequently used power level is not the maximum output power, but ranges from −20 to 15 dBm [1]. A back-off of the output power to the most probable output power creates a significant decrease in efficiency with a fixed dc power supply. Techniques for achieving high efficiency at the most probable output power have been in the spotlight recently as a key element in the designing of power amplifiers for mobile handsets. The power amplifier employing dc–dc converters [2]–[4] operates in near-saturation region at all power levels with a variable supply voltage to the input power, thereby generating higher efficiency. The switched gain stage power amplifier [5] bypasses the power stage for high efficiency at the low output power level. However, these techniques require additional components such as dc–dc converters or switches, which results in a significant increase of the module size, as well as increases in cost; these factors, therefore, make the power amplifier unsuitable for the mobile terminals.

With the conventional Class AB bias, it is difficult for power amplifiers to exhibit high efficiency at the low output power level, and high linearity at the high output power level. To overcome these problems, in this work we propose an on-chip adaptive bias control circuit. The adaptive bias control circuit supplies a low quiescent current at the low output power level for high efficiency, and the quiescent current increases adaptively with the input power to supply a higher quiescent current at the high output power level for high linearity. The adaptive bias control circuit has been successfully implemented to the W-CDMA power amplifier together with the capacitor linearizer [6]. The power amplifier shows an increase in average power usage efficiency by more than 1.93 times, while the maximum linear output power is increased by 2 dB with the linearizer, and an additional increase of 0.8 dB is obtained with the adaptive bias control circuit.

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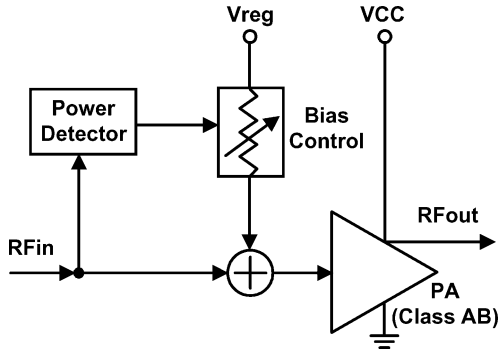

Fig. 1. Block diagram of the adaptive bias control system.

II. Adaptive Bias Control Circuit

The adaptively biased power amplifier for the output power level, such as a low quiescent current at the low output power level and the increasing quiescent current with output power level, is designed to simultaneously provide both high linear and efficient characteristics over a broad range of the output power. The operation principle of the adaptive bias control system is described in Fig. 1. The power detector senses the input power and controls the amount of quiescent current to the base of the power amplifier in proportion to the input power. Therefore, the power amplifier consistently maintains adequate quiescent current for the amplifier to operate in near-saturation region.

Fig. 2 shows the proposed adaptive bias control circuit. Transistor HBT2 senses the incoming input power, and the resistance of Rb and the emitter area of the HBT2 determine the amount of incoming power to the transistor HBT2. The base voltage of the HBT3 and HBT4 is determined as follows:

$$V_{B3} = V_{\mathrm{reg}} - (I_{\mathrm{C2}} + I_{B3})R2 - I_{B3}R3 \quad (1)$$

$$V_{B4} = V_{\mathrm{reg}} - (I_{\mathrm{C3}} + I_{B4})R1. \quad (2)$$

Transistors HBT1 and HBT2 are biased to Class AB with a low quiescent current for high efficiency at the low output power

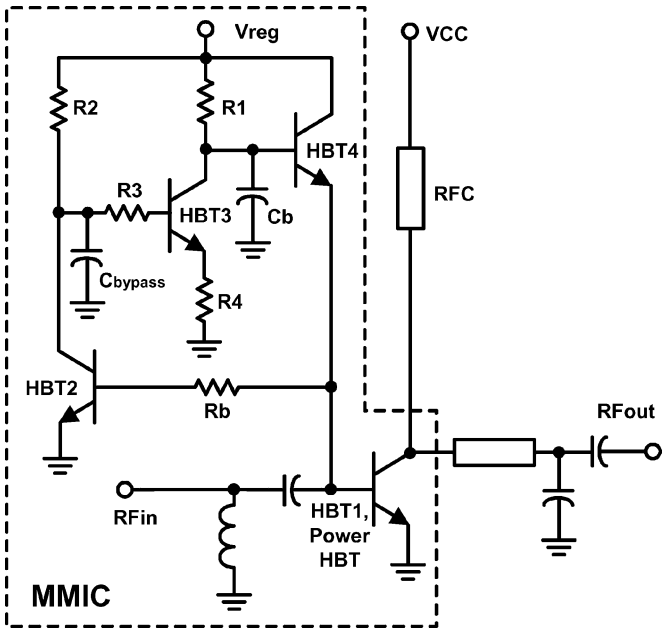

Fig. 2. Schematic diagram of the adaptive bias control circuit.

level; thus, the collector currents increase with the function of the input power. Therefore, the collector current of the HBT2 (I_{C2}) increases with the input power and the amplified power are bypassed through the capacitor C_{bypass}. The increased current of I_{C2} decreases the base voltage of the HBT3 (V_{B3}) in (1), hence, the collector current of the HBT3 decreases. Then, the decreased amount of I_{C3} increases the base voltage of the HBT4 (V_{B4}) in (2), forcing the emitter current of HBT4 and the collector current of HBT1 to increase. Thus, the quiescent current of the adaptive bias circuit is an increasing function of the input power, and the supply of the higher quiescent current over the conventional fixed bias at the high output power region results in high linearity with the tradeoff efficiency. Finally, high efficiency at the low output power level and high linearity at the high output power level can be achieved simultaneously. The resistor Rb and the emitter area of the HBT2 affect the overall operation of the adaptive bias control circuit. With a 0 Ω of Rb, the sensing transistor HBT2 has sufficient incoming RF power, then, I_{C2} starts to increase at the small input power of -2 dBm, decreasing the I_{C3} as shown in Fig. 3(a). However, a 400 Ω of Rb I_{C3} starts to decrease at the high input power of about 13 dBm. Fig. 4 shows the dependence of the collector current of HBT3 (I_{C3}) on the emitter area of HBT2 as a function of input power. Because the increasing amount of I_{C2} under Class AB operation is proportional to the emitter area of the HBT2, the slope of the I_{C3} curve with the 20-μm^2 emitter area of the HBT2 is the smallest. The shunt capacitor Cb (the function of which is described in detail in [6]) at the base node of HBT4 in Fig. 2 is used as a linearizer. The capacitor with the base–emitter diode of the transistor (HBT4) compensates the decreased base bias voltage of the HBT1 caused by the increased input power.

III. Implementation in the W-CDMA MMIC Power Amplifier

A W-CDMA MMIC power amplifier that implements the proposed adaptive bias control circuit and the conventional bias

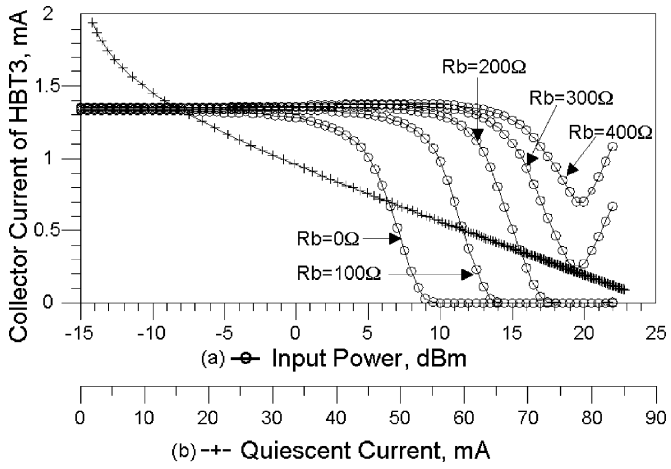

Fig. 3. Simulated collector current of HBT3. (a) As a function of input power to the power amplifier for five different resistor values of Rb. (b) As a function of quiescent current of HBT1.

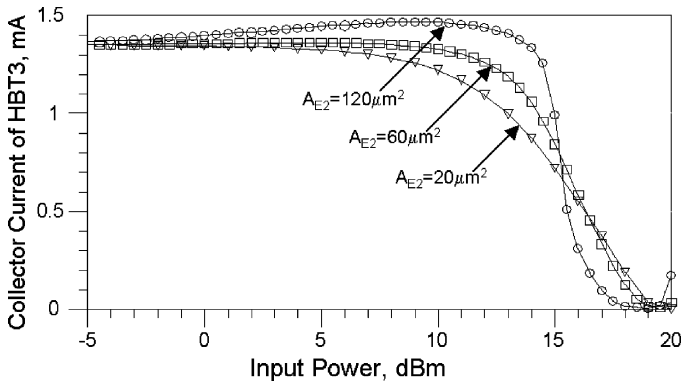

Fig. 4. Simulated collector current of HBT3 as a function of input power for the three different emitter areas of HBT2.

circuit has been fabricated. As shown in Fig. 5, the adaptive bias control circuit does not show any significant increase in chip area and the total MMIC size is 0.69×0.75 mm^2. The MMIC power amplifier is demonstrated using 48 fingers with a unit emitter area of 60 μm^2 InGaP/GaAs heterojunction bipolar transistor (HBT), and 250 Ω of Rb and 60 μm^2 emitter area of the HBT2 in Fig. 2 are used. The integrated high pass-matching network is used in the input matching network for low-frequency stability, and the off-chip output-matching network consists of a low-pass filter in order to exclude harmonic distortions, as shown in Fig. 2.

IV. Measurement Results

Fig. 6 shows the measured gains and adjacent channel leakage ratios (ACLRs) with the linearizer (shunt capacitor Cb in Fig. 2), and without the linearizer as a function of the output power under a fixed 56-mA quiescent current with a 3.4-V supply voltage. The ACLR is measured using a 3.84-Mcps W-CDMA modulated signal (DPCCH + 1DPDCH) in a 5-MHz offset frequency band. The 1-dB gain compression output power with the linearizer is increased as much as 5 dB compared to that without the linearizer (from 22.5 to 27.5 dBm). The ACLR with the linearizer is improved as much as 7 dB compared to that without the linearizer (from -28 to

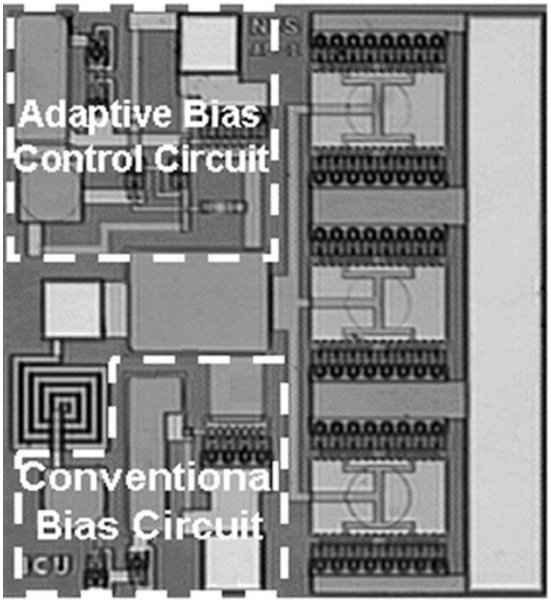

Fig. 5. Photograph of the fabricated HBT MMIC power amplifier.

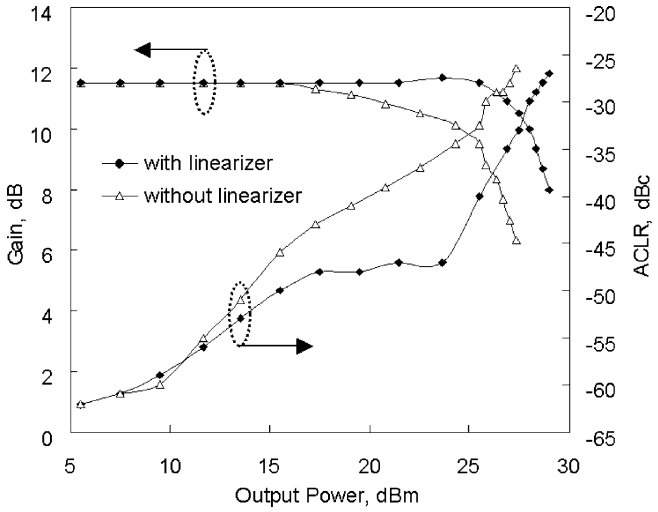

Fig. 6. Measured gain and ACLR of the power amplifier with the linearizer and without the linearizer.

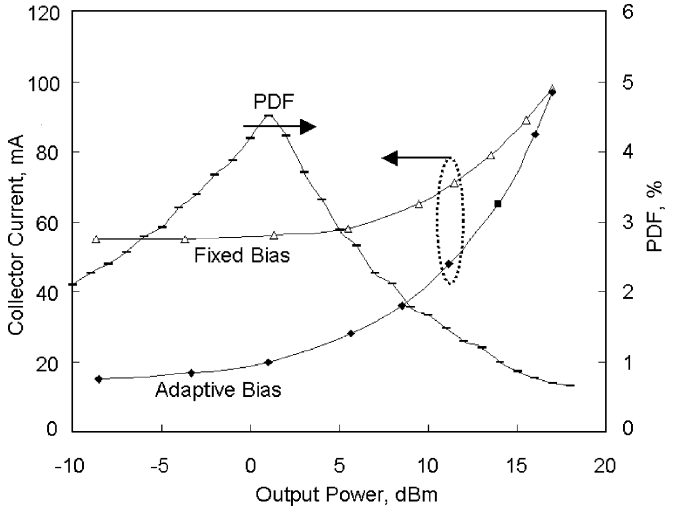

Fig. 7. Measured collector current of the power amplifier with the adaptive bias and the fixed bias circuit, both with linearizer. Power amplifier PDF based on an IS-95 CDMA urban environment [1].

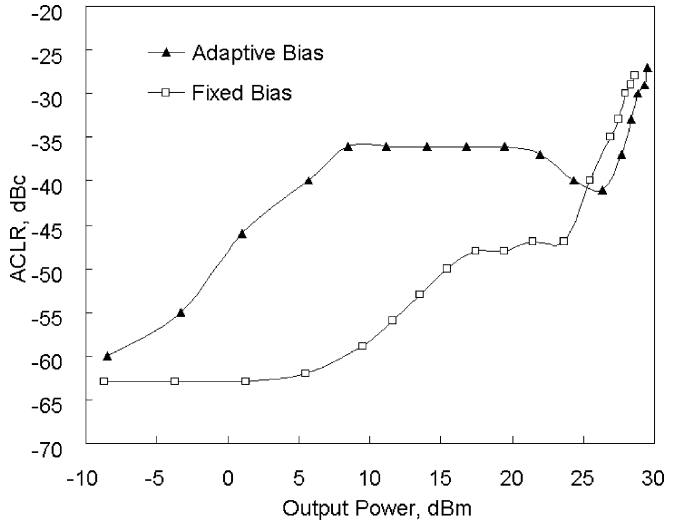

Fig. 8. Measured ACLR of the power amplifier with the adaptive bias and the fixed bias circuit, both with linearizer.

−35 dBc) at the output power of 27 dBm. The measured quiescent current of the power amplifier with the adaptive bias circuit is 16 mA under the 3.4-V supply voltage, and the measured collector current as a function of output power is shown in Fig. 7 in comparison with the fixed Class AB power amplifier with the 56-mA quiescent current. In addition, the power amplifier probability distribution function (PDF) [1] based on an IS-95 CDMA urban environment is illustrated in Fig. 7. The adaptively biased power amplifier consumes the collector current at less than half of the fixed bias in the case of 5-dBm output power, thereby generating higher efficiency in the most probable output power range.

The measured ACLR of the adaptive bias shows better linearity at the high output power level due to the increased quiescent current, as depicted in Fig. 8. With the adaptive bias circuit, the maximum linear output power exhibiting an ACLR of −33 dBc increases as much as 0.8 dB compared to the fixed bias (from 27.5 to 28.3 dBm).

Fig. 9 shows the measured gain and power-added efficiency (PAE) of the power amplifier with the adaptive bias and fixed bias circuit as a function of output power. The gain is 6.5 dB for the low output power and increases to 12.3 dB at the output power of 24 dBm with the adaptive bias circuit. A gain expansion of up to 5.8 dB occurs at the high output power region due to the high quiescent current with the adaptive bias current control. PAE is measured as 52.4% (56.6%) at the 28.3-dBm output power with the adaptive (fixed) bias circuit. The 4.2% decrease of PAE is a tradeoff with the ACLR increase of 4 dB, and the decrease of PAE at the high output power level does not significantly affect the overall efficiency because the power amplifier PDF has a low value.

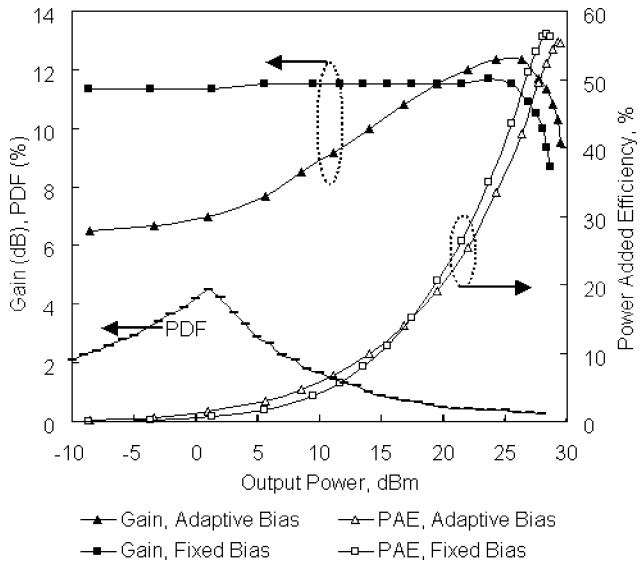

Fig. 9. Measured gain and power-added efficiency of the power amplifier with the adaptive bias and the fixed bias circuit, and power amplifier PDF.

TABLE I
MEASURED PERFORMANCES FOR −33-dBc ACLR WITH W-CDMA MODULATED SIGNAL

Bias Condition	Pout, dBm	PAE, %
Fixed bias without linearizer	25.5	49.7
Fixed bias with linearizer	27.5	54
Adaptive bias with linearizer	28.3	52.4

To evaluate efficiency improvement, average power usage efficiency in [7] is defined by

$$\eta_{\text{usage}} = \frac{\overline{P_{\text{out}}}}{\overline{P_{\text{in}}}} \tag{3}$$

where $\overline{P_{\text{in}}}$ and $\overline{P_{\text{out}}}$ are the average RF output power and input dc power with the power amplifier PDF, respectively. The average power usage efficiency is calculated as high as 11.82% (6.1%) with the adaptive (fixed) bias circuit. Table I summarizes the measured output power and PAE for an ACLR of −33 dBc in three different bias conditions. The linearizer improves the output power by 2 dB and the PAE by 4.3%; the adaptive bias control circuit improves the output power by 0.8 dB, which is a tradeoff with the PAE decrease of 1.6%.

V. CONCLUSION

An on-chip adaptive bias circuit controlling the quiescent current adaptively to the power level is proposed for high efficiency and linearity. The adaptive bias control circuit supplies a low quiescent current to the power amplifier when the input power is small and this current automatically increases according to the power level. A W-CDMA MMIC power amplifier with the proposed adaptive bias control circuit achieves an average power usage efficiency improvement of more than 1.93 times, and an ACLR improvement of 4 dB with a small quiescent current of 16 mA under a 3.4-V supply voltage. The adaptive bias circuit is very attractive in a mobile handset power amplifier because it is integrated on a chip in a small area.

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