A Low-Power ROM Using Single Charge-Sharing Capacitor and Hierarchical Bit Line

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***Abstract*—This paper describes a low-power read-only memory (ROM) using a single charge-sharing capacitor (SCSC) and hierarchical bit line (HBL). The SCSC-ROM reduces the power consumption in bit lines. It lowers the swing voltage of bit lines to a minimal voltage by using a charge-sharing technique with a single capacitor. It implements the capacitor with dummy bit lines to improve noise immunity and to make it easier to design. Furthermore, the HBL saves power by reducing the capacitance and leakage current in bit lines. The SCSC-ROM also reduces the power consumption in control unit and predecoder by using the hierarchical word line decoder. The simulation result shows that the SCSC-ROM with 4 K $\times$ 32 bits consumes only 37% power of a conventional ROM. An SCSC-ROM chip is fabricated in a 0.25-μm CMOS process. It consumes 8.2 mW at 240 MHz with 2.5 V.**

***Index Terms*—Bit line, charge-sharing, low power, ROM, word line decoder.**

I. Introduction

As MOBILE systems are popular and widely used, power consumption has become an important design criterion of VLSI chips. In practice, embedded memories such as static random access memory (SRAM) and read-only memory (ROM) consume a great deal of power in mobile systems. ROM is an important part of many digital systems such as digital signal processors, microprocessors, and digital filters. ROM consumes a lot of power because it has many highly capacitive lines and it is frequently accessed. Fig. 1 shows a conventional ROM architecture. The ROM core dissipates most of the power because word lines and bit lines have a large capacitance due to a large number of cell transistors and many bit lines that are selected for each access.

Many techniques have been proposed to reduce the power consumption in the highly capacitive lines of ROMs [1]–[7]. Some techniques focus on decreasing the capacitances of bit lines and word lines [1]. This can be achieved by the nonzero term minimization which reduces the number of transistors in the ROM core. It reduces power consumption without losing performance but the amount of the saved power is small. Other techniques focus on lowering the swing voltage of the bit lines [1]–[7]. They can save a lot of power because the power is dissipated in proportion to the swing voltage of the bit lines.

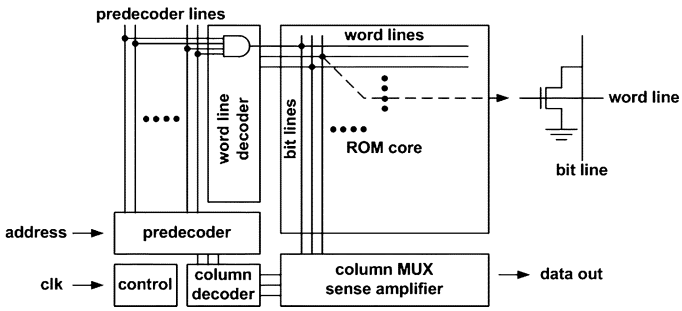

Fig. 1. Conventional ROM architecture.

Recently, the charge-recycling and charge-sharing ROM (CRCS-ROM) was proposed to reduce the power consumption in bit lines, word lines, and predecoder lines [4], [5]. It saves the power in bit lines by using the charge-sharing technique. It reduces the swing voltage of bit lines by using three small capacitors per output. Although the swing voltage of bit lines of the CRCS-ROM is significantly reduced, it must be double the size of the sensing voltage of sense amplifiers. Moreover, the CRCS-ROM is vulnerable to noises because it requires many small capacitors.

In this paper, a single charge-sharing capacitor ROM (SCSC-ROM) is proposed to save the power in bit lines. The SCSC-ROM reduces the swing voltage of bit lines by using a single charge-sharing capacitor. The swing voltage can be reduced to the sensing voltage of sense amplifiers. The swing voltage of the SCSC-ROM is half that of the CRCS-ROM. The SCSC is implemented by dummy bit lines so that the SCSC-ROM is not only robust against noises but also easy to design. The hierarchical bit line (HBL) and hierarchical word line decoder also are proposed to reduce power consumption of the SCSC-ROM. The HBL saves the power in the bit line (BL) by reducing the capacitance of the BL to about a half of the conventional BL. Moreover, the HBL improves the noise margin and saves the power by reducing the leakage current of the BL. The hierarchical word line decoder reduces the power consumption of the control unit and predecoder.

The organization of this paper is as follows. In Section II, we propose the SCSC-ROM using the single charge-sharing capacitor, the HBL, and the hierarchical word line decoder. In Section III, we present performance comparisons and show test results of the fabricated chip. This paper is finished with the conclusion in Section IV.

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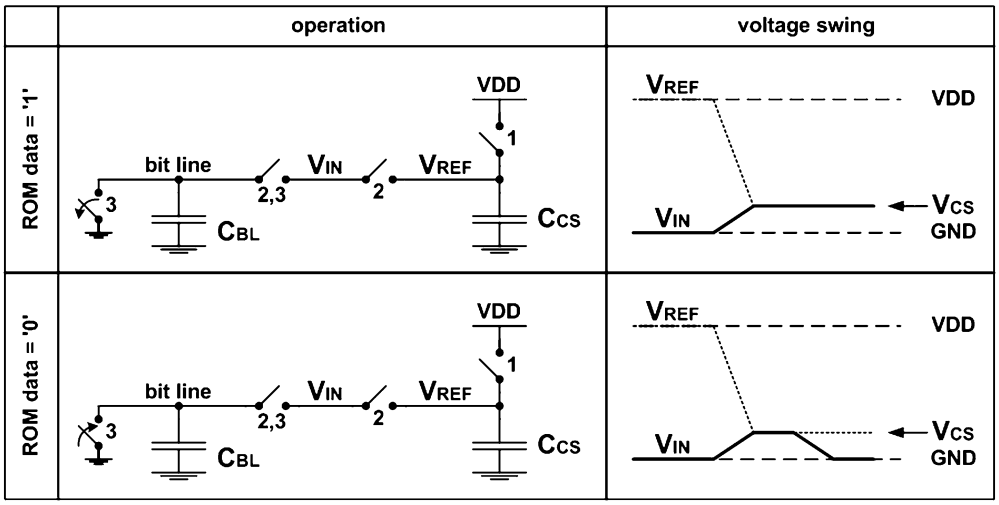

Fig. 2. Concept of the SCSC-ROM.

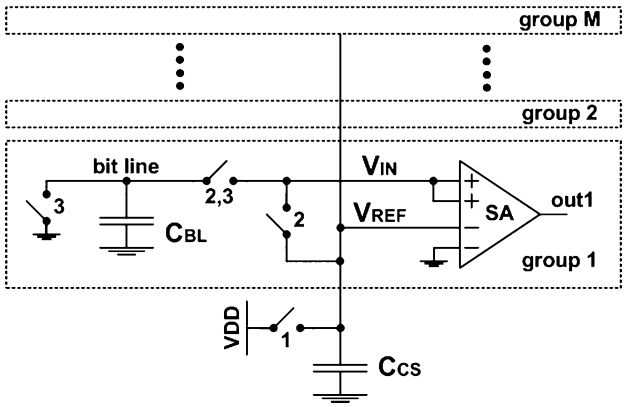

Fig. 3. Simplified architecture of the SCSC-ROM.

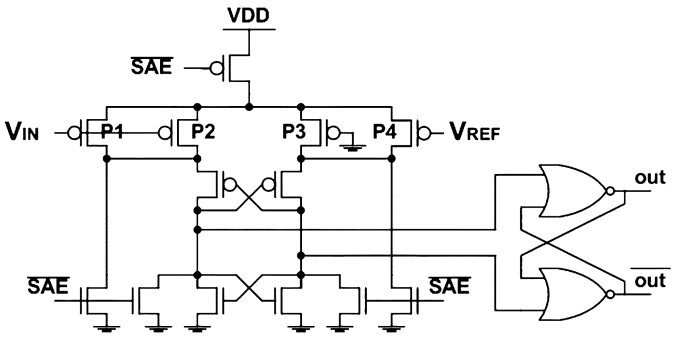

Fig. 4. Sense amplifier used in the SCSC-ROM.

II. Architecture

A. Architecture of the SCSC-ROM

Figs. 2 and 3 show the concept and simplified architecture of the SCSC-ROM, respectively. All switches in the figures represent transistors. A transistor connected to $V_{\rm DD}$ is a PMOS transistor and the other transistors are NMOS transistors. The numbers on the switches show four timing stages (precharge, charge-sharing, evaluation, and sensing) when the transistors are turned on. As shown in Fig. 2, the SCSC-ROM reduces the swing voltage of bit lines with a single charge-sharing capacitor $C_{\rm CS}$. The swing voltage of bit lines becomes the charge-sharing voltage $V_{\rm CS}$ by the charge-sharing between all selected bit lines and $C_{\rm CS}$, as shown in Fig. 3. $V_{\rm CS}$ becomes very small voltage because the total capacitance of the selected bit lines is much larger than $C_{\rm CS}$. Therefore, the power consumption in each selected BL becomes very small.

The operation of the SCSC-ROM is as follows. 1) At the precharge stage, all bit lines are at ground and $C_{\rm CS}$ is precharged to $V_{\rm DD}$. 2) At the charge-sharing stage, a selected BL per group is connected to $C_{\rm CS}$ for the charge-sharing operation. When the number of groups is M, the selected M bit lines are connected to $C_{\rm CS}$. At this time, M bit lines and $C_{\rm CS}$ share their charges. After the charge-sharing, the voltages of the bit lines and $C_{\rm CS}$ become the charge-sharing voltage $V_{\rm CS}$ and the BL consumes power $P_{\rm BL}$ where $C_{\rm BL}$ is the capacitance of the BL and f is the operating frequency

$$V_{\rm CS} = C_{\rm CS} \times V_{\rm DD}/(M \times C_{\rm BL} + C_{\rm CS})$$
$$P_{\rm BL} = f \times C_{\rm BL} \times V_{\rm CS} \times V_{\rm DD}.$$

The swing voltage and power consumption of the BL are very small because $C_{\rm CS}$ is much smaller than $M \times C_{\rm BL}$. (3) At the evaluation stage, a word line is selected. If ROM data is "1," the voltage of the BL remains $V_{\rm CS}$. If ROM data is "0," the voltage of the BL becomes ground. The selected BL is connected to the node $V_{\rm IN}$. As a result, $V_{\rm IN}$ becomes $V_{\rm CS}$ or ground according to the ROM data. (4) At the sensing stage, the dual-reference PMOS current-latch sense amplifier in Fig. 4 detects the ROM data from the small swing voltage of the BL [3]. In the sense amplifier, two PMOS transistors P1 and P2 are connected to $V_{\rm IN}$. The other two PMOS transistors P3 and P4 are connected to ground and the reference voltage $V_{\rm REF}$, respectively. $V_{\rm REF}$ is $V_{\rm CS}$ because the voltage of $C_{\rm CS}$ is used for $V_{\rm REF}$. If $V_{\rm IN}$ is $V_{\rm CS}$, P1 and P2 flow less current than P3 and P4 because the PMOS transistors connected to $V_{\rm CS}$ flow less current than the PMOS transistors connected to ground. The output of the sense amplifier becomes "1." If $V_{\rm IN}$ is at ground, P1 and P2 flow

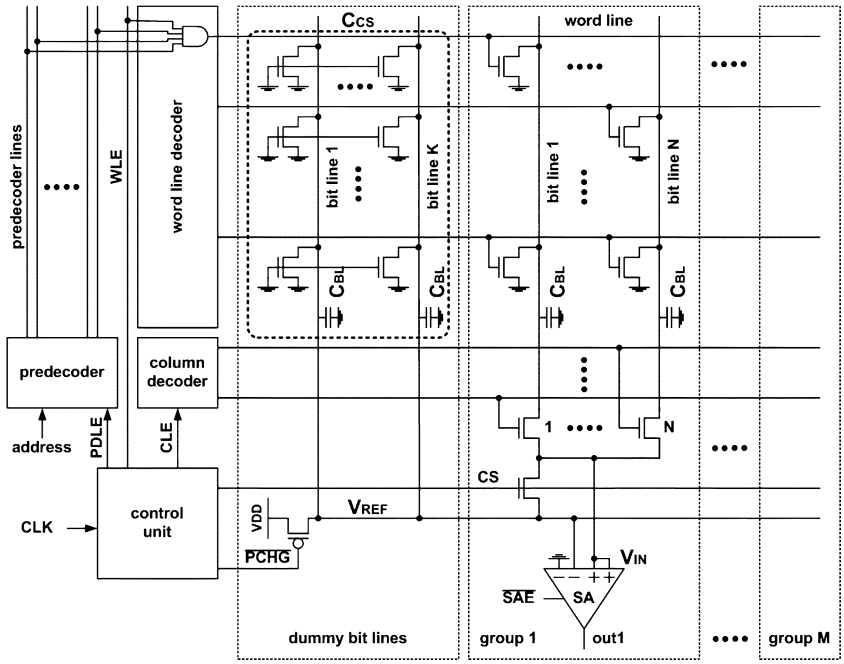

Fig. 5. Architecture of the SCSC-ROM.

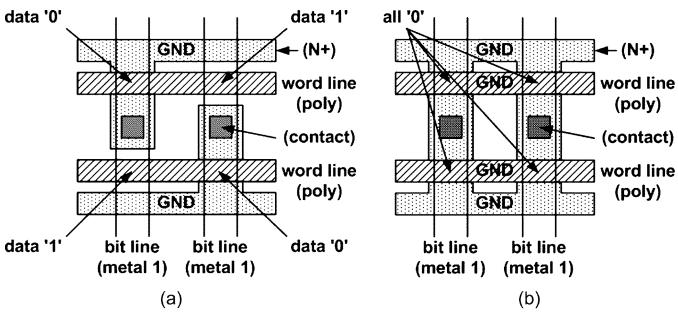

Fig. 6. ROM cell layout. (a) Bit lines. (b) Dummy bit lines.

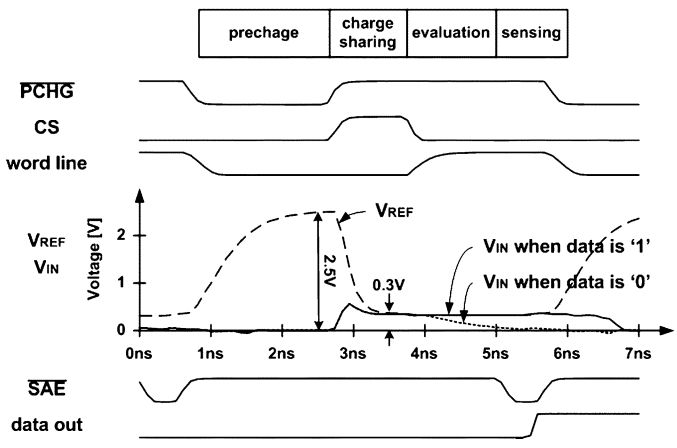

Fig. 7. Simulated waveforms of the SCSC-ROM.

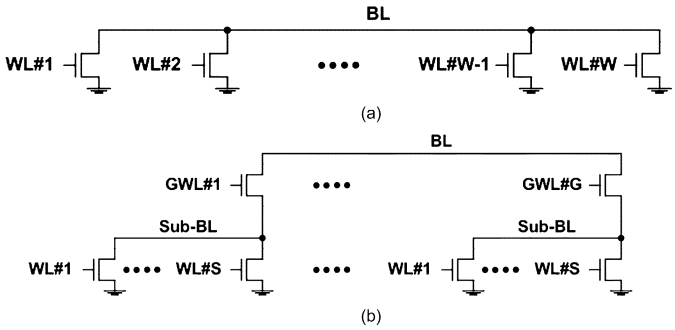

Fig. 8. Architectures of (a) conventional BL and (b) HBL.

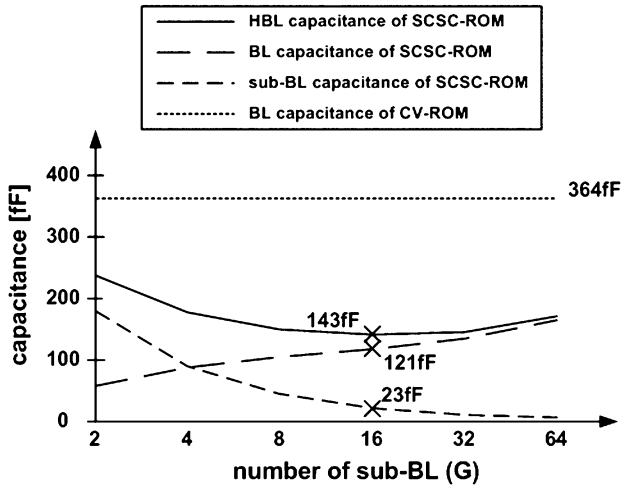

Fig. 9. Capacitance comparisons of BLs.

more current than P3 and P4. The output of the sense amplifier becomes "0."

Fig. 5 shows the architecture of the SCSC-ROM. It consists of a control unit, a predecoder, a word line decoder, a column

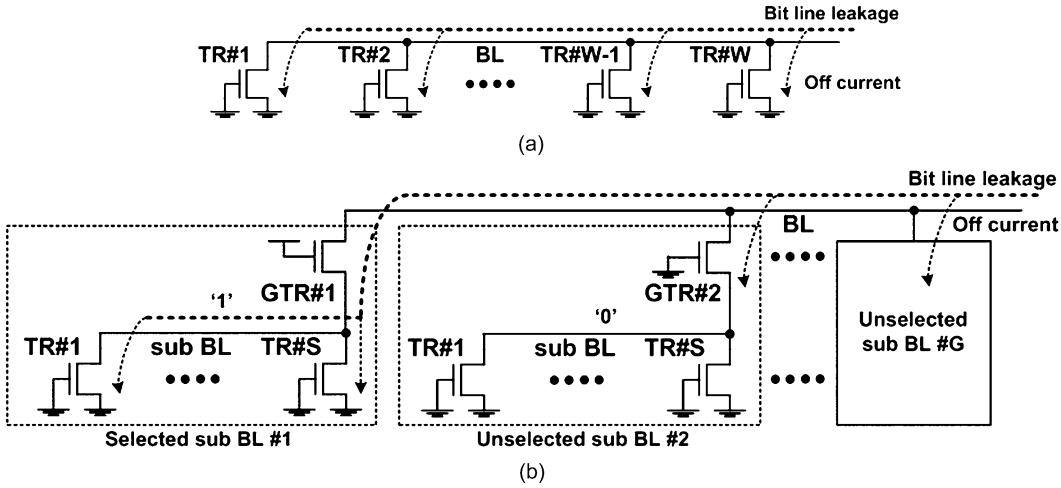

Fig. 10. Leakage currents in (a) conventional BL and (b) HBL.

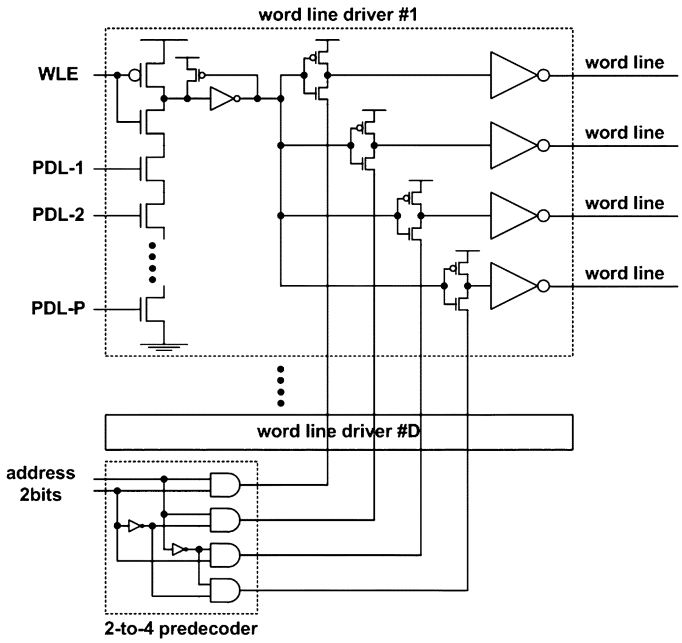

Fig. 11. Conventional word line decoder.

decoder, ROM cells, and sense amplifiers. It has M groups and each group contains N bit lines. Additionally, it has K dummy bit lines to implement the charge-sharing capacitor $C_{\rm CS}$.

The SCSC-ROM uses the conventional diffusion programming ROM cells in Fig. 6(a) because all bit lines have almost the same capacitance $C_{\rm BL}$ independent of the programmed data. The dummy bit lines also have the same capacitance $C_{\rm BL}$. $C_{\rm CS}$ consists of K dummy bit lines. Therefore, the size of $C_{\rm CS}$ is K times larger than $C_{\rm BL}$ and the charge-sharing voltage $V_{\rm CS}$ becomes independent of the physical size of $C_{\rm BL}$

$$\begin{aligned} C_{\rm CS} &= K \times C_{\rm BL} \\ V_{\rm CS} &= C_{\rm CS} \times V_{\rm DD}/(M \times C_{\rm BL} + C_{\rm CS}) \\ &= K \times C_{\rm BL} \times V_{\rm DD}/(M \times C_{\rm BL} + K \times C_{\rm BL}) \\ &= K/(M+K) \times V_{\rm DD}. \end{aligned}$$

$V_{\rm CS}$ is easily controlled by M and K. The designers do not need to consider the physical sizes of $C_{\rm BL}$ and $C_{\rm CS}$ to select $V_{\rm CS}$ for the sense amplifier. Although the real size of $C_{\rm CS}$ is slightly larger than $K \times C_{\rm BL}$ because $C_{\rm CS}$ is connected to all sense amplifiers in M groups, the additional capacitance is much smaller than $K \times C_{\rm BL}$. Therefore, this slightly increases $V_{\rm CS}$ and power consumption. The increased $V_{\rm CS}$ does not affect the operation of the SCSC-ROM.

Fig. 6(a) and (b) shows the layouts of the bit lines and dummy bit lines, respectively. The capacitance of the BL is a little different according to the programmed data. The "0" programmed cell has slightly larger capacitance than the "1" programmed cell. When all cells connected to the BL are "0" programmed cells, the BL has the maximum capacitance. To guarantee that the swing voltage of the BL is higher than the calculated $V_{\rm CS}$, the capacitance of the dummy BL must larger than that of the BL. Therefore, all cells connected to the dummy bit lines are "0" programmed cells, as shown in Fig. 6(b). The transistors connected to the dummy bit lines are not turned on because they are used for the capacitor $C_{\rm CS}$. Their gates are connected to ground.

Fig. 7 shows the simulated waveforms of the SCSC-ROM with 4 kB $\times$ 32 bits. The SCSC-ROM has 32 groups, 256 bit lines, and 4 dummy bit lines ($M = 32, N = 8, K = 4$). All circuit simulation is based on a 0.25-μm CMOS process with $V_{\rm DD}$ =2.5 V. The SCSC-ROM operates according to the four time stages (precharge, charge-sharing, evaluation, and sensing) with four control signals *(/PCHG*, *CS*, *WLE*, and */SAE)*. (1) At the precharge stage, the */PCHG* signal becomes "0" and $C_{\rm CS}$ is charged to $V_{\rm DD}$ by a PMOS transistor. Therefore, V_{REF} becomes 2.5 V. (2) At the charge-sharing stage, the *CS* signal becomes "1" and M bit lines and $C_{\rm CS}$ share their charges. Both V_{REF} and $V_{\rm IN}$ become the charge-sharing voltage $V_{\rm CS}$

$$\begin{aligned} V_{\rm CS} &= K/(M+K) \times V_{\rm DD} \\ &= 4/(32+4) \times 2.5\ {\rm V} = 0.28\ {\rm V}. \end{aligned}$$

$V_{\rm CS}$ is easily calculated by K and M without considering the real sizes of $C_{\rm BL}$ and $C_{\rm CS}$. However, the real swing voltage of the BL is slightly higher than the calculated $V_{\rm CS}$ due to the parasitic capacitances from the interconnection lines, the precharge

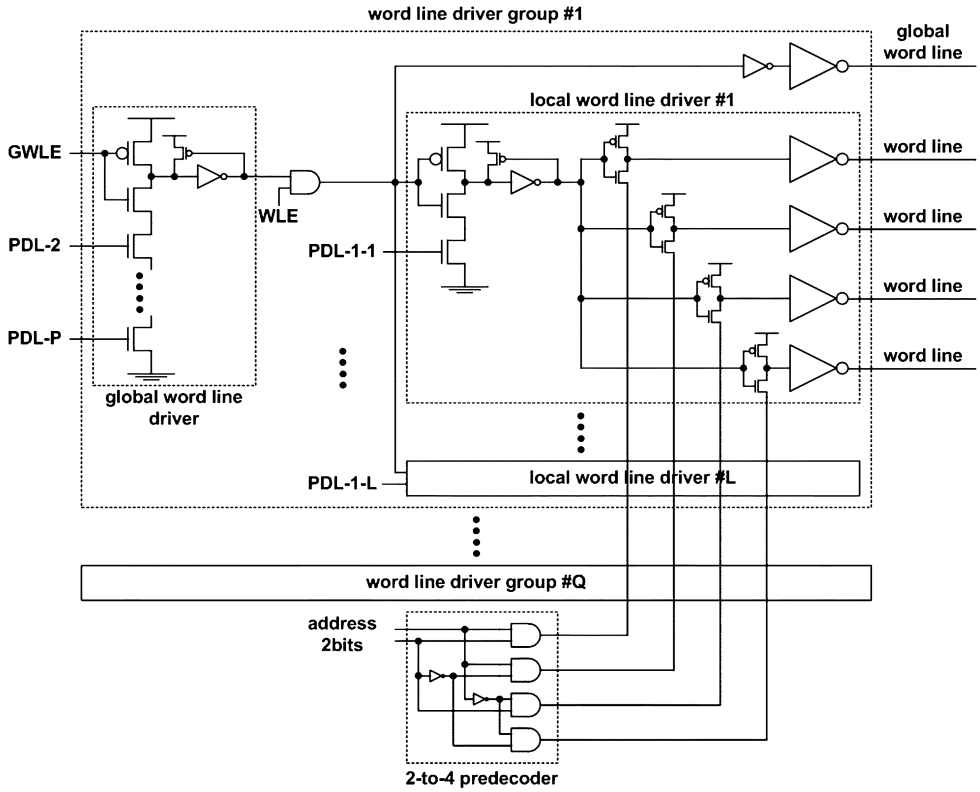

Fig. 12. Hierarchical word line decoder.

PMOS transistor, the charge-sharing transistors, and the sense amplifiers. In the simulation, $V_{\rm CS}$ becomes about 0.3 V. (3) At the evaluation stage, the *WLE* signal becomes "1" and a word line is selected. When the ROM data is "1," $V_{\rm IN}$ remains $V_{\rm CS}$. When the ROM data is "0," $V_{\rm IN}$ returns ground. (4) At the sensing stage, the */SAE* signal becomes "0" and the sense amplifier detects the ROM data.

The four control signals *(/PCHG*, *CS*, *WLE*, and */SAE*) are generated by the clock and delay circuits. The pulse durations for the *CS* and */SAE* are generated by the fixed delay circuits because they are short. The remained times from the clock are used for the */PCHG* and *WLE*. Therefore, the timing circuits are quite simple.

B. Hierarchical Bit Line

Fig. 8(a) and (b) shows the architectures of the conventional BL and the HBL, respectively. The HBL divides the conventional BL having $W\ (=S\times G)$ cell transistors into G sub bit lines (sub-BLs) having S cell transistors. Each sub-BL is connected to the BL through an NMOS transistor which is turned on by the global word line (GWL). The BL and sub-BLs are implemented in different metal lines. The BL runs above its sub-BLs. The G and S transistors are connected to the BL and the sub-BL, respectively. One of the global word lines becomes high and it selects which sub-BL is connected to the BL. As a result, $G+S$ transistors connected to the HBL including the BL and the selected BL. Therefore, the number of transistors connected to the BL is reduced from $S\times G$ to $S+G$. The capacitance of BL consists of drain capacitances of transistors and metal line capacitance of BL. The metal line capacitances of the conventional and HBLs are almost the same but the HBL has much smaller drain capacitance than the conventional BL. Therefore, the HBL reduces the effective capacitance of BLs.

Fig. 9 shows the capacitance comparisons of BLs according to the number of sub-BLs (G) where the BL has 512 cell transistors. As G increases, the capacitance of sub-BLs decreases because the number of cell transistors and the length of the metal line of the sub-BL are proportional to $1/G$. However, the capacitance of the BLs increase because the length of the metal line of the BLs are almost the same and the number of the transistors connected to the BL are G. The total capacitance of the HBL composed of the BL and the sub-BL is much smaller than that of the conventional BL. Although the capacitance, due to the metal line, is almost the same as that of the conventional BL, the number of transistors connected to the BL is reduced from $S\times G$ to $S+G$. When G is 16, the number of transistors in the sub-BL (S) is 32. The number of transistors connected to the BL is reduced from 512 to 48, which is only 9.4% of the conventional BL. The capacitance of the HBL is 39% of the conventional BL due to the similar capacitance of metal lines. The power consumption of the BL is proportional to the BL capacitance. Therefore, the HBL can save lots of power.

The delay of the HBL is almost the same as the conventional BL. The HBL has the capacitance under a half of the conventional BL. However, the HBL is discharged through two NMOS transistors whereas the conventional BL is discharged through an NMOS transistor. The resistance of the discharge transistor of the hierarchical bit is two times of the conventional BL. The

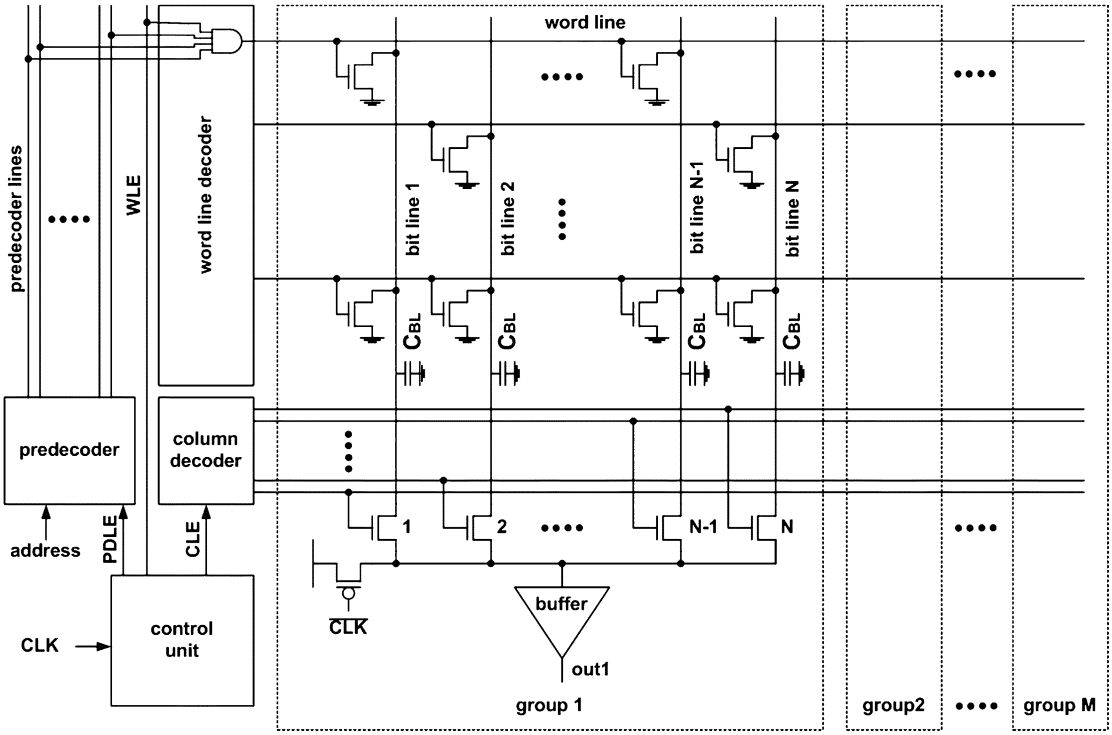

Fig. 13. Conventional low-power ROM (CV-ROM).

delay of the BL is proportional to the product of the BL capacitance and the resistance of the discharge transistor. Therefore, the delay of the HBL is similar to the conventional BL.

Fig. 10(a) and (b) shows the leakage current in the conventional BL and the HBL, respectively. The leakage current in deep sub micron technologies becomes a dominant factor in the power consumption. Moreover, the increased leakage current causes the operation failures in the dynamic circuits. Especially, the ROM uses a wide-OR dynamic circuit. The leakage current increases in proportion to the number of transistors connected to the BL. At first, the BL is precharged to $V_{\rm CS}$. At the evaluation time, if the ROM data is "1," all transistors are turned off. The BL must remain at the precharged voltage. However, when the leakage current is large, the voltage of the BL decreases. In the worst case, the voltage of the BL becomes lower than $V_{\rm CS}/2$. The output changes from "1" to "0." Its operation fails. Therefore, the leakage reduction is very important in the ROM. The HBL simply reduces the leakage current of the BL from $(S \times G) \times {\rm I}_{\rm OFF}$ to $(S + G - 1) \times {\rm I}_{\rm OFF}$, where ${\rm I}_{\rm OFF}$ is the leakage current of an NMOS transistor, as shown in Fig. 10(b). In the selected sub-BL, the leakage current flows through S transistors. The leakage current of the BL flows through $G-1$ transmission transistors connected to $G-1$ unselected sub-BLs. Actually, the leakage currents $({\rm I}_{\rm OFF})$ of the hierarchical and the conventional BL architectures are different. The magnitude of the leakage current of the HBL is greatly reduced by stacking the two NMOS transistors due to the body effect. Therefore, the leakage current of the HBL is less than $(S + G - 1) \times {\rm I}_{\rm OFF}$.

C. Hierarchical Word Line Decoder

Fig. 11 shows the conventional word line decoder. It consists of a lot of word line drivers. Each word line driver has four word lines. A 2-to-4 predecoder selects which word line is enabled among the four word lines. P predecoder lines $({\rm PDL}-1 \sim {\rm PDL}-P)$ are connected to each word line driver. The word line enable (WLE) signal is connected to two transistors for each word line driver. The number of transistors connected to the WLE signal is half of the number of word lines. Since all word line drivers are enabled by the WLE signal, more power is consumed by the WLE signal. The predecoder lines also consume more power because each predecoder line is connected to a large number of word line drivers.

Fig. 12 shows the hierarchical word line decoder. It reduces the power consumption in the WLE signal and predecoder lines. Each word line driver block consists of a global word line driver and L local word line drivers. Each local word line driver has four word lines. The WLE signal drives only the global word line drivers instead of all local word line drivers. The number of transistors connected to the WLE signal of the hierarchical word line decoder is reduced to $1/L$ of the conventional word line decoder. Moreover, the number of transistors connected to $P-1$ predecoder lines $({\rm PDL}-2 \sim {\rm PDL}-P)$ is reduced to $1/L$. Therefore, the hierarchical word line decoder significantly reduces the power consumption in the WLE signal and predecoder lines.

When the conventional word line decoder is used for 512 word lines, the number of word line drivers is 128 $(D = 128)$. The number of transistors connected to the WLE signal is $256(D \times 2)$. Three predecoder lines $({\rm PDL}-1 \sim {\rm PDL}-3)$ are connected to each word line driver. A 3-to-8 predecoder with 8 predecoder lines is used for the PDL-1. The number of transistors connected to each predecoder line of the PDL-1 is 16 $(D/8)$. Two 2-to-4 predecoders with 4 predecoder lines are used for the PDL-2 and PDL-3. The number of transistors

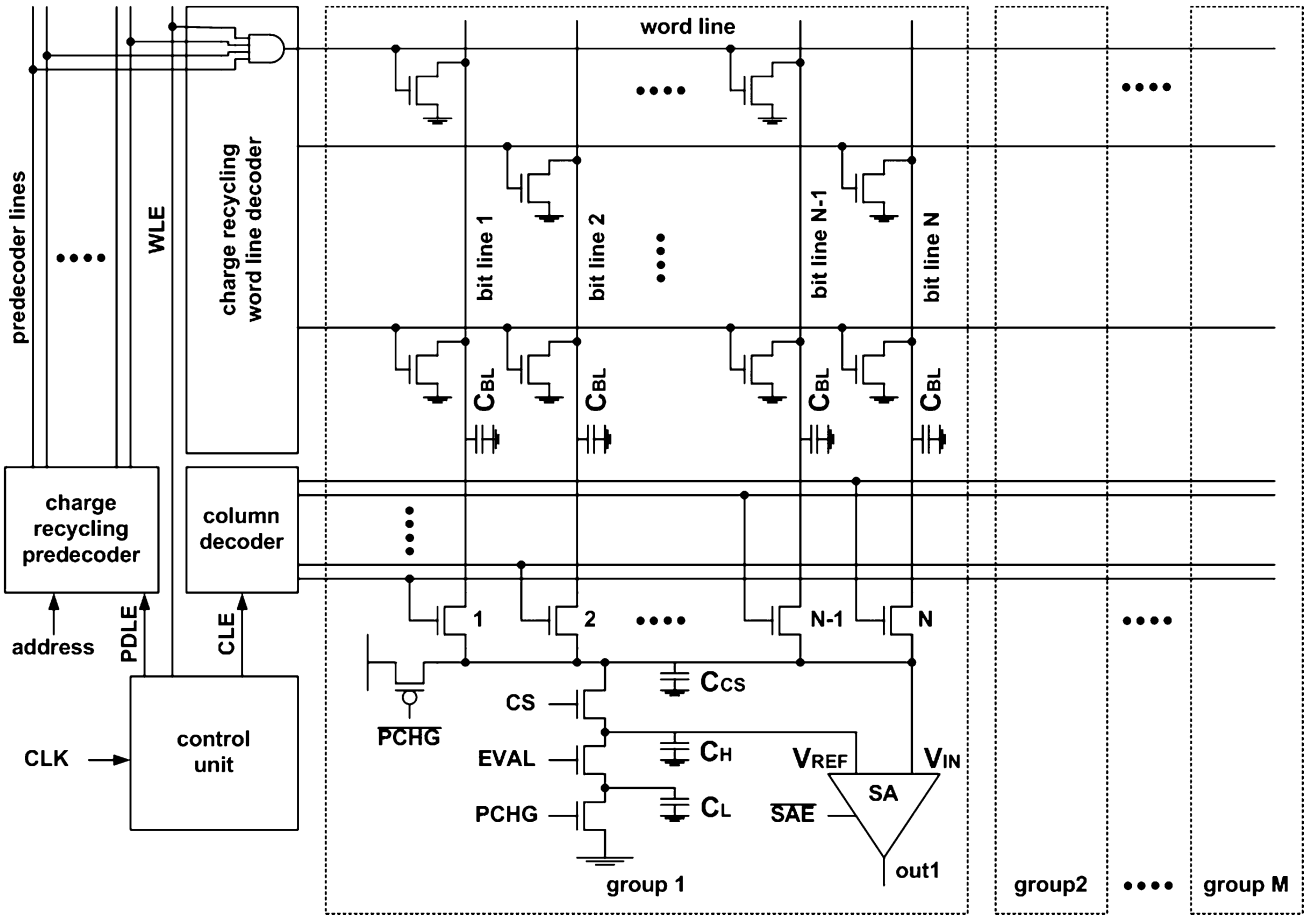

Fig. 14. CRCS-ROM.

connected to each predecoder line of the PDL-2 and PDL-3 is 32 $(W/4)$. However, when the hierarchical word line decoder is used for 512 word lines, each word line driver block consists of a global word line driver and 8 local word line drivers $(L = 8)$ because the 3-to-8 predecoder with 8 predecoder lines is used for the PDL-1. The number of transistors connected to the WLE signal is reduced to 32 $(256/L)$ from 256. Moreover, the number of transistors connected to the PDL-2 and PDL-3 are reduced to $4(32/L)$ from 32.

The power reductions due to the hierarchical word line are shown in Table I. The power of the predecoder is reduced from 0.6 mW of the CV-ROM to 0.53 mW of the SCSC-ROM. The power of the control unit including the WLE signal is reduced from 0.88 mW of the CV-ROM to 0.66 mW of the SCSC-ROM without the HBL. The control unit of the SCSC-ROM consumes 0.78 mW because the SCSC-ROM uses the GWLE signal additionally.

III. Performance Comparison and Test Results

A. Performance Comparisons

The conventional low-power ROM (CV-ROM) [1], the charge recycling and charge-sharing ROM (CRCS-ROM) [4], [5], and the proposed SCSC-ROM are implemented for the comparisons. All circuit simulations are based on a 0.25-μm CMOS process and HSPICE model. The extracted capacitances and resistances from layouts are included in the simulations.

Fig. 13 shows the CV-ROM. It uses conventional low-power techniques such as selective precharge, NMOS precharge, and diffusion programming ROM core. A BL per group is selectively precharged to $V_{\rm DD} - V_{\rm T}$ instead of $V_{\rm DD}$ by using NMOS transistors for the column selection. It reduces the power consumption in the bit lines by limiting the voltage swing of bit lines to $V_{\rm DD} - V_{\rm T}$. The diffusion programming ROM core reduces both cell area and BL capacitance compared to the contact programming ROM core.

Fig. 14 shows the CRCS-ROM. It uses a charge-sharing bit line (CSBL), a charge recycling predecoder (CRPD), and a charge recycling word line decoder (CRWLD). The CSBL is similar to the charge-sharing technique used in the SCSC-ROM. However, it needs three small capacitors per group for the charge-sharing operation. It reduces the swing voltage of bit lines to the charge-sharing voltage between a BL and a charge-sharing capacitor $C_{\rm CS}$. Two additional small capacitors $C_{\rm H}$ and $C_{\rm L}$ are used to make the reference voltage of the sense amplifier. The reference voltage is one half of the charge-sharing voltage. Therefore, the charge-sharing voltage must be larger than twice the minimum sensing voltage of the sense amplifier. The CRPD and CRWLD recycle the previously used charges in predecoder lines and word lines, respectively. The power consumption in the predecoder lines and word lines are theoretically reduced to a half. However, the saved amount is smaller than one half due to the control overheads. The CRPD and CRWLD also incur significant speed degradations.

TABLE I
PERFORMANCE COMPARISON

		CV-ROM	CRCS-ROM	SCSC-ROM w/o HBL	SCSC-ROM
Power [mW] at 100MHz	Control Unit	0.88	1.66	0.66	0.78
	Bit Line and SA	6.67	2.7	1.55	1.03
	Word Line Decoder	0.5	0.35	0.51	0.76
	Predecoder	0.6	0.6	0.53	0.53
	Column Decoder	0.14	0.14	0.14	0.14
	Total Power	8.79	5.45	3.39	3.24
Maximum Speed [ns]		3.5	8.1	4.0	4.0
ROM Area [mm2]		0.24 (0.38mm×0.64mm)	0.27 (0.41mm×0.67mm)	0.25 (1.04) (0.39mm×0.65mm)	0.27 (0.39mm×0.68mm)
ROM Organization		128Kbits (4K × 32bits)	128Kbits (4K × 32bits)	128Kbits (4K × 32bits)	128Kbits (4K × 32bits)
Bit Line Swing Voltage [V]		1.7	0.6	0.3	0.3
Number of Capacitor		0	96	1	1
Leakage Current		$512 \times I_{OFF}$	$512 \times I_{OFF}$	$512 \times I_{OFF}$	$47 \times I_{OFF}$

* I_{OFF} is off-current of NMOS cell transistor

Although the sense amplifier detects much smaller voltage differences, we assume that the minimum sensing voltage required for the sense amplifier is 300 mV because a large voltage difference is desirable to increase noise margins. The BL swing voltages of the CV-ROM, CRCS-ROM, and SCSC-ROM are 1.7 V, 600 mV, and 300 mV, respectively. In the CV-ROM, the BL swing voltage is $V_{\rm DD} - V_{\rm T}$ because NMOS transistors are used to precharge the bit lines. In the CRCS-ROM, the BL swing voltage is 600 mV, which is twice the minimum sensing voltage of the sense amplifier. Its sense amplifier senses the voltage difference between the BL and the reference voltage having a half of the BL swing voltage. Therefore, the sense amplifier actually senses the voltage difference less than 300 mV. However, in the SCSC-ROM, the BL swing voltage is 300 mV because its sense amplifier directly senses the BL swing voltage.

Table I shows the performance comparisons of ROMs with 4 K $\times$ 32 bits. Powers are measured at 100 MHz with $V_{\rm DD} = 2.5$ V. When the half data in the BL are "0" and the other half data are "1," the powers are measured. When all data are "0," the speeds are measured. The SCSC-ROM saves the power in the BLs by using the single charge-sharing capacitor and the HBL. It reduces the swing voltage and the capacitance of BLs to 50% and 39% of the CRCS-ROM, respectively. It also reduces the power consumption in the control unit and predecoder by simplifying the control signals for the charge-sharing operation and by using the hierarchical word line decoder. As a result, the SCSC-ROM consumes 37% and 59% powers compared to the CV-ROM and CRCS-ROM, respectively. As shown in Fig. 15, it saves 41% power compared to the CRCS-ROM by reducing 62% and 60% power in the BLs and the control unit, respectively. It also reduces the leakage current in the BLs to 9% of the CV-ROM and CRCS-ROM by using the HBL.

The SCSC-ROM without the HBL is also compared to show the effect of the HBL. Although the HBL increases 5% area of the SCSC-ROM, it saves 4% power and 91% leakage current. The amount of the saving power due to the HBL is not much because the SCSC-ROM uses the low-swing technique and the HBL increases the power in the word line decoder and control unit for the additional global word lines. However, the SCSC-ROM with the HBL are more powerful. The leakage current reduction is more critical in the SCSC-ROM because the leakage current affects the low-swing BL more seriously than the full-swing BL.

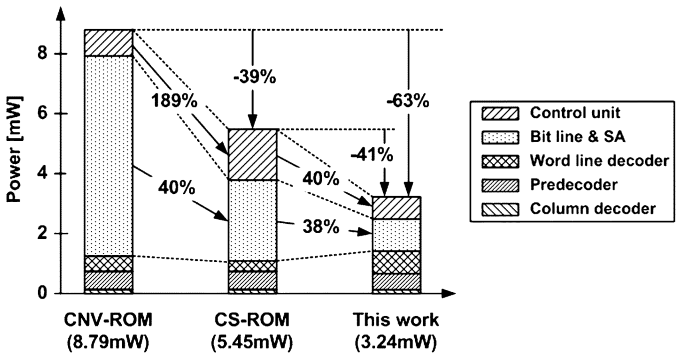

Fig. 15. Power consumptions in ROMs at 100 MHz.

The SCSC-ROM is 14% slower and 9% larger than the CV-ROM, respectively. The sense amplifiers, the charge-sharing capacitor, and the HBL of the SCSC-ROM increases delay and area compared to the CV-ROM, respectively. However, the SCSC-ROM is two times faster than the CRCS-ROM because it does not use the CRPD and CRWLD of the CRCS-ROM.

The CRCS-ROM uses many small capacitors for the charge-sharing operation. It is hard to implement the capacitors exactly because the capacitors are so small that their sizes vary due to interconnections and layout mismatches. However, the SCSC-ROM uses only the single capacitor implemented with the dummy bit lines. The size of the capacitor is large enough to overcome the effects of interconnections and layout mismatches. Therefore, the SCSC-ROM is robust against noises and easy to design compared to the CRCS-ROM.

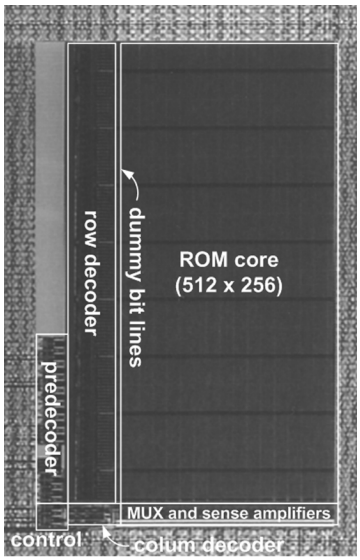

Fig. 16. Chip micrograph.

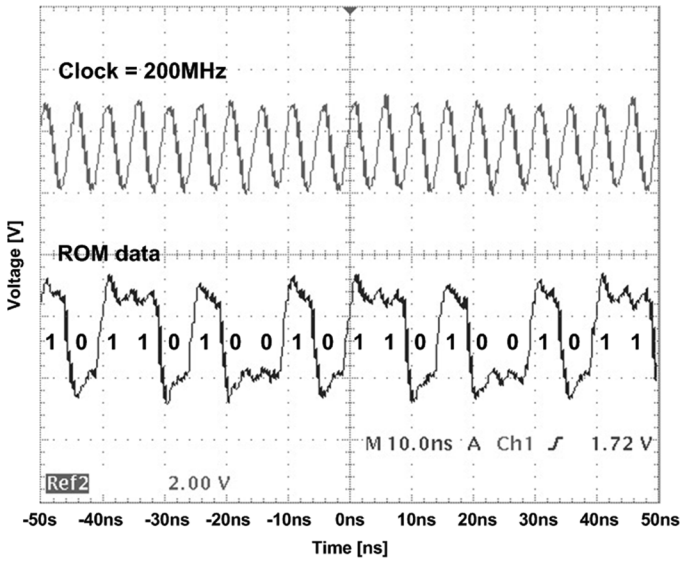

Fig. 17. Measured waveforms of the test chip at 200 MHz with 2.5 V.

TABLE II
FEATURES OF THE TEST CHIP

Technology	0.25μm CMOS
Supply Voltage	2.5V
Maximum Clock Frequency	240 MHz
Organization	4K×32 bits (512 word lines × 256 bit lines)
Chip Core Area	0.27 mm^2 (393μm × 680μm)
Power	8.2mW at 240MHz

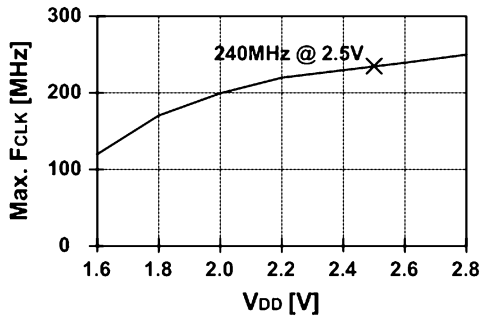

Fig. 18. Maximum operating frequency of the test chip versus $V_{\rm DD}$.

B. Test Results

A SCSC-ROM chip with 4 K × 32 bits is fabricated in a 0.25-μm CMOS process with 2.5-V supply voltage. Fig. 16 shows the chip micrograph. The features of the test chip are tabulated at Table II. The SCSC-ROM chip core consumes 8.2 mW at 240-MHz clock frequency and 2.5-V supply voltage. The core area of the test chip is 0.27 mm^2. Fig. 17 shows the measured waveforms at 200 MHz. Fig. 18 shows the maximum operating frequency according to the supply voltage. Its maximum operating frequency is 240 MHz when $V_{\rm DD} = 2.5$ V.

IV. CONCLUSION

This paper proposes the SCSC-ROM to reduce the power consumption in BLs, control unit, and predecoder. The SCSC-ROM saves the power in BLs by reducing the swing voltage of BLs by using the single charge-sharing capacitor. The swing voltage can be reduced to the sensing voltage of sense amplifiers. The single charge-sharing capacitor is implemented by the dummy bit lines so that the SCSC-ROM becomes not only robust against noises but also easy to design. The SCSC-ROM further saves the power in BLs by reducing the capacitance and the leakage current of BLs by using the HBL. It also saves the power in the control unit and predecoder by using the hierarchical word line decoder. The simulation result shows that the SCSC-ROM with 4 K × 32 bits consumes only 37% power of the conventional low-power ROM. The SCSC-ROM chip is fabricated in a 0.25-μm CMOS process. It consumes 8.2 mW at 240 MHz with 2.5 V.

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