RESONANT TUNNELING DIODE BASED QMOS EDGE TRIGGERED FLIP-FLOP DESIGN

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ABSTRACT

Resonant Tunneling Diode (RTD) is well known as an ultra-fast device due to small intrinsic capacitance, large drive current as well as the high switching speed. Pair of RTDs has self-latching property, which makes RTD a very promising candidate for nano-pipelining circuit design. The most pervasive used RTD-based sequential logic is MOBLIE. However, MOBILE is a return-to-zero mode circuit, which makes it difficult to be used in some specific applications. In this paper, we proposed three Quantum MOS (QMOS) flip-flop designs. Our designs explore the advantage of MOBILE while keeping the output to a holding stage instead of return-to-zero. The circuit topologies and circuit operations are described and discussed. The performance of these circuits is evaluated by using HSPICE. Then the final results are compared with each other.

1. INTRODUCTION

Latches and flip-flops are basic storage elements for sequential circuits. There are two major storage element implementation concepts: static and dynamic. A static implementation uses some positive feedback mechanism to compensate the charge loss at the capacitive storage node caused by the leakage current. The static storage node always has a conductive path connected to power or ground. For a dynamic implementation, the storage node only connects to power supply when the storage element is active. In other word, when the storage element is nonactive, the dynamic storage node is floating and the stored value is valid only in a limited amount of time[1].

RTD pair is a natural candidate for static latches and registers design due to its self-latching characteristic as shown in Figure 1. The output voltage level is determined by the peak current difference between the two RTDs. The output latches at logic high if the load RTD has larger peak current, and vice versa. RTD can also be used in dynamic logic design. The most common used configuration is MOBILE [2] which is composed of a RTD pair augmented by an input NMOS transistor connected parallel with driver RTD. The operation mode of MOBILE is determined by clock signal. When clock is low, MOBILE is in precharge phase, and the output node is discharged to logic low. When clock goes high, the output voltage level of MOBILE is then determined by the effective peak current difference between the driver RTD the load RTD. Input NMOS transistor is used to modify the effective peak current

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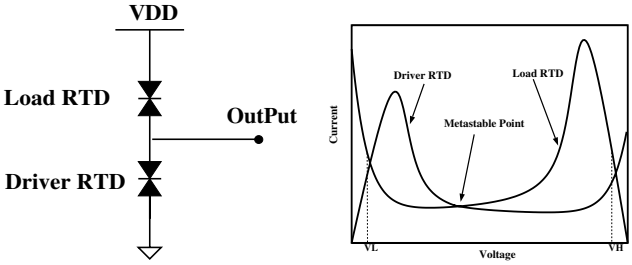


(a) RTD Pair Configuration. (b) Self-latching Property.

Fig. 1. Self-latching Property of RTD pair.

of the driver RTD. The operation principle of MOBILE circuit can be found elsewhere[3] in detail. Since MOBILE is a return-to-zero mode circuit, multi-phase clock usually designed to achieve a pipelined structure [4]. To reduce the complexity of the clock scheme design, it's necessary to design simple clock scheme RTD based latches and flip-flops while preserving the ultra-high switching speed advantage of the MOBILE circuit.

In this paper, we first propose a MOBILE based edge triggered D-type Flip-Flop (MDFF) with a CMOS clocked buffer as the output holding stage. Then a modified MOBILE-TSPC edge triggered Flip-Flop is proposed to overcome the disadvantages introduced by the original MOBILE circuit. Finally, a MOBILE-SRFF configuration is proposed to obtain a better circuit performance. This paper is organized as follows: in Section II, the configurations and operation principles of the proposed circuits are introduced and explained; in Section III, the circuit functionality is verified and the circuit performance is evaluated by using HSPICE. The circuit performance is then analyzed and compared with each other. Finally, we draw the conclusion.

2. DESIGN AND OPERATION PRINCIPLE OF RTD BASED FLIP-FLOPS

2.1. MOBILE D-type Flip-Flop (MDFF)

The configuration of MOBILE D-type Flip-Flop(MDFF)is shown in Figure 2(a). This MDFF is composed of a sampling stage and a holding stage. The sampling stage is a MOBILE circuit which is precharged to logic high instead of return-to-zero. The holding stage is a CMOS clocked buffer. MDFF is an edge triggered Flip-Flop. Input signal is sampled at the rising edge of the clock and is

Table 1. The operation principle of MDFF.

CLK	D	QB	Q
Low		High	Q_{pre}
Low to High	High	High to Low	Q_{pre} to High
	Low	High	Q_{pre} to Low

Table 2. The operation principle of MOBILE-SRFF.

CLK	D	DB	SET	RESET	Q
Low			Low	Low	Q_{pre}
Low to High	High	low	High	Low	High
	Low	High	Low	High	Low

held by the output buffer until the next clock rising edge arrives. The operation principle of MDFF is summarized in Table 1, where Q_{pre} denotes the output of the previous state. The advantages of this circuit are as follows: First, the sampling stage is ultra-fast due to MOBILE configuration; Second, in order to reduce the circuit delay that is dominated by the holding stage, we use precharged high MOBILE such that an enable NMOS transistor can be used in the holding stage instead of a PMOS transistor. However, MDFF needs double phase clock to achieve a successful operation, which increases the complexity of the layout and clock scheme design. To overcome this drawback, we proposed another MOBILE-TSPC circuit which only needs single phase clock to achieve the correct functionality.

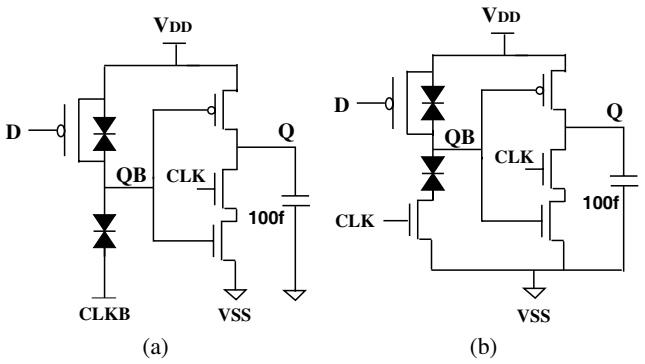


Fig. 2. (a) MOBILE D-type Edge Triggered Flip-Flop Schematic. (b) MOBILE-TSPC Edge Triggered Flip-Flop Schematic.

2.2. MOBILE True Single Phase Clock Flip-Flop(MOBILE-TSPC)

Circuit schematic of MOBILE-TSPC is shown in Figure 2(b). The sampling stage is modified by adding an enable NMOS transistor, which makes this MOBILE-TSPC flip-flop a true single phase clock circuit. Adding a foot NMOS transistor also reduces the capacitive load of the clock signal, and therefore, reducing the the power consumption of this circuit. The operation principle of MOBILE-TSPC is identical to that of MDFF as shown in Table 1. The major disadvantage of this circuit is that the foot NMOS transistor limits the switching speed of the MOBILE circuit. Another disadvantage is that both MDFF and MOBILE-TSPC are sensitive to noise. This is because both MDFF and MOBILE-TSPC are dynamic edge triggered flip-flops. The output node is floating when they are in holding mode. Due to the leakage current of the storage node, the clock frequency is also limited in order to keep the valid output value in evaluation phase. In typical CMOS design, a small keeper may be used at the output to improve the noise immunity. However, keeper usually increases the clock to output delay. To overcome these drawbacks, we proposed a new MOBILE-SR Flip-Flop (MOBILE-SRFF) as shown in Figure 3.

2.3. MOBILE Set-Reset Latch FF (MOBILE-SRFF)

The sampling stage of MOBILE-SRFF is built by two return-to-zero mode MOBILEs. The holding stage is a RTD based Set-Reset latch. For RTD Set-Reset latch, the effective peak current of load RTD and that of driver RTD are both modified by a parallel connected NMOS transistor. The output voltage is then determined by the effective peak current difference between the pull up network and pull down network. MOBILE-SRFF is expected to have best performance among the proposed circuit topologies due to several reasons: First, MOBILE-SRFF has ultra-high sampling speed due to MOBILE configuration in the sampling stage; Second, propagation delay is reduced by using RTD based Set-Reset latch as the holding stage, which is faster than CMOS based clocked buffer; Third, the Set-Reset latch is static, and therefore, MOBILE-SRFF has very good noise immunity. The possible disadvantages of this circuit are: (1)clock signal has large capacitive load; (2) the RTD Set-Reset latch has DC power consumption when the circuit is in the holding mode. However, since the stable point of the Set-Reset latch is determined by the valley current of the RTD pair. If RTD has a very low valley current, the DC power consumption can be very small. The operation principle of this MOBILE-SRFF is summarized in Table 2. As we have mentioned, we can add foot NMOS transistor to sampling stage in order to reduce the power consumption by sacrificing the speed of this circuit.

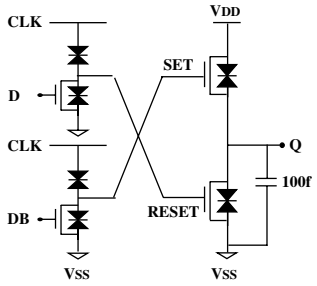


Fig. 3. Schematic Diagram of MOBILE Set-Reset Latch Edge Triggered Flip-Flop.

3. EVALUATION AND DISCUSSION

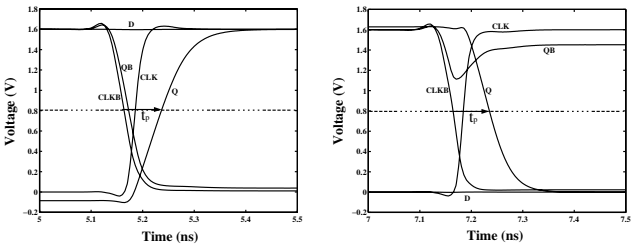
Power consumption, speed performance as well as the timing constrains of proposed flip-flops are evaluated by using HSPICE with Level-49 MOS model at 0.18μ technology. In our simulation, we have used physical RTD model developed in [5]. The waveforms of proposed circuits are shown in Figure 4, Figure 5 and Figure 6.

Table 3. Speed Comparison Of The RTD Based Edge Triggered Flip-Flops.

Circuits	Delay (ps)									Setup	Hold	Min Pulse Width
MT^*	CLK to QB			CLK to Q						$-91.8p$	$231.4p$	$139.6p$
	t_{PLH}	t_{PHL}	t_P	t_{PLH}		t_{PHL}		t_P				
	0	20.6	10.3	74.9		83.8		79.4				
MD^*	CLKB to Q			CLKB to QB			CLK to Q			$-5.28p$	$176.2p$	$170.9p$
	t_{PLH}	t_{PHL}	t_P	t_{PLH}	t_{PHL}	t_P	t_{PLH}	t_{PHL}	t_P			
	72.3	70.6	71.5	8.3	8.9	8.6	50.6	50.6	50.6			
MS^*	CLK to SET			CLK to RESET			CLK to Q			$28.09p$	$127.6p$	$155.7p$
	t_{PLH}	t_{PHL}	t_P	t_{PLH}	t_{PHL}	t_P	t_{PLH}	t_{PHL}	t_P			
	3.4	2.8	3.1	5.3	3.3	3.8	46.2	45.0	45.6			

MT^*: MOBILE-TSPC; MD^*: MDFF; MS^*: MOBILE-SRFF.

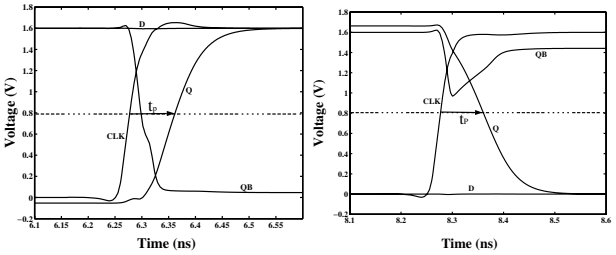
The speed performance of these circuits are optimized for minimum Power Delay Production (PDP). RISE and FALL delay are measured at stable region[6],where input signal to clock delay does not affect the clock to output delay. Figure 4 shows the RISE and



(a) Rise Delay Waveform. (b) Fall Delay Waveform

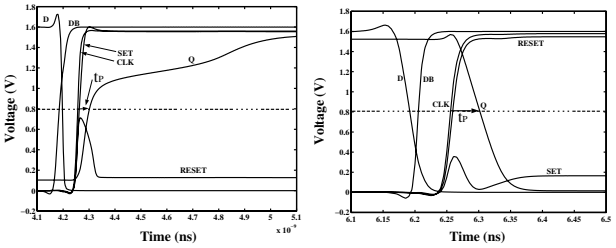
Fig. 4. Simulation Waveform of MDFF.

Fall delay waveforms of MDFF. CLK signal has an inverter delay with CLKB signal. We notice that CLKB to Q delay is dominated by the holding stage. One reason is that CMOS clocked buffer has slower switching speed than MOBILE circuit. Another reason is that CLK signal is later than CLKB signal to ensure the correct operation, and therefore, the QB cannot be latched in the holding stage until CLK signal is active. Reducing the delay between CLKB and CLK will reduce the circuit delay. In Figure 4(b), we notice that the Fall delay waveform of MDFF has a relatively large glitch at the falling edge of the CLKB signal, which increases CLKB to Q delay. This glitch happens due to the larger response time of input PMOS transistor than that of the RTD pair. At precharge phase, load RTD and driver RTD both work in the first Positive Differential Resistance (PDR I) region. When clock goes high, supply voltage across the driver RTD increases rapidly, which causes driver RTD to switch into the Negative Differential Resistance (NDR) region while load RTD switches into Wide Valley Region (WVR) before PMOS device has proper response. At this moment, the transient current of driver RTD is much larger than that of load RTD because of the following reasons: First, load RTD is sized smaller than driver RTD in sampling stage to realize the correct functionality; Second, the current in NDR region is larger than that in WVR region. Therefore, this large current difference causes a fast discharging of the QB node. When driver RTD also switches into the WVR region, the current difference between driver RTD and load RTD is greatly reduced, causing a slow transition to the metastable point, which allows PMOS to obtain enough time to restore the storage node back to high. The load RTD then switches back to PDR I region while driver RTD goes to second Positive Differential Resistance (PDR II) region.



(a) Rise Delay Waveform. (b) Fall Delay Waveform.

Fig. 5. Simulation Waveform of MOBILE-TSPC.



(a) Rise Delay Waveform. (b) Fall Delay Waveform.

Fig. 6. Simulation Waveform of MOBILE-SRFF.

Transient waveform for MOBILE-TSPC is shown in Figure 5. In Figure 5(a), the falling transition waveform of QB has a kink at lower voltage level. For typical MOBILE switching from logic high to logic low, the driver RTD has larger current than load RTD when the metastable point has been passed. Therefore, the switching speed should be improved at lower voltage level for a typical MOBILE circuit. However, in MOBILE-TSPC, I_{DS} becomes smaller with the decreasing of V_{DS} of foot NMOS transistor, which limits the switching speed of the MOBILE, resulting a kink phenomenon.

Figure 6 shows the transient simulation results for MOBILE-SRFF. The RISE delay waveform shows that the output initially

switches very fast. Then it goes into a very slow transition region. Finally, the output switches fast again until it reaches logic high. This phenomenon is caused by the transition behavior of the Set-Reset latch. The initial fast switching behavior is caused by the fast switching ability of the RTD pair. When both driver RTD and load RTD reach the WVR region where the RTD current is very small, the switching speed is then dominated by the SET and RESET NMOS transistors. For pull up transition, due to body effect,the SET NMOS transistor cannot provide enough current to maintain the switching speed, and thus it slows down the transition process. Once the output voltage passes the metastable point, the current difference of load RTD and driver RTD again dominates the transient current, causing a second fast switching behavior. In our simulation, the size of load RTD is chosen much smaller than that of driver RTD to minimize the power consumption while preserving the reasonable fast transition. This explains that the second faster switching shown in Figure 6(a) is not remarkable since the load RTD doesn't have large drive current. Since the RESET NMOS has no body effect, the pull down transition waveform shown in Figure 6(b) doesn't have the similar behavior as the pull up transition.

In Table 3, we compared the speed performance of the three flip-flops. We also measured the setup time, hold time and the minimum input pulse width for each circuit. For MDFF, the setup time is measured from input (D) to CLKB since CLKB is earlier than CLK. For MOBILE-SRFF, D and DB are generated by using local buffer. Since signal DB has an inverter delay with signal D, the setup time and hold time are measured from signal D to signal CLK in order to ensure the correct operation. From our experiment, we notice that the setup time for MOBILE can be slightly negative. However, for MOBILE-SRFF, setup time is positive instead of negative, which is caused by the signal delay between D and DB. Table 3 also shows that, for MDFF, the CLKB to Q delay is much longer than CLK to Q delay due to the reasons we mentioned in the previous section. The results show that MOBILE-SRFF is about 42.6% faster than the slowest MOBILE-TSPC.

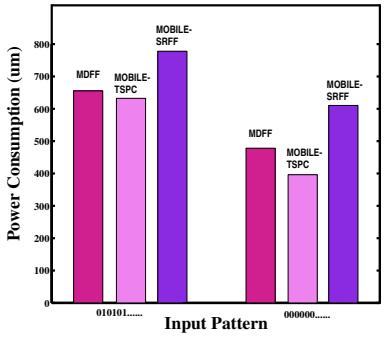


Fig. 7. Power consumption comparison.

We measured the power consumption for each circuit with different switch activity of the input data pattern. Power consumption measurement includes three parts: the power consumed by the clock generator, the power consumed by the input signal generator and the power consumed by the core flip-flop components[6]. The results are shown in Figure 7 and Table 3. We observed that the switching factor does not affect the power consumption too much. This is because large portion of power is consumed by clock generator which always switches no matter what input data pattern is applied. The results also show that, as we expected, MOBILE-SRFF consumes most power among these three circuits. However, due to the fast switching speed, MOBILE-SRFF has a minimum Power Delay Product(PDP). We already mentioned that MOBILE-SRFF has very good noise immunity. Therefore, MOBILE-SRFF has the best performance in terms of reliability and PDP among the proposed edge triggered flip-flops.

Table 4. Comparison of The Three Flip-Flops

Circuit		MD^*	MT^*	MS^*
# of RTDs		2	2	6
# of FETs		4	5	4
Delay (ps)		71.5	79.4	45.6
Power (μw)	$\alpha = 0.5$	538.56	510.98	709.71
	$\alpha = 0.35$	499.75	392.07	678.00
	$\alpha = 0.2$	495.44	390.08	677.72
PDP (fJ)	$\alpha = 0.5$	38.51	40.57	32.36
	$\alpha = 0.35$	35.73	31.13	30.91
	$\alpha = 0.2$	35.42	30.97	30.90

MT^*: MOBILE-TSPC; MD^*: MDFF; MS^*: MOBILE-SRFF.

4. CONCLUSION

Three RTD based QMOS edge triggered Flip-Flops are designed and simulated by using HSPICE. MDFF and MOBILE-TSPC are dynamic flip-flops. They have CMOS clocked buffer as the holding stage, which increases the propagation delay but avoid the DC power consumption. MOBILE-SRFF uses the RTD based Set-Reset latch as the holding stage, which makes it a static flip-flop.Therefore, MOBILE-SRFF has better noise immunity. Simulation results show that MPBILE-SRFF has best PDP performance among these three filp-flops.

5. REFERENCES

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