Gate-to-Source/Drain Nonoverlap Device for Soft-Program Immune Unified RAM (URAM)

Jin-Woo Han, Chung-Jin Kim, Sung-Jin Choi, Dong-Hyun Kim, Dong-Il Moon, and Yang-Kyu Choi

***Abstract*—A soft-program immune structure for a unified RAM (URAM) is presented. A unique feature of URAM is the multifunctionality of a flash and capacitorless 1T-DRAM in a single transistor. However, charge trapping into O/N/O during a cyclic 1T-DRAM operation can cause an undesirable threshold voltage shift, resulting in an unstable URAM operation called a soft program. In a gate-to-source/drain nonoverlap structure with a nonextended O/N/O layer under the gate spacer, the impact ionization region is steered out from the gate, which is located under the spacer. In the 1T-DRAM mode of URAM, the programming biases are selected so that impact ionization can occur under the gate spacer, thereby alleviating the soft program. The nonoverlap device relieves the operational voltage constraint imposed by the soft program. In addition, nonvolatile flash memory and capacitorless 1T-DRAM perform an acceptable performance without interference.**

***Index Terms*—Disturbance, nonoverlap, nonvolatile memory (NVM), soft-program, unified RAM (URAM), 1T-DRAM.**

I. Introduction

UNIFIED RAM (URAM) is a promising fusion memory for combining high-speed DRAM and nonvolatile memory (NVM) into a single memory transistor [1], [2]. Unlike the conventional 1T/1C DRAM, the DRAM mode of URAM uses a floating-body hysteresis effect, which enables the capacitorless 1T-DRAM [3]. Because an O/N/O gate dielectric is used in a partially depleted floating-body structure, the operation of the NVM and capacitorless 1T-DRAM can be realized in a single memory transistor. In the 1T-DRAM mode, unfortunately, impact ionization for programming can adversely affect the trapped charges in the O/N/O layer, giving rise to a soft-program issue [1], [2]. While a harsh impact ionization condition can provide a faster writing speed and wider sensing window for 1T-DRAM, increased hot-electron injection causes an undesired shift in the threshold voltage (V_T) after cyclic 1T-DRAM operations. Thus, the program voltage of 1T-DRAM is constrained so as to avoid interference with the NVM. This is an increasingly important concern. Accordingly, the development of the soft-program immune device structure is very timely and inevitable.

Manuscript received January 27, 2009. First published April 7, 2009; current version published April 28, 2009. This work was supported in part by the National Research Program for the 0.1-Terabit Nonvolatile Memory Development, sponsored by the Ministry of Knowledge Economy. The review of this letter was arranged by Editor S. Kawamura.

The authors are with the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: ykchoi@ee.kaist.ac.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2016441

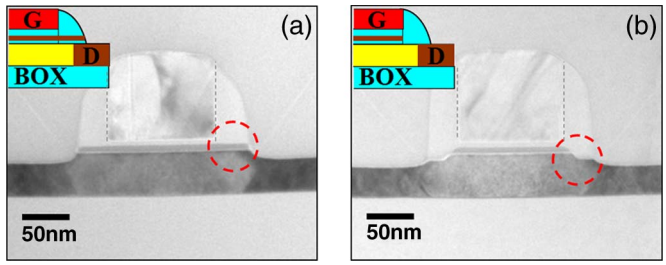

Fig. 1. TEM images of gate-to-S/D nonoverlap devices. (a) O/N/O layer is extended to the spacer region (extended O/N/O). (b) O/N/O layer is not extended to the spacer region (nonextended O/N/O).

A gate-to-source/drain (S/D) nonoverlap structure has an impact ionization region outside of the gate [4]. Even though impact ionization triggers a hot-electron injection, the hot electrons in the gate–S/D nonoverlap structure have a negligible effect on the trap sites in the O/N/O layer during 1T-DRAM operation. Thus, the constraint of selecting proper biases to isolate the NVM and 1T-DRAM can be alleviated. In this letter, the nonoverlap device is presented as a soft-program immune URAM structure. Two different nonoverlap device structures are fabricated, namely, the extended O/N/O layer and the nonextended O/N/O layer under the spacer. The electrostatic properties of the two structures are compared. Furthermore, memory characteristics are analyzed, and simulation data support the virtues of the nonoverlap structure.

II. Device Fabrication

A p-type (100) SOI substrate with a top-silicon thickness of 100 nm and a buried-oxide thickness of 140 nm is used as a starting material. The top silicon is thinned down to the desired thickness of 50 nm by sacrificial oxidation and removal. After the active area is patterned, an O/N/O gate dielectric with a thickness of 3/8/6 nm is formed, and n^+ poly-Si is sequentially deposited. At the gate and spacer formation step, two different structures are prepared. While the gate poly-Si and O/N/O layer are etched in a "nonextended O/N/O" device, only the gate poly-Si is patterned, and the O/N/O layer remains in an "extended O/N/O" device. The n^+ S/D junctions are formed in a conventional manner. According to the process simulation, the lateral straggle of phosphorus (P) impurities for the metallurgical junctions of the S/D is less than 20 nm, which is shorter than the spacer length of 35 nm. Thus, the nonoverlap of the gate to the S/D is attained. The transmission electron microscopy (TEM) images of the fabricated devices are shown in Fig. 1. The physical gate length and width are 110 and 350 nm, respectively. The marked regions show the existence of the

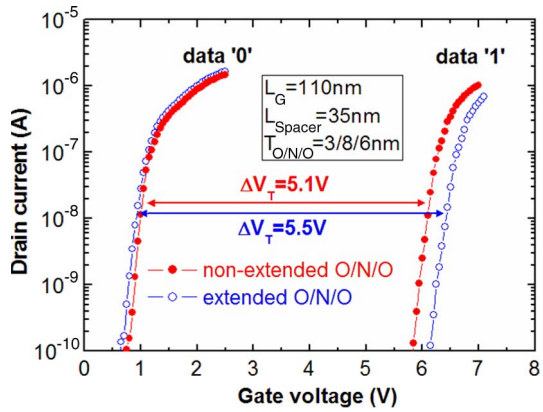

Fig. 2. NVM characteristics. P/E are carried out by CHEI ($V_{G,\mathrm{PGM}} = 10$ V and $V_{D,\mathrm{PGM}} = 2.5$ V, with $\tau_{\mathrm{PGM}} = 200$ μs) and HHI ($V_{G,\mathrm{ERS}} = -10$ V and $V_{D,\mathrm{ERS}} = 2.5$ V, with $\tau_{\mathrm{ERS}} = 10$ ms), respectively. Even though the nonoverlap would degrade the P/E efficiency, an acceptable V_{T} window of more than 5 V is achieved.

O/N/O layer under the spacer region. All measurements were carried out at 25 °C, and the source and the substrate (back gate) were grounded.

III. Results and Discussion

Fig. 2 shows the measured $I_D - V_G$ characteristics of program and erase (P/E) states. P/E are carried out by means of channel hot-electron injection (CHEI: $V_{G,\mathrm{PGM}} = 10$ V, $V_{D,\mathrm{PGM}} = 2.5$ V, and $\tau_{\mathrm{PGM}} = 200$ μs) and hot-hole injection (HHI: $\mathrm{V}_{G,\mathrm{ERS}} = -10$ V, $\mathrm{V}_{D,\mathrm{ERS}} = 2.5$ V, and $\tau_{\mathrm{ERS}} =$ 10 ms), respectively. The "extended O/N/O" exhibits V_T window of 5.5 V, which is larger than the "nonextended O/N/O." It reveals that the trapped charges at the "extended O/N/O" contribute to a larger V_T shift. Ten years of data retention and 10^7 cycles of endurance are ensured with a V_T window that is larger than 3 V (data are not shown). It should be noted that, even though the nonoverlap would degrade the P/E efficiency in the NVM mode due to the decreased injection efficiency, the measured performance is certainly acceptable for flash memory application.

Fig. 3(a) shows the schematics for overlap/nonoverlap and extended/nonextended structures for 1T-DRAM mode analysis. The simulation data for overlap and nonoverlap devices with "nonextended O/N/O" are shown in Fig. 3(b), and the measurement data for "extended O/N/O" and "nonextended O/N/O" devices with nonoverlap structure are shown in Fig. 3(c). Before the cell is allocated to the 1T-DRAM mode, V_T is adjusted to 0.2 V by preprogramming of the NVM [1], [2]. As shown in Fig. 3(b), even though the nonoverlap device suffers from degradation of impact ionization efficiency, the sensing current window of the nonoverlap device is still higher than that of the overlap device. This result can be attributed that the enlarged hole storage volume formed near the junction and the reduced junction leakage current countervail the reduced impact ionization efficiency [5]. Therefore, the nonoverlap structure is preferred in terms of 1T-DRAM performance. It is worthwhile to note that the gate–S/D nonoverlap structure inevitably degrades a device performance due to a parasitic

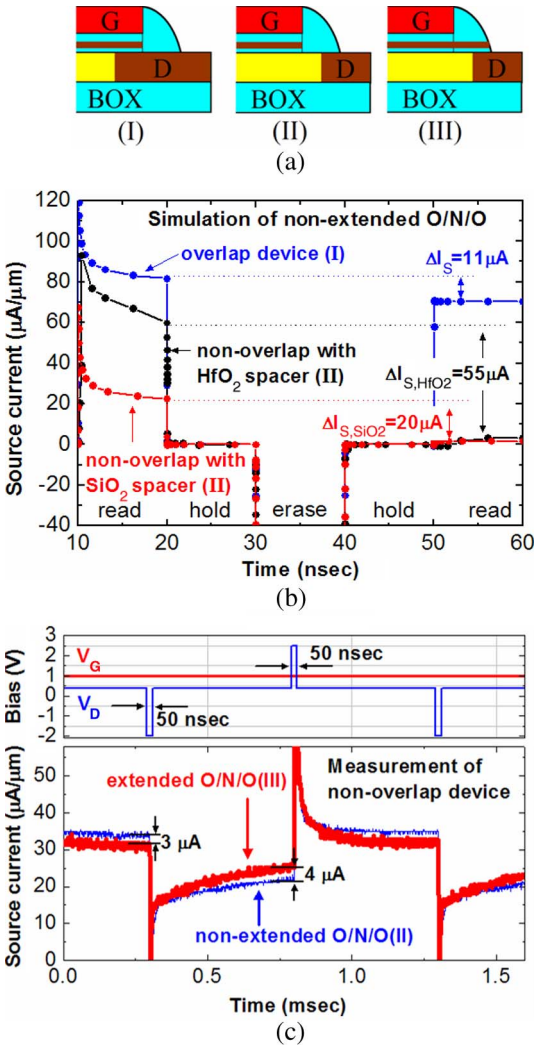

Fig. 3. (a) Comparative device schematics for 1T-DRAM analysis. (b) Simulation results of 1T-DRAM for the overlap versus nonoverlap structure with different spacers: SiO_2 versus HfO_2. (c) Measurement results of 1T-DRAM for the "extended O/N/O" versus "nonextended O/N/O" device.

voltage drop caused by extra series resistance. Nonetheless, a variety of high-k offset spacers can be introduced to improve current drivability and impact ionization efficiency [6]. The simulation results support that the high-k spacer can further increase the 1T-DRAM performance in the nonoverlap structure. An operational bias waveform for the measurement is shown in the upper part of Fig. 3(c). The "extended O/N/O" shows a wider sensing current window than the "nonextended O/N/O." The difference in the dielectric constant of the spacer region, i.e., with or without nitride, causes the disparity of the channel potential near the drain. The higher dielectric constant of the spacer is expected to boost impact ionization, and the resultant abundance of excess holes improves the 1T-DRAM performance in nonoverlap devices.

Fig. 4 shows the results of the soft program during 1T-DRAM operations. The dc stress of the 1T-DRAM programming voltage is applied, and the V_T shift is monitored. The simulation results of soft programming for overlap and nonoverlap devices are shown in Fig. 4 for the purpose of verifying the advantages of the nonoverlap device. They show that the

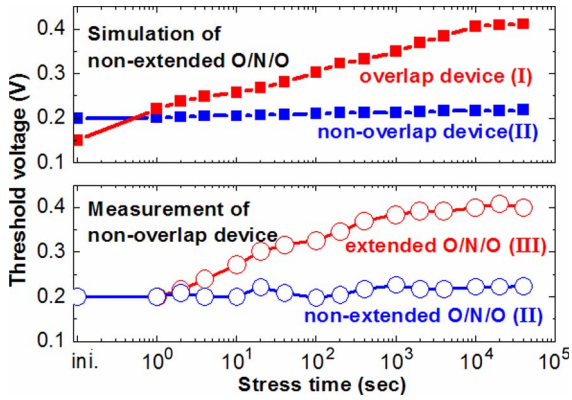

Fig. 4. V_T shift after dc stress. The stress condition is $V_G = 1$ V and $V_D = 2.5$ V, which is a program condition of 1T-DRAM. (Filled square) Simulation data support that the nonoverlap device is resistant to soft programming. The (blank circle) measured data of nonoverlap devices confirm that the "nonextended O/N/O" shows superior soft-programming immunity compared to the "extended O/N/O."

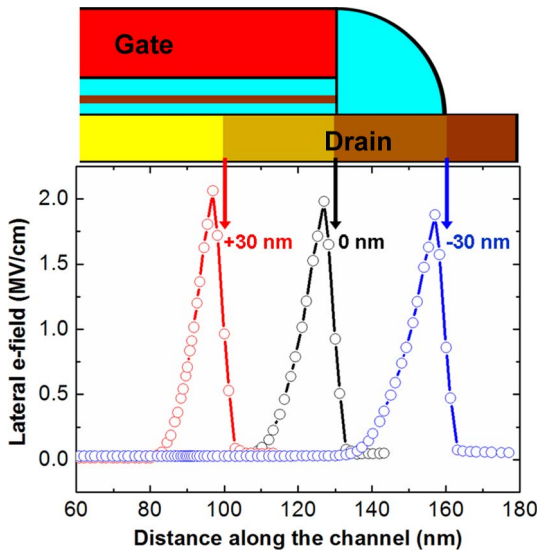

Fig. 5. Simulation results of electric field. The peak electric field moves from under the gate to under the spacer according to the "overlap," "zero overlap," and "nonoverlap." Thus, undesired soft-programming during a cyclic 1T-DRAM operation can be suppressed in the nonoverlap device.

gate–S/D nonoverlap device exhibits distinctively superior soft-programming immunity than the overlap device. In the case of the fabricated gate–S/D nonoverlap devices, the "nonextended O/N/O" shows better soft-programming immunity than the "extended O/N/O." Even though the "nonextended O/N/O" shows worse NVM and 1T-DRAM characteristics, the performance difference is ignorable. Therefore, the "nonextended O/N/O" with gate–S/D nonoverlap structure is attractive because it displays superior soft-programming immunity with an acceptable memory performance. The electric field is simulated for various gate-to-drain offsets from the overlap to the nonoverlap. The results are compared in Fig. 5. As the offset shifts from the overlap to the nonoverlap, the position of the peak electric field moves from under the gate to under the spacer. Consequently, the hot-carrier injection to the nitride traps is suppressed. Thus, the nonoverlap approach is a practical way of avoiding the soft-program issue.

IV. Conclusion

A gate–S/D nonoverlap structure is presented for a soft-program immune URAM structure. As the position of the impact ionization region moves from under the gate to under the spacer, the NVM state is unaffected by hot-carrier injection into O/N/O during a cyclic 1T-DRAM operation. Consequently, the gate–S/D nonoverlap structure embedded with the nonextended O/N/O mitigates the constraint of setting up a proper bias condition to avoid disturbance between NVM and 1T-DRAM operations.

References

[1] J.-W. Han, S.-W. Ryu, S. Kim, C.-J. Kim, J.-H. Ahn, S.-J. Choi, J. S. Kim, K. H. Kim, G. S. Lee, J. S. Oh, M. H. Song, Y. C. Park, J. W. Kim, and Y.-K. Choi, "A bulk FinFET unified-RAM (URAM) cell for multifunctioning NVM and capacitorless 1T-DRAM," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 632–634, Jun. 2008.

[2] J.-W. Han, S.-W. Ryu, C.-J. Kim, S. Kim, M. Im, S.-J. Choi, J. S. Kim, K. H. Kim, G. S. Lee, J. S. Oh, M. H. Song, Y. C. Park, J. W. Kim, and Y.-K. Choi, "Partially depleted SONOS FinFET for unified RAM (URAM)—Unified function for high-speed 1T DRAM and nonvolatile memory," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 781–783, Jul. 2008.

[3] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A capacitor-less 1T-DRAM cell," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 85–87, Feb. 2002.

[4] P. K. Ko, T. Y. Chan, A. T. Wu, and C. Hu, "The effects of weak gate-to-drain(source) overlap on MOSFET characteristics," in *IEDM Tech. Dig.*, 1986, pp. 292–295.

[5] K.-W. Song, H. Jeong, J.-W. Lee, S. I. Hong, N.-K. Tak, Y.-T. Kim, Y. L. Choi, H. S. Joo, S. H. Kim, H. J. Song, Y. C. Oh, W.-S. Kim, Y.-T. Lee, K. Oh, and C. Kim, "55 nm capacitor-less 1T DRAM cell transistor with non-overlap structure," in *IEDM Tech. Dig.*, 2008, p. 797.

[6] M.-W. Ma, C.-H. Wu, T.-Y. Yang, K.-H. Kao, W.-C. Wu, S.-J. Wang, T.-S. Chao, and T.-F. Lei, "Impact of high-k offset spacer in 65-nm node SOI devices," *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 238–241, Mar. 2007.