Low-jitter multi-phase digital DLL with closest edge selection scheme for DDR memory interface

K.-I. Oh, L.-S. Kim, K.-I. Park, Y.-H. Jun and K. Kim

A multi-phase digital delay-locked loop (DLL) capable of a low-jitter feature for DDR memory interface is reported. The DLL repeatedly selects the output clock edge which is closest to the reference clock edge to reduce the total jitter. A test chip was fabricated in a 0.18 μm CMOS process to verify its functionality. The measured RMS and peak-to-peak jitter of the DLL are 6.2 and 20.4 ps, respectively. The power consumption of the DLL is 12 mW from a 1.8 V supply voltage.

Introduction: Recently, memory I/O bandwidth has been increased for processing large amounts of data. A stable low-jitter clock generator is required to transfer data correctly at multi-gigabit rates for a high-performance memory interface. A multi-phase digital delay-locked loop (DLL) is used in the memory interface owing to its simplicity and short wake-up time from sleep-mode [1–6]. However, the output jitter of the digital DLL is limited to the time resolution of the delay cells. In this Letter, a multi-phase digital DLL using the closest edge selection scheme is proposed. The proposed DLL repeatedly selects the output clock edge which is closest to the edge of the reference clock to reduce jitter caused by resolution limitation.

Proposed low-jitter digital DLL: The block diagram of the proposed digital DLL is shown in Fig. 1. The delay line is coarsely controlled by a 4-bit digital code C_delay[3:0] and finely controlled by an analogue voltage VFINE. Each delay cell has binary weighted shunt capacitors, which are selectively connected to the output node according to the value of C_delay[3:0]. It also has a shunt capacitor which is controlled by the analogue value VFINE.

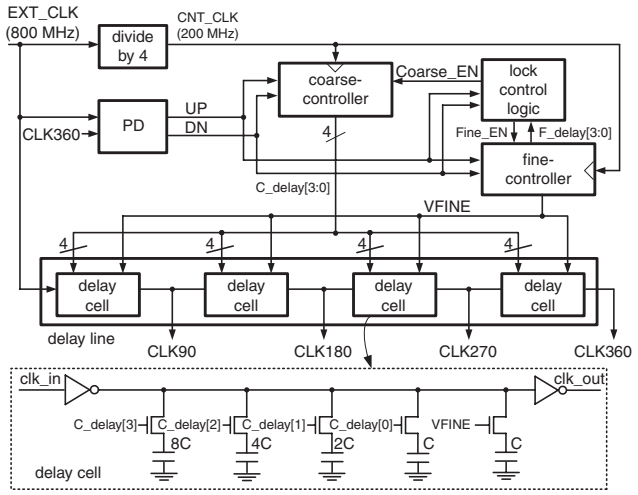

Fig. 1 *Block diagram of DLL*

Fig. 2 shows the block diagram of the control logic of the DLL. Coarse_EN signal is set to high to begin coarse-edge selection. C_delay[3:0], which controls the delay of the delay line, is determined by UP and DN from the PD. If the minimum and the maximum delay of the delay line are assumed as $0.5T$ and $1.5T$ for a proper operation of the DLL, where T is a period of the external clock EXT_CLK, a coarse delay step t_{C_STEP} of the delay line is expressed as $T/2^M$ where M is the bit-width of a coarse control code. In this design, M is selected as 4 based on the trade-off between a logic complexity and a coarse clock resolution ($t_{C\_STEP} = T/16$). Since the frequency of EXT_CLK is 800 MHz, t_{C_STEP} is 75 ps. When the coarse loop lock occurs, two adjacent edges around the rising edge of EXT_CLK are selected alternately because of the resolution limitation of coarse delay. Then, UP and DN appear alternately, which means coarse-edge selection is accomplished. Coarse_EN is set to low and Fine_EN is set to high. Fig. 3*a* shows the operating principle of closest edge selection.

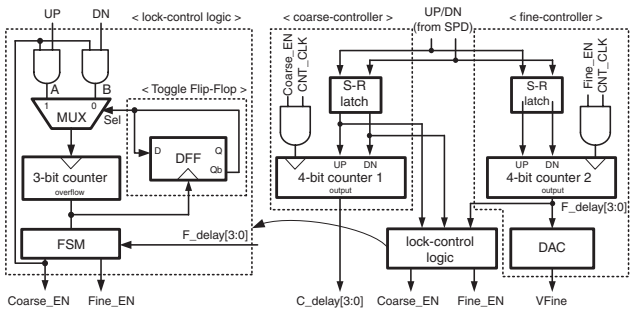

Fig. 2 *Block diagram of control logic*

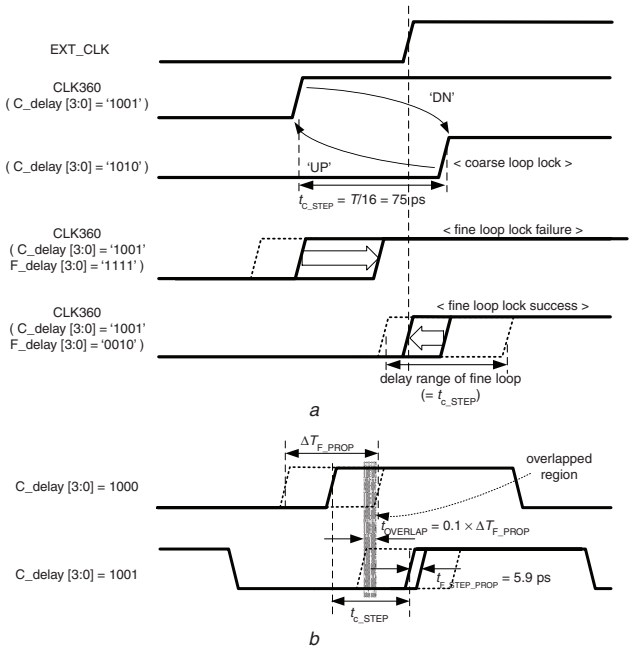

Fig. 3 *Closest edge-selection scheme*

a Operating principle
b Resolution jitter

The fine-edge selection begins when the Fine_EN signal is set to high. F_delay[3:0] is provided to a digital-to-analogue converter (DAC) and converted to VFINE, which adjusts the fine delay of the delay line. Since CLK360 is adjusted to lead or lag EXT_CLK within a phase difference of $T/16$, a phase adjustment of $T/16$ is required in the fine delay line. A fine delay step t_{F_STEP} of the delay line is expressed as $t_{C\_STEP}/2^N$ where N is the bit-width of a fine control code F_delay[N-1:0]. If N is selected as 4, t_{F_STEP} is 4.9 ps. When F_delay[3:0] becomes '1111' or '0000', which means fine loop lock has failed, Coarse_EN is toggled to high again. The coarse-controller selects the other edge by the lock-control logic. The delay range of the fine-edge selection of the conventional digital DLL ΔT_{F_CONV} is expressed as

$$\Delta T_{F\_CONV} = 2 \times t_{C\_STEP} = \frac{2T}{2^M} = \frac{T}{2^{(M-1)}} \quad (1)$$

where t_{C_STEP} is the coarse delay step of the delay line, T is a period of the EXT_CLK, and M is a bit-width of a coarse control code. ΔT_{F_CONV} covers two times of the coarse delay step because the conventional DLL cannot select an output clock edge which is closest from the EXT_CLK. If one edge is selected, the selected edge covers the delay range of adjacent edges. If no delay variation according to the process variation in the delay line is assumed for simplicity, the fine delay step of the conventional digital DLL $t_{F\_STEP\_CONV}$ is

$$t_{F\_STEP\_CONV} = \frac{\Delta T_{F\_CONV}}{2^N} \frac{T}{2^{(M+N-1)}} \quad (2)$$

where N is a bit-width of a fine control code. Unlike the conventional digital DLL, the proposed DLL selects an output clock edge repeatedly until the closest edge is selected. The coarse-controller selects one of the two different adjacent edges. If the selected edge does not reach the edge of the reference clock after the fine-edge selection, the coarse-controller

selects the other edge. Therefore, the delay range of the fine-controller is reduced compared to the conventional digital DLL. The delay range of the fine edge selection of the proposed digital DLL $\Delta T_{\text{F\_PROP}}$ is expressed as

$$\Delta T_{\text{F\_PROP}} = t_{\text{C\_STEP}} = \frac{T}{2^M} \tag{3}$$

Hence, the fine delay step of the proposed digital DLL $t_{\text{F\_STEP\_PROP}}$ is

$$T_{\text{F\_STEP\_PROP}} = \frac{\Delta T_{\text{F\_PROP}}}{2^N} = \frac{T}{2^{(M+N)}} \tag{4}$$

By comparing (2) and (4), the jitter of the output clock of the proposed digital DLL is also effectively reduced since the fine delay step size of the proposed digital DLL is reduced by almost one-half. To guarantee seamless edge changes and compensations for delay variation of the delay line, overlapped region t_{OVERLAP} exists among each delay range of fine edge selection. Assuming that t_{OVERLAP} is 10% of $\Delta T_{\text{F\_PROP}}$, (4) becomes

$$t_{\text{F\_STEP\_PROP}} = \frac{\Delta T_{\text{F\_PROP}} + 0.2\Delta T_{\text{F\_PROP}}}{2^N} = \frac{1.2T}{2^{(M+N)}} \tag{5}$$

If $T = 1.25$ ns, and $M = N = 4$, $t_{\text{F\_STEP\_CONV}}$ is 9.8 ps and $t_{\text{F\_STEP\_PROP}}$ is reduced to 5.9 ps. The resolution jitter of the closest edge selection scheme is shown in Fig. 3*b*.

Experimental results: A prototype chip has been fabricated in a 0.18 μm CMOS logic process with a 1.8 V supply voltage. Fig. 4 shows the measured jitter histogram of the output clock of the proposed multi-phase digital DLL. The RMS jitter and the peak-to-peak jitter of the DLL output clock are measured as 6.2 and 20.4 ps, respectively. A jitter of the output clock and power consumption comparisons of the proposed digital DLL to other works are shown in Fig. 5. The proposed digital DLL shows small peak-to-peak jitter and low power consumption among recent digital DLLs owing to the closest edge selection scheme. The active area is 70 × 230 μm for the DLL. The total power consumption of the DLL is 12 mW. The performance summary of the test chip is given in Table 1.

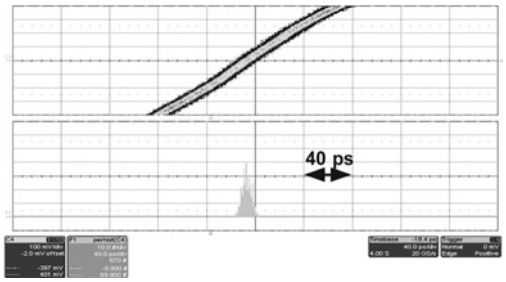

Fig. 4 *Measured jitter histogram of proposed DLL output clock*

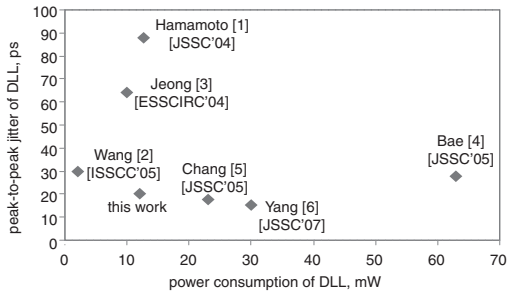

Fig. 5 *Performance comparison of proposed DLL*

Table 1: Performance summary of test chip

Technology	0.18 μm CMOS
Supply voltage	1.8 V
Operating frequency of DLL	510 MHz–1.1 GHz
Locked time of DLL	<80 cycles
Measured jitter of DLL	6.2 ps [RMS] at 800 MHz 20.4 ps [peak-to-peak] at 800 MHz
External clock frequency	800 MHz
Active area	70 × 230 μm
Power consumption	12 mW

Conclusions: The proposed DLL repeatedly selects the output clock edge which is closest to the reference clock edge to reduce the total jitter. The total power consumption of the DLL is 12 mW. The RMS jitter and the peak-to-peak jitter of the DLL clock are 6.2 and 20.4 ps, respectively.

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