A Fully Differential Rail-to-Rail Input Dynamic Latch

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Abstract

This paper proposes a fully differential rail-to-rail dynamic latch using both NMOS and PMOS input pairs for wide dynamic range, and the design issues with the proposed latch are discussed. For trans-conductance matching between the NMOS and PMOS inputs, body voltage control scheme is investigated.

1. Introduction

As supply voltage reduces with deep-submicron CMOS technologies, reduced signal swing range makes it difficult to achieve high dynamic range. In flash ADC design, such a condition makes comparator design difficult because the offset and noise requirements become stringent. In order to alleviate such constraints, this paper investigates a comparator structure with a rail-to-rail input stage [1]. So far-reported comparators with rail-to-rail input structure are based on the folded-cascode structure with static power consumption [2]. However, considering low power design trends these days [3], such static power consuming comparators are not preferable. Thus, we suggest a dynamic latch based rail-to-rail input comparator. The NMOS and PMOS input pairs in the proposed structure are stacked on the same current branch. In the following sections, the design principle and design considerations of the proposed latch will be discussed. Process variation insensitive circuit technique for the proposed structure is introduced, and the upper limitation of its application in flash ADC will be investigated by various simulations.

2. Circuit description

Fig. 1(a) is a conventional dynamic latch which has no static power consumption [4]. The reasonable input signal range for the latch is between the supply voltage and the threshold voltage (V_{TH}) of NMOS input transistor. Since V_{TH} does not reduces as much as the supply voltage does, the input dynamic range of this type of latch reduces in deep submicron technology. The proposed rail-to-rail input dynamic latch is based on this structure in order to take the advantage of its low power characteristic. The rail-to-rail input structure is build up by simply stacking a PMOS input pair (M4 and M5) on the same branch where NMOS inputs (M6 and M7) exist, as shown in Fig. 1(b). Then the output polarity is determined by the difference of the differential input and the reference as the equation

$$I_D = g_{mn}(V_{in+} - V_{ref+}) - g_{mp}(V_{in-} - V_{ref-}) \quad (1)$$

If $g_{mn} = g_{mp} = g_m$,

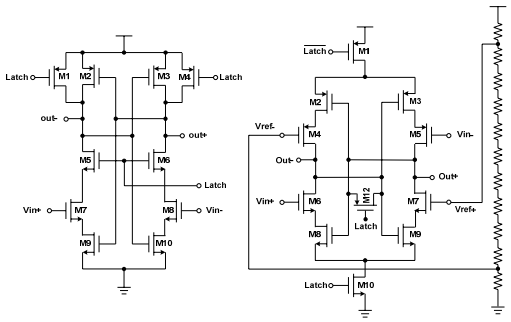
$$I_D = g_m(V_{in+} - V_{ref+}) - g_m(V_{in-} - V_{ref-}) \quad (2)$$

Note that the minimum supply voltage of the proposed structure is the sum of the threshold voltage of the NMOS and PMOS input transistors.

Unlike in Fig. 1(a), both outputs cannot be connected to V_{DD} during reset phase. The reason is following. If we do so, the PMOS input pair in the rail-to-rail structure cannot wake up as fast as the NMOS input pair does, then the output will depend only on the NMOS input difference. Thus, in the proposed circuit, two reset switches (M1 and M10) are located between the comparator core and V_{DD}/ground in order to make the comparator core to be floated during reset, while the additional reset switch (M12) connects two outputs. This results in the output voltages (out+ and out-) to be around half V_{DD} by charge sharing, By doing this, the latch operation becomes fast since it does not require turn on time (The comparator input transistors are in the saturation region as soon as the latch enabled (Latch = High).

For this condition, V_{cm} is equal to $V_{DD}/2$, reference connected to NMOS transistor higher than V_{cm}, and reference connected to PMOS transistor lower than Vcm. If (V_{in+}-V_{in-}) is larger than (V_{ref+}-V_{ref-}), then out- goes to ground by M6 and M8. On the other hand, if (V_{ref+}-V_{ref-}) is larger than (V_{in+}-V_{in-}), out- is pulled towards V_{DD} by M2 and M4.

Note that, so far, we have just discussed the case where $g_{mn} = g_{mp}$. But, in practice, we can hardly guarantee such conditions due to variations in process, supply voltage, temperature, and so on. As can be seen from equation (1), if $g_{mn} \neq g_{mp}$, then the output polarity will be differ from ideal. In addition, the common level of the input signal can vary and this will make g_m mismatch between the NMOS and PMOS input transistors. In the following sections, we discuss the effects of those non-idealities and some possible circuit techniques to reduce those problems.



(a) Limited input range [4] (b) Rail-to-rail input range

Figure 1. Latch-type comparators

3. Design considerations

The proposed comparator has been designed using CMOS 0.13um process with supply voltage (V_{DD}) of 1.2V, and its input common level is assumed to be 0.6V, $V_{DD}/2$. The transistor size ratio of NMOS and PMOS input pairs is 1:4.3 for the same g_m values.

A. Input common level

First, the effect of the input common level change is discussed. As the input common level varies from the ideal value, $V_{DD}/2$, trans-conductances of input transistors deviate from its nominal value. Fig. 2 shows the offset voltage variation in several comparators with different reference voltages.

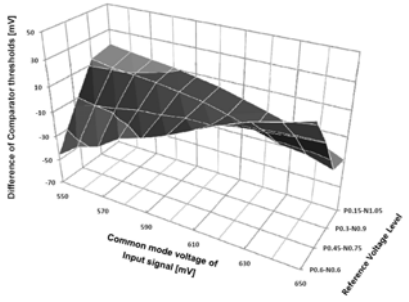


Figure 2. The effect of commom mode voltage

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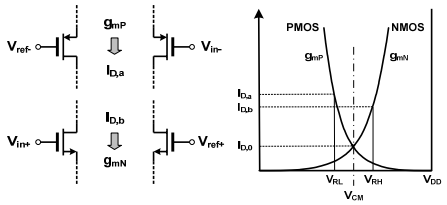
Here, the notation, P0.15-N1.05, means the comparator with its PMOS reference input connected to the reference voltage of 0.15V and its NMOS input to 1.05V. Others follow the same convention. This simulation shows that the offset voltage varies about ± 40mV as the common level varies about 100mV. This is quite severe sensitivity to the common level change unlike other fully differential circuits. The reason of this high sensitivity to the common level can be explained with Fig. 3. For the typical SPICE model, when we design, we try to match the current and g_m between NMOS and PMOS pairs. The beginning point of design would be when the both input signals are at the common level (We designed size ratio of 1:4.3 for NMOS:PMOS in this condition). But, once the common level changes this condition varies. Fig. 3 depicts this phenomenon. Two transistor pairs of Fig. 3(a) are the simplified input pairs of Fig. 1(b). More severe cases happen when the comparators have different reference points. In such comparators, the trial for same g_m with the assumption of same input is not valid. Thus, even though the differential input varies symmetrically based on the ideal common level (V_{RL} and V_{RH}), g_m's of NMOS and PMOS are different because of the transistor V-I curve are not symmetrical. Even though the proposed comparator structure has such disadvantages, however, the problem can be effectively relaxed by known compensation methods such as [5].



(a) (b)

Figure 3. Analysis of current mismatch effect of the input pairs

B. Random offset

Assuming that the deviation of the input common can be corrected, now we investigate the statistical offset voltage distribution in the proposed comparators with different reference voltages. The comparator with references of $V_{DD}/2$ will have the minimum offset because its over-drive voltage is the minimum [6]. Other comparators will have higher offset voltages since NMOS transistors are connected to higher reference voltages than $V_{DD}/2$ and PMOS transistors are connected to lower than that. This reasoning is verified by simulating the random offset effect using the Monte-Carlo simulation. Fig. 4 shows the random offset voltage of proposed latches with different references. As the reference voltages deviate from $V_{DD}/2$, the offset voltage increases. The max offset is about 25mV for the references of 1.125 for NMOS and 0.072 for PMOS.

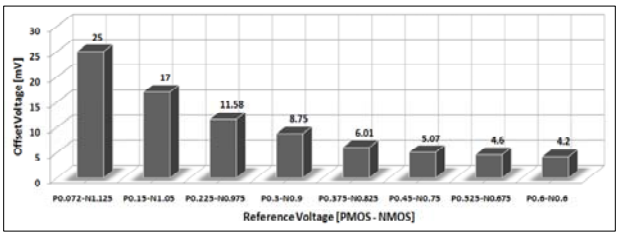


Figure 4. Random offset as a fuction of reference voltage

C. Process variation

Similarly to the previous discussions, process variations also make mismatch between the NMOS and PMOS input pairs, and thus, the designed transistor size for the typical SPICE model is not valid in this case. In order to control the operation condition of NMOS and PMOS so that they can match, we can control the body voltage of transistors by using the proposed body control circuit (comparator replica + negative feedback circuit with op-amp) as shown in Fig. 5. The comparator replica is the half circuit of the comparator when switches on. The output level of the replica is sensed by and the transistor body voltages are controlled in unison so as for the output to be at the center, which means the current through NMOS and PMOS matches, at least. Fig. 6 shows the effect of the proposed body control technique in the comparator with zero reference ($V_{REF}+ = V_{REF}- = V_{DD}/2$). For the matched NMOS and PMOS input pairs for typical SPICE model, the offset voltage due to process variation varies up to 16mV without the compensation circuit. After applying the proposed body control technique, the offset is remarkably reduced. By sharing a single body control circuit for multiple comparators, we can efficiently cancel the NMOS-PMOS mismatch effect.

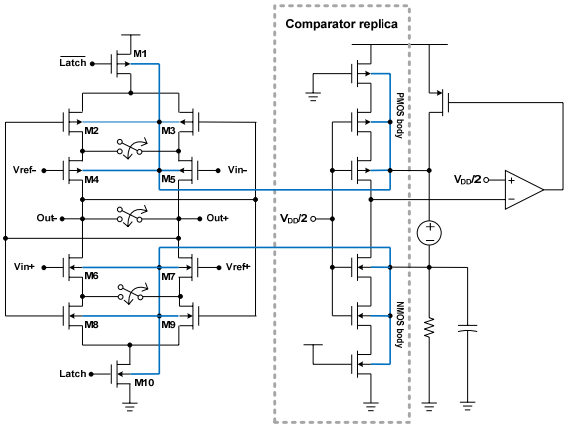


Figure 5. Body control circuit

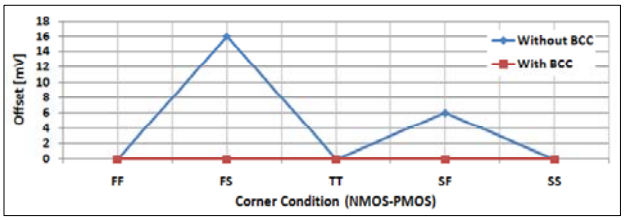


Figure 6. The effect of body control circuit (BCC)

4. Conclusion

This paper has presented a fully differential rail-to-rail input latch with body control circuit for wide dynamic range flash ADC. Various design considerations and design technique have been discussed. Based on the simulation results, the proposed comparators can be used for a 5 bit flash ADC under 1.2V supply.

References

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