A CMOS Linear Preamplifier Design for Electret Microphones

Gil-Seop Park and Seung-Tak Ryu
School of Engineering
Information and Communications University (ICU)
Daejeon, Korea
stryu@icu.ac.kr

***Abstract* — A gm-opamp-RC configured CMOS linear preamplifier for electret microphone is presented in this paper. The transconductance amplifier (gm-cell), as a V/I convertor at the input stage of the preamplifier, adopts a negative feedback loop at its input pair to enhance the linearity of the output current. Feedback loop improves the SFDR of the preamplifier by 9dB. Simulated peak signal-to-noise and distortion ratio (SNDR) is 62 dB at 100mVpp with 2pF switching capacitor load at 2.56 MHz. The preamplifier operates under 1.8V supply voltage and the total current consumption is 190 μA. It has been designed for a 0.18 μm CMOS technology.**

Keywords – Linear preamplifier, gm-opamp-RC, Electret capacitor microphone.

I. INTRODUCTION

Among various types of microphones, electret capacitor microphones (ECMs) have been the most popular for mobile multimedia equipments and hearing aids by virtue of their simple structure and small dimension. The key element of ECM is the electret capacitor. Sound pressure to the electret capacitor changes the distance between the two plates of it. Then the fixed charge in the electret layer generates voltage variation. Thus, the electret capacitor is simply modeled as a capacitive voltage source in series with 2~5 pF capacitor (C_{ECM} in Fig. 1). Because of the high output impedance of the electret capacitor, ECM requires a high input-impedance readout buffer at its output. Traditionally, discrete JFET amplifier has been used for it as shown in Fig.1. Its high impedance gate is suitable for the interface with electret capacitor, and its low resistance load (R_L) at its drain provides output drivability with small gain, usually 1 ~2. Even if JFET seems to be very good solution for the electret capacitor interface, at the same time, it becomes the major source of performance bottle-neck: its nonlinearity limits the total harmonic distortion (THD) and the gate leakage current increases the in-band noise and, therefore, limits the maximum SNR. Single-ended load resistor (R_L) connected to the supply brings on poor PSRR. In addition, on-board signal routing from JFET to the following CODEC is prone to be coupled by the noise. Moreover, JFET cannot be integrated in standard CMOS IC. In order to improve the signal quality and to integrate the high impedance interface

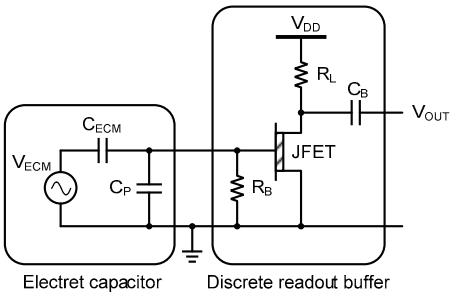

Fig.1. Equivalent circuit of electret capacitor and JFET-based readout buffer.

with other CMOS circuits such as CODEC, recent researches have tried to realize the interface with CMOS preamplifier [1-6]. This paper reviews several previous CMOS preamplifier designs for ECM and focuses on the gm-opamp-RC preamplifier [1] as the most suitable architecture. This work concentrates on the gm cell design in gm-opamp-RC circuit for better linearity.

The organization of this paper is as following. In Section II, several prior arts of ECM preamplifiers are discussed. The proposed linear preamplifier design is discussed in Section III. In Section IV and V, simulation results are represented and analyzed.

II. PRIOR ARTS

Several CMOS preamplifier designs for ECM applications have been reported to overcome the drawbacks of the traditional JFET based interface. This Section reviews cons and pros of the previously reported designs.

Fig.2 shows a sense amplifier topology employing split-frequency feedback [2] to improve the PSRR of the JFET based preamplifier. Similarly to the conventional ECM, this design uses the drain current of JFET buffer and drives the output voltage, which is defined by the currents through feedback resistor R_f. The feedback loop composed of the transconductance amplifier (gm) and the PMOS M_1 between the output and drain node of JFET improves the PSRR. In spite of the advantage of this architecture, this technique is still

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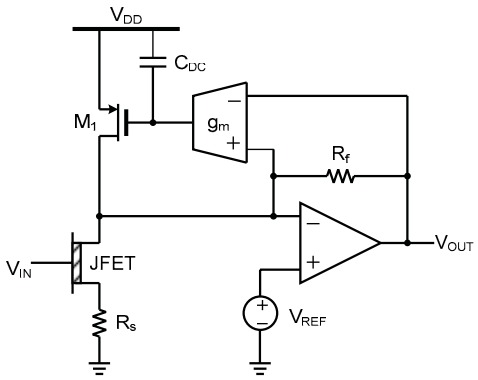


Fig.2. Sense amplifier topology employing split-frequency feedback.

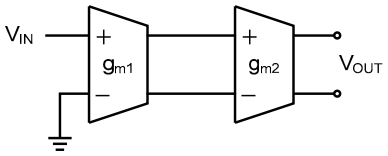


Fig.3. Preamplifier of composed with two fully differential Gm-cells.

based on a discrete JFET, and thus all the disadvantages except for the poor PSRR still exist.

Fig.3. shows the preamplifier architecture with cascaded fully differential transconductors. Traditional JFET is replaced with the open-loop gm-cell for high input impedance, and the fully differential architecture improves the PSRR [3][4]. Although this design can be integrated with CMOS ICs, the second stage gm cell is likely to have too high output impedance to drive the following circuits such as switched-capacitor-based ADCs. And the outdriving with open-loop transconductance amplifier limits the linearity of the output signal.

Fig.4 shows the difference differential preamplifier structure. The main advantage of this configuration is it has enough gain with simple circuit design [5], [6]. It is desirable for the preamplifier to have the differential output for the common noise immunity and high PSRR. The difference differential amplifier shown in Fig. 4, however, has unbalanced output structure, which brings on poor noise immunity and low PSRR.

In order to overcome all the disadvantages discussed above, [1] suggests a simple gm-opamp-RC configured preamplifier as shown in Fig. 5. For the high impedance at the input stage, this design adopts transconductance amplifier similarly to [3]. But the function of gm in [1] is totally different from that of [3]. All the gm cells in Fig. 3 are for voltage amplification, but the gm cell in [1] is a V/I converter. The signal current from the gm cell flows through the feedback resistor R_f of the following inverting amplifier (which is composed of Av and R_f) and generates output voltage. The signal-band gain of this amplifier (G_{PREA}) can simply be expressed as

$$G_{PREA} = g_m \times R_f \quad (1)$$

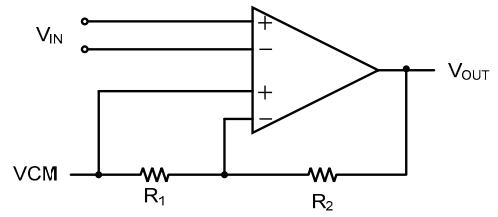


Fig.4. Differential difference preamplifier.

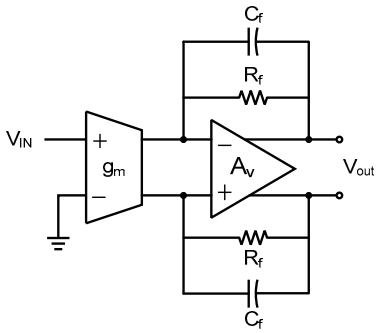


Fig.5. Gm-opamp-RC configured preamplifier with low pass filter.

Because of the negative feedback of the inverting amplifier, the linearity of the output signal and the output drivability are greatly improved when it is compared with the case in Fig.2. Moreover, compared with the g_{m1} in Fig.3, the gm cell in Fig. 5 is more linear because its output voltage is fixed to the signal ground level owing to the virtual grounded output node. And since the structure is fully differential, it inherently provides high PSRR.

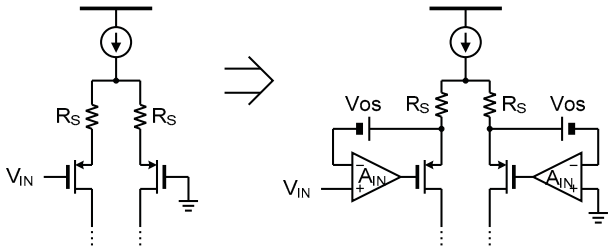
III. Linear Preamplifier Design

From the above considerations, the authors believe that the gm-opamp-RC configuration is the most suitable architecture for the ECM preamplifier design among the known various designs.The goal of this work is to improve the linearity of gm-opamp-RC configured preamplifier. Even though the output current from the gm-cell of the gm-opamp-RC amplifier is more linear than that of the gm cell in Fig. 3, the nonlinearity from the input differential pair is still the major source of the performance limitation. The design is divided into two parts: gm-cell as V/I converter and inverting amplifier as output driver (Opamp-RC, I/V converter).

A. Gm-cell (V/I converter) design

Fig. 6 shows two possible input stage designs for the gm cell. Since the signal from the electret capacitor is centered at ground (refer to Fig. 1), PMOS input differential pair has been used. For well-defined gm, source degeneration resistor, R_S, is inserted. As well known, the linearity of differential pair can be enhanced by the negative feedback amplifier (A_{IN}) along with the source degeneration resistor (R_S) as shown in Fig. 6 (b). Note that the negative feedback loops in both sides have dc level shift (V_{OS}) for proper DC biasing. This is because the input DC level is at ground.

The schematic of the proposed gm cell with the linearized input stage is shown in Fig. 7. Here, the conceptual voltage



(a) Normal input pair (b) Linearized input pair with negative feedback

Fig.6. Input differential pair designs for gm cell.

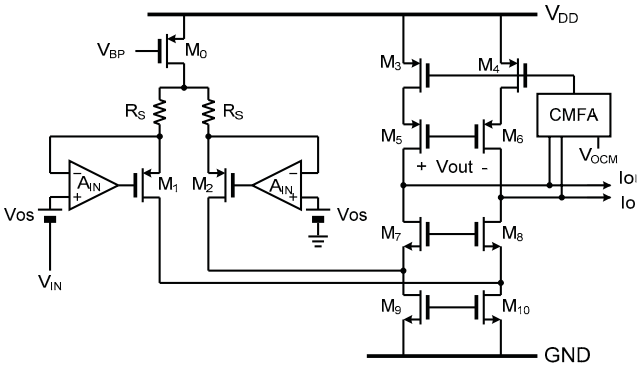


Fig.7. proposed gm cell configuration.

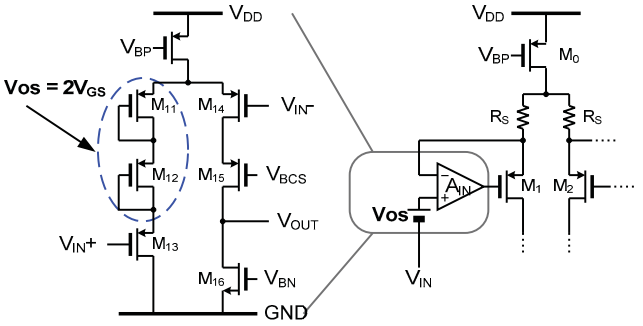


Fig.8. Feedback amplifier for the input stage of gm cell.

source for the DC level shift is attached at the positive input terminal of the opamp (A_{IN}) for the match with the real circuit design in Fig. 8. When the gain of A_{IN} is large enough, the equivalent transconductance of the gm cell is 1/2Rs. The gm cell has a common mode feedback amplifier (CMFA) to set its output common level to be the same as that of the following inverting amplifier (A_V in Fig. 5) so that no DC current flows through the feedback resistor (R_f in Fig. 5). Fig. 8 shows the schematic design of the amplifier, A_{IN}. DC level shifting voltage, V_{OS}, has been realized using two diode connected transistors (M_{11}, M_{12}) between the source node and the tail current source. The sizes of the diode connected transistors have been decided to guarantee enough voltage margin for all the transistors to be in saturation region. For proper work of A_{IN}, its output transistor, M_{16}, must operate in the saturation region even at the minimum input level, which is about -200mV. And M1 should also be in the saturation region at the

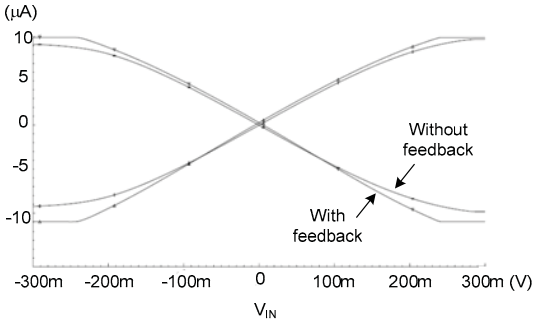
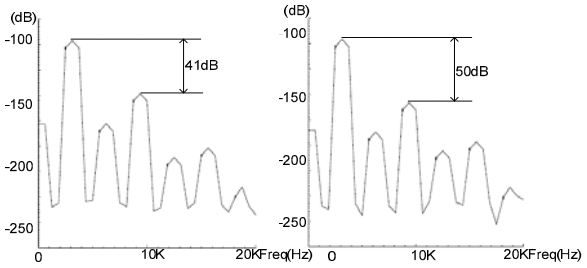


Fig. 9. Output current DC sweep comparison (Linearity test)



(a) Without feedback (b) With feedback

Fig. 10. Comparison of Gm cell output current using FFT.

same condition. These considerations give us the conditions for Vos design as following two equations.

$$-0.2V + V_{OS} > V_{GS1} + V_{DSAT16} \quad (2)$$

$$-0.2V + V_{OS} > V_{DSAT1} + V_{DSAT9} \quad (3)$$

Also, the tail current source of the input pair of the gm cell, M_0, must be in the saturation region even when the input signal is the maximum, which is about + 200mV. Thus, the maximum voltage condition of V_{OS} comes from the following equation.

$$0.2V + V_{OS} + \text{IR drop through } R_S + V_{DSAT0} < V_{DD} \quad (4)$$

From the above three conditions, (2), (3) and (4), V_{OS} has been decided to be 0.9V and it has been achieved by changing the W/L of M_{11} and M_{12}. M_{15} is a cascode device for high output impedance of A_{IN} for the gain enhancement. The simulated gain of the feedback loop composed of A_{IN} and M_1 is 39dB and its phase margin is more than 90 degree at 1.4MHz unity loop gain frequency. Fig. 9 compares the output current DC sweep result of the two gm cell designs, one is without feedback and the other is with feedback as in Fig. 6(a) and (b), respectively. Fig. 10 shows the output current FFT results. Harmonic distortion of the proposed configuration as in Fig. 7 and Fig. 8 has 9dB higher SFDR than the gm cell without input feedback. These results show that the linearity of the output current of the proposed one has better linearity.

B. Inverting amplifier (I/V converter) design

The inverting amplifier as an I/V converter (Opamp-RC part) of the gm-opamp-RC preamplifier in Fig. 5 has been designed with a normal two stage opamp along with a common mode feedback amplifier. It has been designed to have maximum

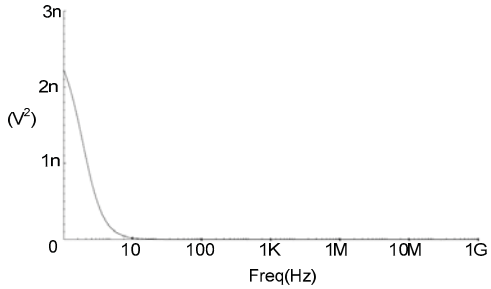


Fig. 11. Noise simulation of the designed preamplifier

TABLE I. PPERFORMNACE SUMMARY

Type	Without feedback	With feedback
Current consumption	160uA	190uA
SNR @ Vin = 1Vpp	82dB	81dB
THD @ Vin=100 mVpp	-54dB	-63dB
SNDR @ Vin 100 mVpp	53dB	62dB

output swing up to 2Vpp differential at 400mVpp single-ended input signal at the gm cell. Feedback capacitor (Cf in Fig. 5) has been used to reduce noise for better SNR.

IV. SIMULATION RESULTS

Proposed circuit has been designed for CMOS 0.18μm process and the supply voltage is 1.8V. The output noise of the proposed gm-opamp-RC preamplifier was simulated as shown in Fig. 11. Since the ADC to be connected to this preamplifier, which is not discussed in this paper, is expected to have 2.56MHz sampling frequency and the target signal bandwidth is 20kHz, SNR was calculated using the equation (5).

$$\mathrm{SNR} = 10 \times \log\left(\frac{\mathrm{P_{signal}}}{\sum_{20}^{20\mathrm{K\,Hz}} \mathrm{P_{noise}} + \left(\sum_{20\mathrm{K\,Hz}}^{1\mathrm{G\,Hz}} \mathrm{P_{noise}}/\mathrm{OSR}\right)}\right) \quad (5)$$

Note that flicker noise should not be divided by OSR and the noise has been integrated up to 1GHz since the noise contribution above 1GHz was measured to be negligible. OSR is 64. The simulated SNR at 1Vpp input is 81dB while the design without feedback (as in Fig. 6(b)) is 82dB.

Transient simulation of the proposed preamplifier has been performed to check the harmonic distortion with real switching load. In this design, the load capacitor is assumed to be 2pF and the switching frequency is 2.56MHz. Simulated THD at 3.125kHz 100mVpp input signal is -63dB with 4096 samples. Table I compare the performance of two designs: One is with the conventional degenerated differential pair at its gm stage (as in Fig. 6(a)) and the other is with the linearization feedback (as in Fig. 6(b)). Due to the increased number of devices and current branches, linearized gm cell with feedback draws 30uA more current, which is about 16% increase of power consumption. And the noise degradation is

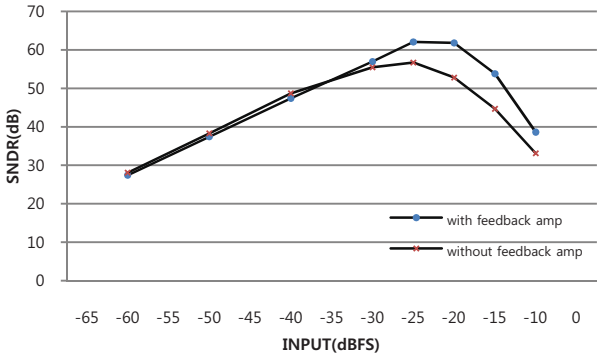


Fig. 12. SNDR measurment

1dB which is thought to be negligible. Compared with disadvantages on power and noise, the linearity improvement is noticeable since it increases SFDR by 9dB. Fig. 12 shows the SNDR simulation results. Simple source degenerated differential pair (as in Fig. 6(a)) shows better SNR when the signal is small because of its simplicity, but its linearity degrades as the signal become larger. On the contrary, SNDR with the linearized gm cell keep increasing until the signal becomes -20dB which is about 100mVpp signal. When the signal is large, proposed design shows higher SNDR due to the increased linearity and results in higher dynamic range. In this plot, 0dB means single ended 1Vpp input signal.

V. CONCLUSION

In this paper, gm-opamp-RC configured CMOS preamplifier for ECM application has been designed focused on the linear gm cell design. The differential pair of the gm cell has been linearized by virtue of the negative feedback. Intentional offset voltage in the feedback amplifier generated using diode connected transistors simply solves the DC biasing problem. With 16% power overhead and 1dB noise loss, proposed design achieves 9dB higher peak SNDR. Proposed preamplifier design is very suitable for the ECM application especially where the large signal is important.

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