

# A Time-Interleaved Flash-SAR Architecture for High Speed A/D Conversion

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**Abstract**— A time-interleaved flash-SAR ADC architecture has been suggested for high speed A/D conversion. Owing to the MSBs determined by the front end flash ADC, SAR ADC completes the A/D conversion in a reduced number of cycles. Time-interleaved SAR ADCs with a commonly shared low resolution flash ADC provide a new size and power efficient high speed ADC architecture. The proposed ADC structure has been verified by developing a behavioral model of a 6-bit 1.2GHS/s ADC. Circuit design considerations have also been discussed based on the sampling network mismatch between the flash and SAR ADCs.

## I. INTRODUCTION

Over the past years, flash ADCs have been dominantly used for low resolution high speed A/D applications such as ultra-wide band (UWB) receivers, optical and magnetic storage systems and satellite receivers. However, as deep submicron CMOS technologies accelerate the transistor operation speed, recently, low power successive approximation register (SAR) type ADCs can replace the traditional flash ADC being assisted by the time-interleaved technique. For example, in [1], eight identical time-interleaved channels of SAR ADCs have been used for a 6-bit 600MHz ADC design. Since the traditional binary search algorithm based SAR ADCs require  $n+1$  clock cycles for  $n$ -bit decision including a sampling period, a massive time-interleaved technique has to be used. However, increasing the number of time-interleaved channels is not desirable because of the offset, timing mismatch, and gain errors between the channels. Thus, highly time-interleaved designs often require mismatch calibration schemes or redundant channels [2]. Such an inherent speed limitation of SAR ADC could be improved by the 2-bits/cycle decision algorithm [3]. However, according to [3], in order to determine 2-bits/cycle, the hardware complexity has been increased about 3 times compared with normal SAR ADCs.

This paper presents a new high speed ADC architecture based on a flash-assisted SAR decision algorithm. By achieving several MSBs in one clock cycle using a front-end low-resolution flash ADC, many clock cycles can be reduced from the SAR operation. In addition, by applying a time-interleaving technique to the suggested structure, total

conversion time can be greatly reduced. By sharing the front-end flash ADC with the time-interleaved SAR ADCs, hardware and power efficiency are achieved.

This paper is organized as following. In Section II, the operational principle of the time-interleaved flash-SAR architecture is explained. In Section III, the Simulink<sup>®</sup> behavioral model of a 6-bit 1.2GS/s ADC is developed, and its simulation results are demonstrated to verify the operation of the proposed architecture. In Section IV, circuit design considerations are discussed. Finally, conclusions are made in Section V.

## II. TIME-INTERLEAVED FLASH-SAR ARCHITECTURE

### A. Flash-SAR architecture

Fig. 1 (a) shows a symbol and a timing diagram of the conventional binary searching 6-bit SAR ADC. In conventional design, total 7 clock cycles are used for one A/D conversion. The first clock cycle is used for input sampling, and the rest 6 cycles are used for code decisions, from MSB to LSB. Since the number of clock cycles increase as much as the resolution increase, this decision algorithm becomes inherent speed bottleneck of SAR ADC.

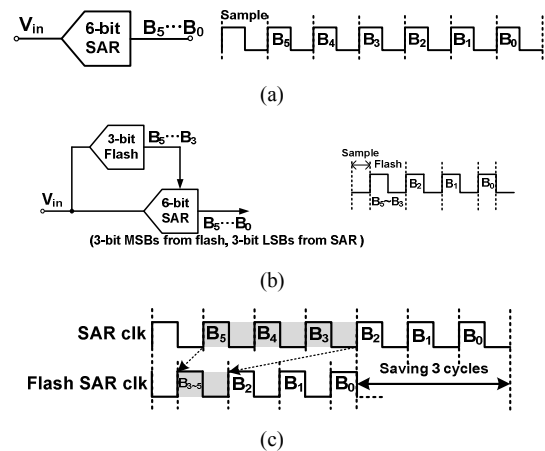


Figure 1. (a) A 6-bit conventional SAR block, (b) a proposed 6-bit flash-SAR block, (c) timing diagram of (a), (b).

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In the proposed flash-SAR architecture, several MSBs are achieved at one clock cycle by the front-end flash, and the rest codes (LSBs) are decided by the normal SAR algorithm. The conceptual block diagram of the proposed ADC for 6-bit resolution is shown in Fig. 1 (b). This structure is composed of a 3-bit flash ADC and a normal 6-bit SAR ADC. At the beginning of the flash-SAR ADC operation, both flash and SAR ADCs sample the input signal at the same time.

After the input sampling is done, during the second half period of the first clock cycle, the flash ADC converts the sampled signal into 3-bit MSBs ( $B_5, B_4, B_3$ ). Now, since the 3 MSBs are known, the 6-bit SAR ADC can start the decision from  $B_2$  by using the MSB information. This reduces total 3 clock cycles from the normal SAR operation and, therefore, a 6-bit flash-SAR ADC completes A/D conversion in four clock cycles. Note that since the SAR ADC has a full 6-bit DAC, this architecture does not need to generate a residue signal. However, even if the power consumption from a 3-bit flash can be much less than that of a 6-bit SAR ADC [5], its overhead is considered in this design, and we suggest a new power and size-efficient flash-SAR based high speed time-interleaved ADC architecture.

### B. Time-interleaved flash-SAR architecture.

In order to further increase the conversion speed of the flash-SAR ADC, time-interleaving technique is adopted. Unlike other time-interleaving techniques, the flash-SAR architecture does not need to have flash ADCs in every channel. As can be seen in Fig.1 (b), the flash ADC completes the 3-bit MSB decision in a single clock cycle and does not work until the SAR finishes the whole conversion. Thus, a single 3-bit flash ADC can be shared by multi channel of time-interleaved SAR ADCs.

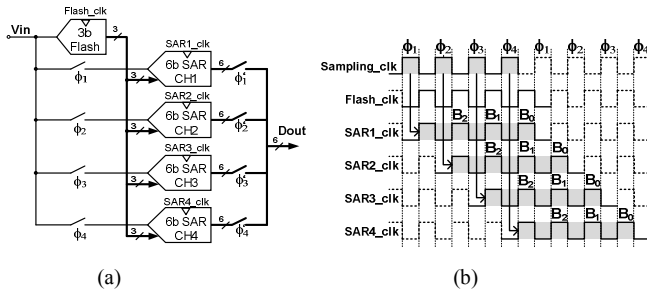


Figure 2. (a) A 6-bit 4 channel time-interleaved (TI) flash-SAR block, (b) Timing diagram of the 6-bit 4 channel TI flash-SAR.

Fig. 2 shows the proposed time-interleaved flash-SAR ADC architecture and the corresponding timing diagram. As shown in Fig.2 (a), one 3-bit flash ADC and four 6-bit SAR ADCs are used as a design example of 6-bit ADC. The flash ADC operates at every clock cycle and a single channel SAR ADC samples the input at every four clock cycles in turns. Owing to the flash ADC, the conversion speed of the proposed 6-bit SAR ADC is increased, and it is the same as that of a 3-bit time-interleaved SAR ADC.

The hardware efficiency and the expected figure of merit (FoM) of the proposed architecture are to be compared with previous designs in [3][4]. In [4], a 6-bit two-step sub-ranging architecture employing a 3-bit flash ADC as a course ADC

and two 4-bit flash ADCs as fine ones was introduced. The coarse ADC is shared by both fine channels like the proposed architecture in this paper. However, the number of comparators which need 6-bit offset cancellation is much more than that in the proposed architecture, and therefore, the power and area overhead related to the flash offset cancellation can be the major drawback of [4]. Also, the 2-bit/step SAR ADC [3] can be compared with the proposed work. In [3], equivalently three 6-bit SAR ADCs are used to build a single channel 2-bit/step SAR ADC while the required number of clock cycles is the same as that of the proposed work. Thus, if 4-channel time-interleaved is assumed for both designs, the hardware complexity of 2-bit/step design corresponds to twelve normal SAR ADCs while that of the proposed ADC corresponds to four SAR ADCs plus one 3-bit flash ADC. According to the comparison between the flash and SAR in [5], 3-bit flash has better power efficiency than any resolution SAR ADCs. Thus, the flash-SAR structure has about one third FoM of the 2-bit/step SAR architecture. The FoM of the proposed ADC can be roughly calculated as Table I.

TABLE I. COMPARASION FIGURE OF MERIT

Type	Figure of Merit(6-bit, 1.2GHz S/s, normalized)		
	Structure	Single	4 channels
2-bit/step ADC in [3]	Three SAR ADCs	1	4
This work	One flash and one SAR ADCs	0.34	1.37

Based on the Fig 4 in [5].

### III. BEHAVIORAL MODEL DEMONSTRATION.

To verify the operation of the proposed time-interleaved flash-SAR ADC architecture, the behavioral model of a 6-bit 1GS/s ADC with a 3-bit flash and 4 channel time-interleaved 6-bit SAR has been developed using Simulink<sup>®</sup>. The model has been developed as close as possible to the real circuit operation: It includes the time delay of latches in comparators and the lumped gate delays in critical logic path. In addition, all the control signals required inside the ADC are generated from the model using the input clock and logic gates.

#### A. Flash model

A 3-bit flash ADC model has been developed for the schematic shown in Fig. 3.

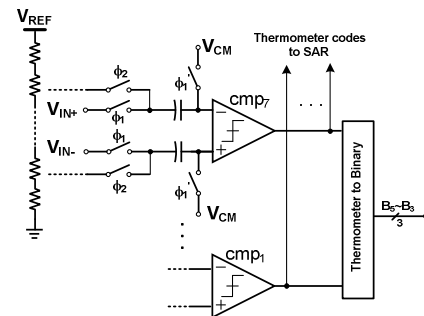


Figure 3. A 3-bit flash model

Since the 3-bit flash ADC and SAR ADC should sample the same input signal, the sampling network should be matched

each other, so the switched-capacitor-based comparator structure is assumed for the flash.

In the Simulink®, the flash ADC model is implemented as shown in Fig. 4. All comparators have fully differential structure, and the full scale reference voltages are assumed to be 1.8V and 0V (rail-to-rail). By assuming the reference voltages are defined by resistor string, each reference voltage is equally divided by the flash ADC's step size. Just like how the real circuit operates, the difference of differential input signal is compared with the difference of the differential reference levels.

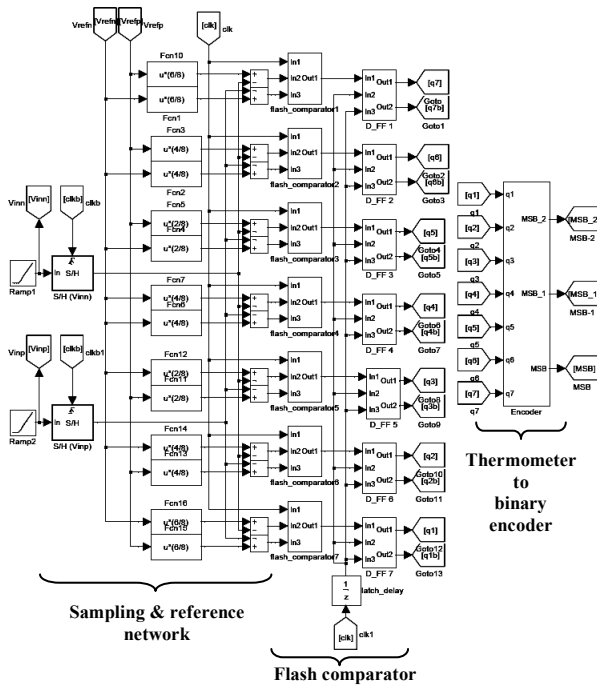


Figure 4. A 3-bit flash schematic in Simulink®.

The array of seven comparators generates 7-bit thermometer code, and the code is sent to SAR ADCs to control their switched-capacitor DACs. To model the comparator's latching delay and control gate delays, each comparator's output is transferred after 400ps time delay. This modeling is done by attaching a D-flip flop in each comparator output.

### B. SAR model.

The 6-bit SAR ADC has been modeled based on the bottom sampling switched-capacitor DAC structure. Note that the flash ADC modeling is made with the assumption of the switched-capacitor sampling network to match two ADCs.

Just like the flash ADC model, the SAR ADC's Simulink® model has a fully differential structure, and its full scale is assumed to be 1.8V supply level and the ground level. So are the reference levels. Since the 3-bit MSBs of the 6-bit DAC in SAR are controlled by the flash ADC, 7-bit thermometer code has been directly used at DACs in SAR and, thus, the 3 MSB capacitors are composed of 7 identical unit capacitors.

Each of those seven capacitors has its own voltage weight of  $4C_{unit}/C_{total} * 1.8V$ , and it is controlled by the thermometer code.

Here,  $C_{unit}$  is the capacitor value for LSB of the 6-bit DAC, and  $C_{total}$  corresponds to  $2^6 C_{unit}$  plus the parasitic capacitance ( $C_p$ ) at the comparator input node. The rest 3 LSBs are decided by the normal SAR operation.

Each reference has its own weight depending on the corresponding code position, such as  $4C_{unit}/C_{total}$ ,  $2C_{unit}/C_{total}$  and  $C_{unit}/C_{total}$ . In order to model the logic delay, lumped time delay has been inserted in the critical feedback path of SAR logic in between the comparator output and the DAC networks.

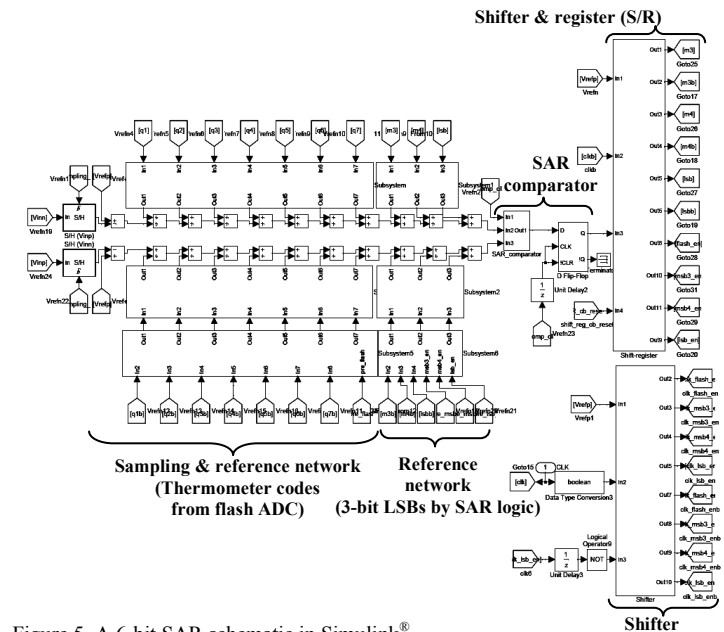


Figure 5. A 6-bit SAR schematic in Simulink®.

The shifter and register (S/R) blocks for SAR logic are composed of seven D-flip flops, and the S/R generates SAR's operating signals and stores 3 LSB data as well.

The comparator latch delay and the lumped logic delay in the feedback path from the comparator to the DAC are assigned as shown in Fig. 6. This realistic delay model limits the developed flash-SAR model to operate with 1.2GS/s as the maximum speed.

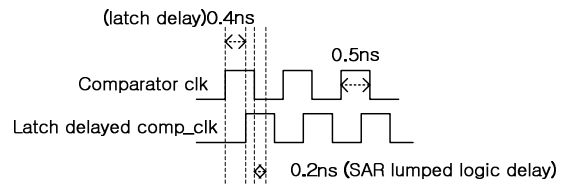


Figure 6. The modeled SAR ADC's delay assignment.

The developed model for the flash-SAR ADC generates all the control signals based on the input clock just like the real circuit does. To make it possible, one extra shifter and logic gates are added. Each channel has its own flash clock and comparator clock signals. The flash clock signal is generated for each SAR ADC to take its MSB data from the flash ADC at appropriate timing, and the comparator clock is for the SAR's comparator which turns on 3 times for sampling conversion.

### C. Time-interleaved flash-SAR model

Based on the developed 3-bit flash model and the 6-bit SAR ADC model, a 4-channel time-interleaved 6-bit flash-SAR structure has been developed. For that, a 4-bit shifter enables each SAR ADC to turn on, and eight D-flip flops synchronize the flash output code with the SAR ADC output.

The whole schematic of the proposed ADC and the operating signals of each channel are shown in Fig. 7.

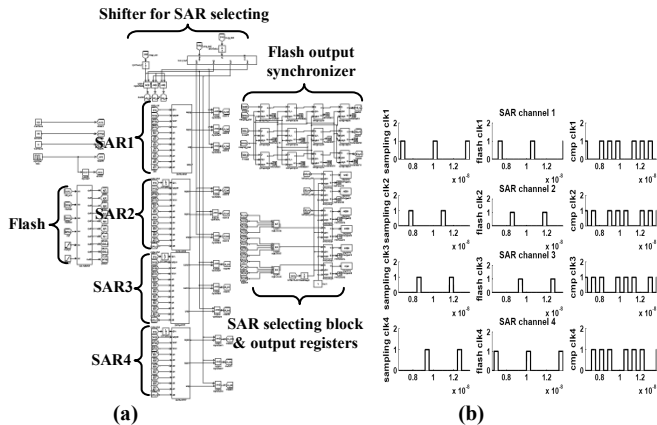


Figure 7. (a) The time-interleaved flash-SAR block, (b) sampling clock, flash clock, comparator on signals for each channel.

In order to test the validity of the proposed ADC architecture, the simulation has been conducted with a ramp signal and sine wave. The results are shown in the Fig. 8. Fig. 8 (a) is the output code for the ramp signal and, total 64 codes have been successfully generated at 1.2GS/s operation. The FFT simulation result for the 441MHz input signal at the same speed is shown in Fig. 8 (b). The SNR of the time-interleaved flash-SAR is 37.6 dB, and effective number of bit (ENOB) is 5.96 bits with no error sources in the model.

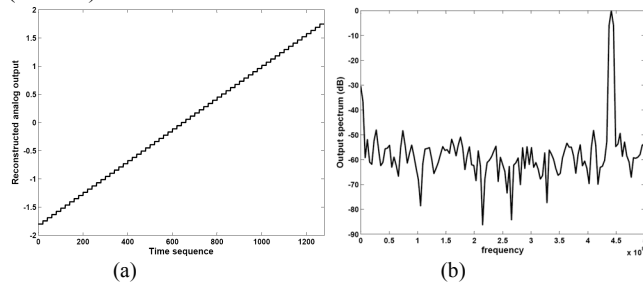


Figure 8. (a) The rail to rail ramp signals applied output, (b) the result of FFT simulation at 441MHz.

### IV. DESIGN CONSIDERATIONS

To design the proposed time-interleaved flash-SAR ADC, gain error, offset error, and timing errors between channels should be considered as in normal time-interleaving design. In addition, this particular architecture should consider one more design point. Even if the model assumes the same bottom-sampling network for the flash and the SAR, there happens a critical mismatch in the reference level due to the parasitic capacitance effect at the input of the comparator. Fig. 9 explains the reference scaling effect in flash and SAR ADCs.

The input signal and the reference levels at the input node of the comparator in flash ADC are reduced with the same ratio by input parasitic capacitance, so there is no reference level scaling effect. However, in the sampling network of the SAR ADC, only the reference level is scaled by the input parasitic capacitance. Thus, considerable amount of reference level mismatch can occur if the parasitic effect is not counted. Hence, the parasitic capacitance ( $C_p$ ) should be less than the minimum capacitor ( $C$ ) for LSB decision.

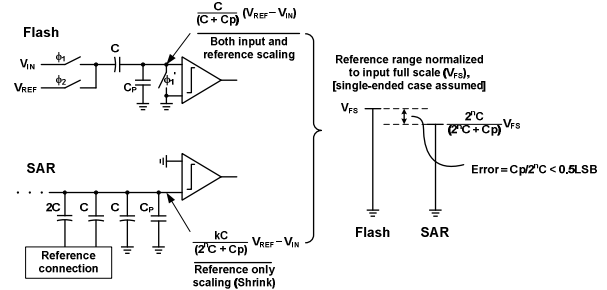


Figure 9. Gain error in flash and SAR ADCs.

Also, the offset of the comparators in flash and SAR degrades the ADC linearity. Roughly when the comparators have more than 0.5 LSB offset of 6-bit resolution, the overall ADC can have missing codes. Hence, the offset cancellation scheme should be applied for the real circuit design.

Besides, to guarantee the same input sampling at flash and SAR, both sampling networks should have the same RC time constant.

### V. CONCLUSION

A time-interleaved flash-SAR ADC architecture for high speed A/D conversion has been proposed. Flash ADC reduces SAR decision cycles, and the time-interleaved technique with a shared flash ADC enables high speed A/D conversion with a small hardware and power overhead. The operation of the proposed architecture has been proved by the 6-bit 1.2GS/s ADC Simulink<sup>®</sup> model, and the circuit design considerations are considerations have been studied.

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