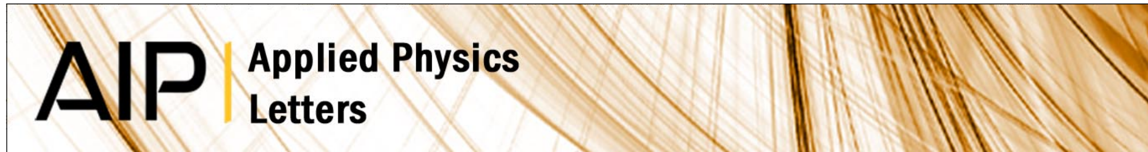

Seeding atomic layer deposition of high-k dielectric on graphene with ultrathin poly(4-vinylphenol) layer for enhanced device performance and reliability

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Seeding atomic layer deposition of high-k dielectric on graphene with ultrathin poly(4-vinylphenol) layer for enhanced device performance and reliability

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We demonstrate that ultrathin poly(4-vinylphenol) (PVP) acts as an effective organic seeding layer for atomic layer deposition (ALD) of high-k dielectric on large-scale graphene fabricated by chemical vapor deposition (CVD). While identical ALD conditions result in incomplete and rough dielectric deposition on CVD graphene, the reactive groups provided by the PVP seeding layer yield conformal and pinhole-free dielectric films throughout the large-scale graphene. Top-gate graphene field effect transistors fabricated with the high quality, PVP-seeded Al_2O_3 gate dielectric show superior carrier mobility and enhanced reliability performance, which are desirable for graphene nanoelectronics. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4737645]

Graphene, a layer of carbon atoms, has attracted much attention for use in future nanoelectronics due to its superior electrical properties.[1] Owing to its extremely high carrier mobility and controllable carrier density, graphene is a promising material for practical applications, particularly as a channel layer of high-speed FET.[2,3] However, the lack of dangling bonds in the graphene plane leads to difficulty in depositing dielectric films on graphene by atomic layer deposition (ALD), which is the most suitable and widely used technique to form an ultrathin gate dielectric layer.[4] In order to deposit dielectrics on graphene, several surface treatments have been proposed, including oxidation of metal films[5] and functionalization processes.[6,7] However, these methods have been investigated with mechanically exfoliated, nanometer-scale graphene flakes that are not suitable for mass production of functional devices. The integration of uniform and pinhole-free dielectric with large-scale graphene still remains a major challenge. One of the most promising methods to synthesize high-quality graphene is metal-catalyzed chemical vapor deposition (CVD) because it provides large-scale production of monolayer graphene films with excellent electrical properties.[8,9] In contrast to mechanically exfoliated, defect-free graphene, CVD graphene contains large intrinsic defects and dislocations arising from the rough metal surface and inevitable graphene transfer processes,[9] which may affect the subsequent ALD growth. However, ALD of high-κ dielectrics on CVD graphene has not been systematically investigated thus far, although it would enable the precise control of ultrathin oxide films on large-scale monolayer graphene, ultimately leading to improvement of dielectric scaling capability and device reliability.

In this work, we explore the feasibility of ALD of high-κ dielectric on the large-scale monolayer graphene fabricated by CVD. Although the Al_2O_3 film formed by ALD fully covered the underlying CVD graphene, it resulted in incomplete and rough dielectric film with large pin-holes. We further demonstrate that ultrathin poly(4-vinylphenol) (PVP) (5 nm) acts as an effective seeding layer for facilitating ALD on top of the CVD graphene and that the PVP-seeded Al_2O_3 film possesses high uniformity and low defect density. Then, top-gate CVD graphene FETs are fabricated with high-quality, PVP-seeded Al_2O_3 gate dielectric. Compared to the control devices without seeding layer, the graphene FETs with PVP-seeded Al_2O_3 dielectric exhibited much higher FET mobility (3600 cm^2/Vs extracted with two-terminal transconductance) and enhanced reliability performance under gate bias stress. These results are important for evaluating the feasibility of large-scale graphene-dielectric integration, which is the major obstacle to future graphene electronics.

For large-scale graphene-dielectric integration, graphene film was grown on a Cu film via CVD at a temperature of 680 °C. The CVD graphene synthesized on the Cu film was subsequently transferred onto a SiO_2 substrate and characterized with Raman spectroscopy (514 nm).[3] By controlling the solution concentration, an ultrathin PVP (5 nm) film was spin-coated on top of graphene and annealed at 180 °C for 1 h. Poly(melamine-coformaldehyde) and propylene glycol monomethyl ether acetate were used as a cross linking agent and solvent, respectively. The PVP thickness was confirmed by the measurement of the edge step height using atomic force microscopy (AFM).[10] The ALD of Al_2O_3 (20 nm) was prepared using trimethyl aluminum (TMA, Aldrich, 99.99%) and H_2O as a precursor and oxygen source, respectively.[9]

We first carried out this study on a direct ALD of high-k dielectric on CVD graphene. The surface roughness of CVD graphene immediately after transfer process is around ∼10 Å. Figures 1(a) and 1(b) present AFM images of the area before and after ALD of 20 nm of Al_2O_3, respectively. The Al_2O_3 film directly grown on the CVD graphene is patchy and discontinuous, which confirms previous reports about ALD on mechanically exfoliated graphene flakes[4] or highly oriented pyrolytic graphite (HOPG).[11] Furthermore, we observed that the CVD graphene was fully covered by the Al_2O_3 film even though the film has a rough surface (rms surface roughness ∼10 Å), which is different from the case

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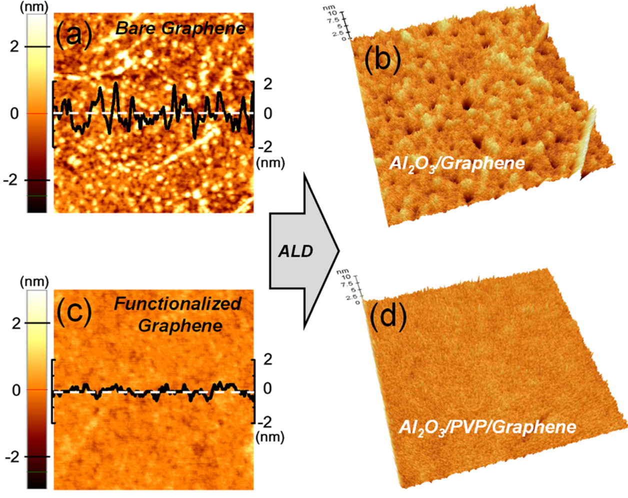

FIG. 1. Surface morphology of (a) bare CVD graphene, (b) Al_2O_3/graphene, (c) functionalized graphene, and (d) Al_2O_3/functionalized graphene films. Scan size is $1 \times 1\ \mu m^2$ for all images. The rms surface rougness of graphene becomes much smoother after the functionalization using PVP. The Al_2O_3 film deposited on the functionalized CVD graphene shows a much smoother morphology than that of the Al_2O_3 on bare CVD graphene.

of pristine graphene.[4] This suggests that the ALD nucleation on CVD graphene is more efficient compared to that on pristine graphene; this discrepancy may be attributed to the intrinsic defects in the CVD graphene. However, the large pinholes and the roughness provided by the direct ALD on CVD graphene are still problematic given that these factors ultimately degrade oxide reliability in terms of leakage current and dielectric strength. In order to improve the uniformity of the high-k dielectric, 5 nm of PVP was used as an organic seeding layer; this functionalization process was carried out by spin coating of PVP on top of CVD graphene. PVP has often been utilized as a gate dielectric for organic FETs due to its good insulating properties; it is known to possess a relatively high dielectric constant (>4).[10] The rms surface roughness of PVP-coated graphene is less than ~3 Å. Figures 1(c) and 1(d) present AFM images of the surface of the PVP/graphene and the Al_2O_3/PVP/graphene, respectively. Following the functionalization of CVD graphene with the PVP seeding layer, the resulting ALD dielectric film showed high uniformity and low defect density; it appeared to conformally coat the large-scale graphene films. The root-mean-square (rms) surface roughness of the PVP-seeded Al_2O_3 is less than 5 Å. The superlative uniformity of the PVP-seeded Al_2O_3 is attributed to the functional groups contained in the PVP seeding layers. Figure 2(a) shows attenuated the total reflection Fourier transform infrared (ATR-FTIR) spectra for the functionalized graphene. It is revealed that the PVP seeding layer possesses abundant functional groups such as O-H and C-H that facilitate the subsequent ALD. We also observed that the contact angle of CVD graphene (76° ± 2°) transferred on SiO_2 decreased after the chemical functionalization (62° ± 2°) due to the hydrophilic O-H groups. We found that the measured contact angle of our CVD graphene is lower than those found in pristine graphene or epitaxial graphene grown on silicon carbide.[12]

Another important aspect that must be considered for graphene-dielectric integration is that we must render graphene intact even after dielectric formation, because additional defects can readily be generated in the graphene lattice during the dielectric deposition. Figure 2(b) shows the Raman (514 nm) measurements taken before and after the functionalization using PVP. We observed no change in the D-band located at ~1350 cm^{-1} and I_{2D}/I_G, indicating that the solution-processed PVP layer can be formed on top of the CVD graphene without introducing additional defects or doping effects in the graphene.[13]

With the high-quality PVP-seeded Al_2O_3, we further demonstrated high performance graphene FETs that is the most feasible application of graphene. Figure 3(a) describes the cross sectional view of the proposed top-gate graphene FET structure with the PVP layer. The graphene active region was defined by oxygen plasma and Au (30 nm)/Cr (5 nm) were deposited for source, drain and gate electrodes. Figure 3(b) shows the microscopy images of the top-gate graphene FETs. For comparison purposes, devices without a PVP seeding layer were also fabricated. Figure 3(c) shows the representative transfer (I_{DS}-V_G) characteristics of the top-gate graphene FETs with PVP-seeded Al_2O_3 and a single Al_2O_3 dielectric at $V_{DS} = 1$ V. The PVP-seeded devices exhibit much higher electron and hole currents and better gate controllability compared to the control device. The superior current drivability of the device with the PVP-seeded dielectric is attributed to the enhanced carrier mobility, which can be extracted using the following equation:

$$\mu_{FET} = \frac{LG_m}{WC_{ox}V_{DS}},$$

where G_m is the two-terminal transconductance, L and W are the channel length and width, C_{ox} is the capacitance density, and V_{DS} is the drain voltage. The capacitance densities of single and PVP-seeded dielectrics were 395 nF/cm^2

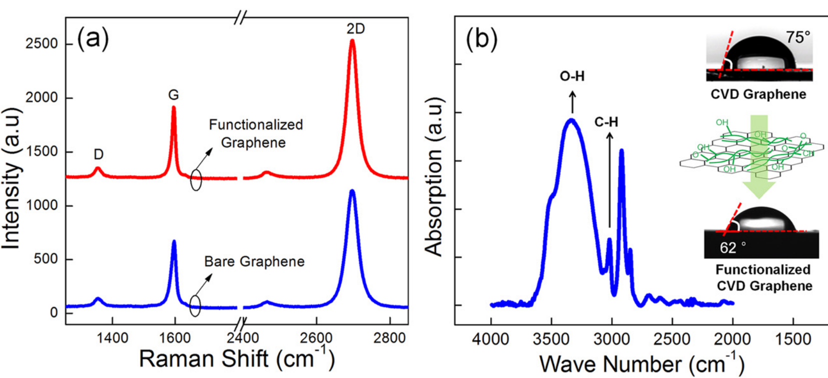

FIG. 2. (a) AT-FTIR spectroscopy of the functionalized CVD graphene surface with PVP, showing the presence of O-H and C-H functional groups. (b) Raman spectroscopy of the monolayer CVD graphene before and after functionalization with PVP. The measurement is performed with an excitation wavelength of 514 nm. The PVP was uniformly formed while preserving the sp^2 carbon framework of the large-scale graphene.

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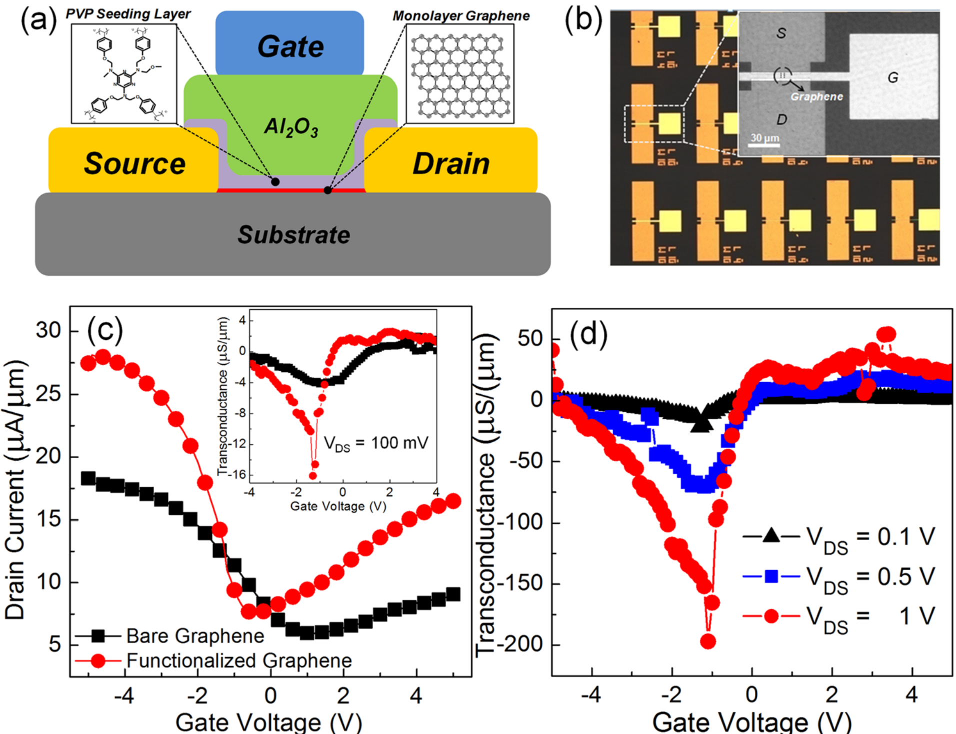

FIG. 3. (a) Schematic diagram showing top-gate graphene FET structure with PVP-seeded Al_2O_3 gate dielectric. (b) Microscopy images showing large scale device integration. (c) Representative I_D-V_G characteristics of top-gate graphene FET before and after the CVD graphene channel is functionalized with PVP. The channel length and width of the devices are 4 and 8 μm, respectively. The inset figure shows the transconductance of the graphene FETs with different gate dielectrics as a function of gate voltage. (d) G_m-V_G characteristics of the PVP-seeded graphene FET for different drain voltages. The maximum peak transconductance is as high as 200 μS/μm at $V_{DS} = 1$ V.

(dielectric constant $\kappa = 9$) and 250 nF/cm^2 ($\kappa = 7$), respectively. Based on the standard parallel plate capacitor model ($1/C_{total} = 1/C_{PVP} + 1/C_{Al2O3}$), the dielectric constant of PVP seeding layer in our experiment is estimated to be ~4, which is higher than that of SiO_2. The transconductance of devices with different dielectrics are shown in the inset image in Fig. 3(c). The peak transconductance of the device with the PVP-seeded dielectric is much higher than that of the device with a single dielectric, and the measured maximum transconductance is 200 μS/μm at $V_{DS} = 1$ V (Fig. 3(d)). The hole and electron mobility of the device with the PVP-seeded dielectric, extracted based on the peak transconductance shown in Fig. 3(c), were found to be 2710 cm^2/vs and 625 cm^2/vs, respectively, while the control device showed a much lower hole (450 cm^2/vs) and electron (220 cm^2/vs) mobility. The low carrier mobility for the control device with the Al_2O_3 dielectric can be attributed to the defects in graphene generated by the ALD process or to the charged impurities at the graphene/dielectric interface.[14–16] In contrast, the maximum measured carrier mobility among the devices with the PVP-seeded graphene FET is 3600 cm^2/vs which is an exceptional value for top-gate FET based on CVD graphene. It should be noted that our mobility is extracted using two-terminal transconductance, G_m instead of $I_{DS}/(V_{GS}$-$V_{Dirac})$. Different procedures have been utilized to extract the mobility of graphene, which make the accurate comparison with reported mobility values in the literature difficult.

The measured maximum mobility is much higher than previously reported values based on the same mobility extraction technique as that used in our work.[17,18]

In addition to the electrical performance, the bias stress reliability of the top-gate graphene FETs was tested, with results as shown in Fig. 4. The time-dependent changes of Dirac voltage (V_{Dirac}) and carrier mobility for the devices before and after the functionalization were measured under the same gate electric field of 0.4 MV/cm. As shown in Fig. 4(a), large V_{Dirac} shift and mobility degradation were observed for the control device without the PVP seeding layer after application of gate bias stress for two hours. On the other hand, the V_{Dirac} shift and the mobility degradation were significantly reduced for the device with the PVP-seeded Al_2O_3 gate dielectric (Fig. 4(b)). In particular, the

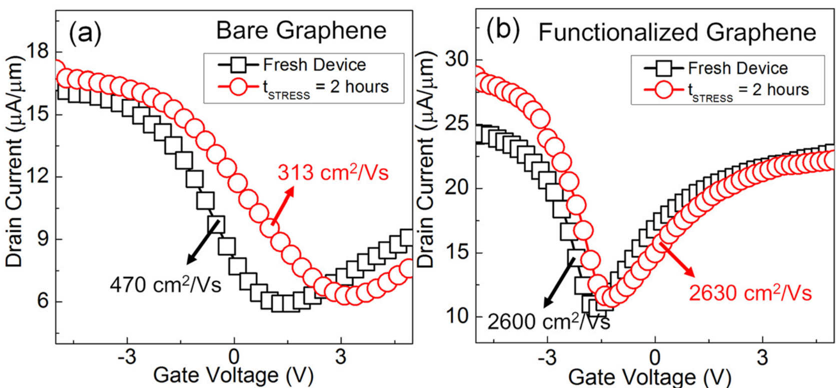

FIG. 4. The time-dependent behavior of V_{Dirac} and the carrier mobility of the graphene FETs (a) before and (b) after the functionalization of graphene channel region with PVP seeding layer. The gate stress field is 0.4 MV/cm. The PVP-seeded device has a much smaller ΔV_{Dirac} (0.7 V) than that of the control device (2 V). A negligible carrier mobility change after gate bias stress is obtained with the functionalized graphene channel layer.

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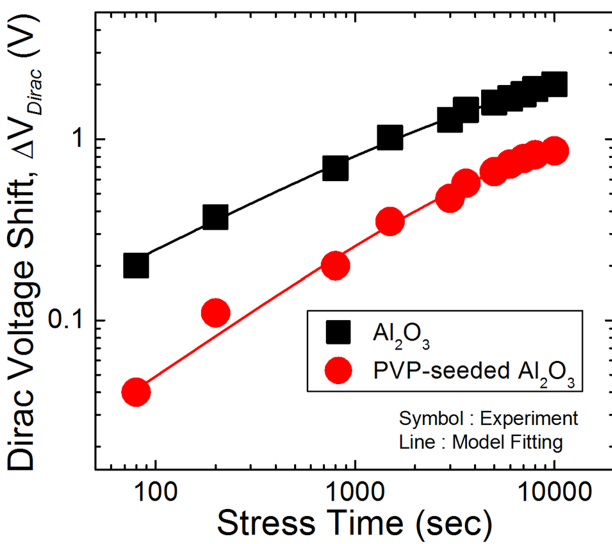

FIG. 5. The time-dependent V_{Dirac} shift of graphene FETs with the two different dielectrics. The experimental results were well fitted to the stretched exponential function. Determination coefficients (R^2) showing the quality of the fitting are close to unity. The device with PVP-seeded Al_2O_3 gate dielectric has a much smaller ΔV_{Dirac} (∞) (1.1 V) than that of the control device (2.7 V).

carrier mobility after the gate bias stress is almost the same as or even higher than that before gate bias stress. In order to quantify the time-dependent V_{Dirac} shift, we adopted the following stretched exponential function:

$$\Delta V_{Dirac}(t) = [V_{Dirac}(\infty) - V_{Dirac}(0)][1 - e^{-(t/\tau)^{\beta}}],$$

where V_{Dirac} (∞) is the Dirac voltage when equilibrium has been reached at $t = \infty$, V_{Dirac} (0) is the initial Dirac voltage at $t = 0$ s, τ is the characteristic time constant, and β is the stretched-exponential factor ($0 < \beta \leq 1$), indicating the width of the involved trap distribution.[19,20] As shown in Fig. 5, the time-dependent V_{Dirac} shift is well fitted with the stretched exponential function. The determination coefficients (R^2), a measure of the quality of the fit, were close to unity, indicating an excellent fit. From the ΔV_{Dirac} (∞) (V_{Dirac} (∞)-V_{Dirac} (0)) values, we observed that the device with the PVP seeding layer has a much smaller ΔV_{Dirac} (∞) (1.1 V) than that of the control device (2.7 V), demonstrating that the time-dependent V_{Dirac} shift of top-gate graphene FETs can be reduced by employing the seeding layer emebedded high-k gate dielectrics.

In summary, we have systematically investigated the ALD of a high-k dielectric on top of monolayer CVD graphene. While identical ALD conditions result in incomplete and rough dielectric films, the reactive groups provided by the PVP seeding layer yield conformal and pinhole-free dielectric films throughout the large-scale monolayer graphene. By utilizing the high-quality PVP-seeded Al_2O_3 gate dielectric, top-gate CVD graphene FETs with superior carrier mobility and reliability performance were achieved. We expect that these results can be used to enable large-scale graphene-dielectric integration, which is the major obstacle to future graphene nanoelectronics.

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[1]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[2]F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010).
[3]J. K. Park, S. M. Song, J. H. Mun, and B. J. Cho, Nano Lett. **11**, 5383 (2011).
[4]X. Wang, S. M. Tabakman, and H. Dai, J. Am. Chem. Soc. **130**, 8152 (2008).
[5]S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **94**, 062107 (2009).
[6]D. B. Farmer, H. Y. Chiu, Y. M. Lin, K. A. Jenkins, F. Xia, and P. Avouris, Nano Lett. **9**, 4474 (2009).
[7]B. Lee, G. Mordi, M. J. Kim, Y. J. Chabal, E. M. Vogel, R. M. Wallace, K. J. Cho, L. Colombo, and J. Kim, Appl. Phys. Lett. **97**, 043107 (2010).
[8]X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, Science **324**, 1312 (2009).
[9]T. Yoon, W. C. Shin, T. Y. Kim, J. H. Mun, T. S. Kim, and B. J. Cho, Nano Lett. **12**, 1448 (2012).
[10]W. C. Shin, H. Moon, S. Yoo, Y. Li, and B. J. Cho, IEEE Electron Device Lett. **31**, 1308 (2010).
[11]B. Lee, S.-Y. Park, H.-C. Kim, K. Cho, E. M. Vogel, M. J. Kim, R. M. Wallace, and J. Kim, Appl. Phys. Lett. **92**, 203102 (2008).
[12]Y. J. Shin, Y. Wang, H. Huang, G. Kalon, A. T. S. Wee, Z. Shen, C. S. Bhatia, and H. Yang, Langmuir **26**, 3798 (2010).
[13]A. Das, S. Pisana, B. Chakraborty, S. Piscanec, S. K. Saha, U. V. Waghmare, K. S. Novoselov, H. R. Krishnamurthy, A. K. Geim, A. C. Ferrari, and A. K. Sood, Nat. Nanotechnol. **3**, 210 (2008).
[14]W. C. Shin, S. Seo, and B. J. Cho, Appl. Phys. Lett. **98**, 153505 (2011).
[15]J. G. Oh, Y. Shin, W. C. Shin, O. Sul, and B. J. Cho, Appl. Phys. Lett. **99**, 193503 (2011).
[16]J. S. Moon, Carbon Lett. **13**, 17 (2012).
[17]O. M. Nayfeh, IEEE Trans. Electron Devices **58**, 2847 (2011).
[18]A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, IEEE Electron Device Lett. **32**, 1008 (2011).
[19]F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1992).
[20]H. Sirringhaus, Adv. Mater. **21**, 3859 (2009).

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