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Physical-gap-channel graphene field effect transistor with high on/off current ratio for digital logic applications

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We propose and analyze an approach to secure a high on/off current ratio in a graphene field effect transistor (FET) by introducing a physical gap along the channel rather than by attempting to open the energy bandgap of graphene. The device simulation results of the newly proposed device structure reveal highly suppressed off-state current of $\sim 10^{-9}$ A/μm, an on/off current ratio of more than seven orders of magnitude, and a subthreshold slope of 2.23 mV/decade more than a 20-fold reduction relative to the theoretical limitation of conventional metal-oxide-semiconductor FETs. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4756795]

Graphene field effect transistors (FETs) have been a subject of intense interest in recent years as researchers seek to replace current silicon based MOSFET technology. To date, most attempts to fabricate graphene FETs are based on a conventional metal-oxide-semiconductor FET (MOSFET) structure, with simple replacement of the channel material from silicon to graphene.[1,2] However, it must be noted that the current MOSFET structure has been designed and optimized for several decades for semiconducting materials, especially silicon, not for semimetal materials such as graphene. Therefore, simple replacement of the channel material in the conventional MOSFET structure necessitates efforts in opening the bandgap of graphene. Even though extensive efforts have been made to open up the energy bandgap of graphene,[3–11] it is found that the bandgap and carrier mobility are in a trade-off relationship in most materials.[1] Once the energy bandgap is opened in graphene, its original physical properties are altered and degradation of carrier mobility is unavoidable.[1,12,13] It is also unrealistic to attain a bandgap of larger than 0.4 eV, which is the minimum practical requirement for digital circuit applications.[1] Therefore, because graphene has a unique band structure that is substantially different from that of silicon, research on graphene transistors should take into consideration on device fundamentals, including device structure, rather than simply replacing the channel material and opening the bandgap.

In this perspective, various promising approaches, graphene nanoribbon tunnel graphene transistors,[14,15] bilayer pseudospin field effect transistors (BiSFET),[16] and Veselago lens switch,[17,18] exhibit promising results and strengthen the fundamentals of graphene FET. However, these devices require precise control of doping concentration or advanced fabrication technique for highly complex device, hindering the realization of graphene logic device.

In this work, we propose a device structure that does not require opening the bandgap of graphene and therefore can fully utilize the original unique properties of graphene. This device employs a physical-gap along the channel instead of opening graphene's energy bandgap, and is designed with

consideration of producibility and compatibility to conventional complementary-MOS (CMOS) process technology.

The physical-gap-channel graphene transistor is designed based on the impact-ionized MOS (IMOS) structure[19] and implemented on a silicon-on-insulator (SOI) substrate (Fig. 1). The channel is composed of a series connection of an ungated silicon region (physical gap) and a graphene/silicon hybrid channel upon which the gate dielectric and electrode are formed. The silicon body is almost intrinsic (very lightly p-doped), and the source is p$^+$ doped while the drain is n$^+$ doped. High-κ dielectric spacer is placed at the side of the gate stack. Nickel silicide is formed in the drain region for good ohmic contact, as is quite commonly employed in advanced CMOS devices.

The physical-gap-channel graphene transistor is designed on a SOI substrate that has a 20 nm thick silicon body. The lengths of the graphene/silicon hybrid channel and the physical gap are 100 and 80 nm, respectively. The physical thickness of the gate dielectric is 2 nm and the width of the high-κ spacer is 20 nm. Here, the dielectric constant of the high-κ spacer is assumed to be 40, which can be realized by using cubic structured La-doped HfO$_2$.[20,21] N$^+$ polysilicon is used for the gate electrode. The silicon body is very lightly doped with p-type dopant with a concentration of 1×10^{15} cm^{-3}. The source and drain are doped with p-type and n-type, respectively, with a doping concentration of 1×10^{20} cm^{-3}. The operation behavior and feasibility of

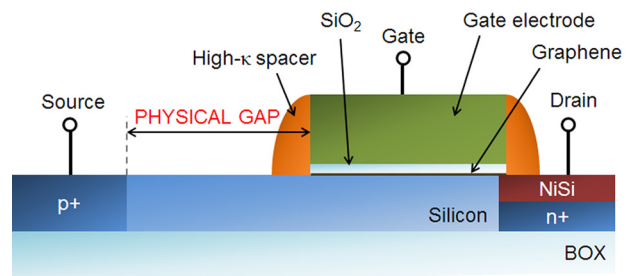FIG. 1. Illustration of the physical-gap-channel graphene transistor. The graphene channel under the gate is physically separated from the source edge. The source is p$^+$ doped, while the drain is n$^+$ doped. The silicon body is almost intrinsic. A high-κ spacer is used to induce a fringing electric field to the silicon surface.

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the devices are analyzed using commercial device simulation software, Technology Computer-Aided Design (TCAD), Silvaco.[19,22] Prior to the analysis of the proposed structure, the characteristics of a graphene back gate FET structure are analyzed to verify the suitability of the simulation tool for modeling the graphene transistor, because there is no physical model of graphene for a computer simulation in the commercial device simulator. In our simulation, the graphene is defined as a zero bandgap general semiconductor with a physical thickness of 1 nm, a work function of 4.5 eV, intrinsic carrier density of 2×10^{11} /cm^2, and both hole and electron mobilities of $10\,000$ cm^2/V·s.[23–26] The simulation results of the back gate graphene FET with a 100 nm thick gate dielectric reveal typical characteristics of a graphene FET, including ambipolar conduction (Fig. 2(a)), zero bandgap, high mobility (Fig. 2(b)), and linear output characteristics (Fig. 2(c)), thus indicating that we can use this model for simulation of the physical-gap-channel graphene transistor.[23–28]

The basic operation principle of the proposed graphene transistor is depicted in Fig. 3. When a negative bias is applied to the gate, the graphene under the gate becomes p-type. However, because of the presence of the physical gap along the channel, the device remains in an off-state and the drain current is limited by the reverse saturation current of the p-i-n junction. When the gate voltage is positive, the graphene becomes n-type. As the gate voltage is increased further, an electron inversion layer is formed underneath the high-κ spacer by a fringing field. The surface regions from the drain to the edge of the high-κ spacer in the physical gap region are then electrically connected. The formation of the electron inversion layer under the high-κ spacer results in reduction of the effective length of the physical gap, causing an increase of the lateral electric field in this region (Fig. 3(b)). With higher gate voltage, the resistance between the drain and the edge of the high-κ spacer in the physical gap

region drops further, and then the lateral electric field in the physical gap is further enhanced at a given drain bias. This process eventually ignites the impact ionization in the physical gap region and electrons are injected from the valence band of the p$^+$ source into the physical gap region and thereby the device is turned on. It is known that the work function of graphene is around 4.5 eV. Then, the Fermi level of graphene is located within the bandgap of silicon as shown in Fig. 3(e). At the edge of the graphene channel region (near high-K spacer), the electrons in the silicon inversion region under high-K spacer region will flow to graphene due to the band offset between silicon conduction band and graphene, making it possible to fully exploit the high electron mobility of the graphene layer. As the switching of this device is controlled by the fringing field at the edge of the physical gap, the switching operation of this graphene FET is insensitive to the Dirac voltage and the initial doping concentration of graphene, which are almost uncontrollable quantities in conventional graphene FETs.[29–31] The engineered nickel silicide, which has a work function of 4.5 eV, helps provide barrier-less conduction of electrons from graphene to the drain electrode. The engineered nickel silicide, which has a work function of 4.5 eV, helps provide barrier-less conduction of electrons from graphene to the drain electrode. The drain biases used in this simulation are rather large, because the device requires avalanche breakdown in the physical gap region. However, several solutions are already suggested to address this issue, such as channel length scaling,[32] utilizing new material with high impact ionization coefficient,[33] introducing strain,[34] and so on.

The calculated I-V characteristics of the proposed device are shown in Fig. 4. The physical dimension of the gated graphene channel length is fixed at 100 nm. A conventional n-channel silicon MOS device with the same gate channel length and a similar threshold voltage is simulated together for comparison. The graphene channel device shows
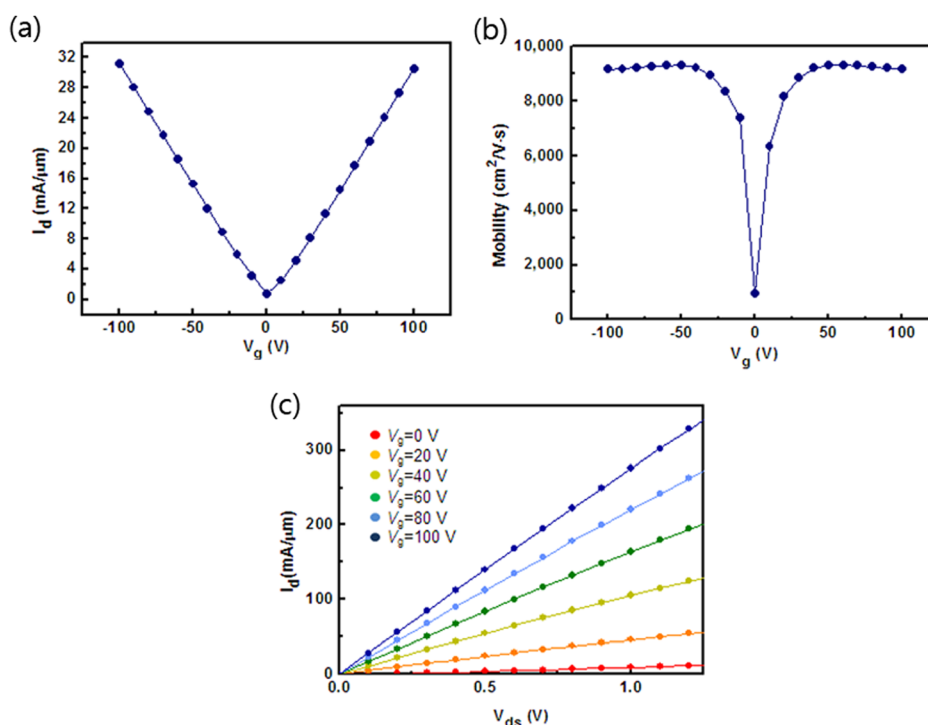

FIG. 2. The simulation result of the back gate graphene FET with a 100 nm thick gate dielectric. The graphene is defined as a zero bandgap general semiconductor with a physical thickness of 1 nm. (a) I_d-V_g characteristics show ambipolar transport and a low on/off ratio. (b) Carrier mobility calculated from the I_d-V_g curve by Drude model. (c) I_d-V_d characteristics of the graphene transistor.
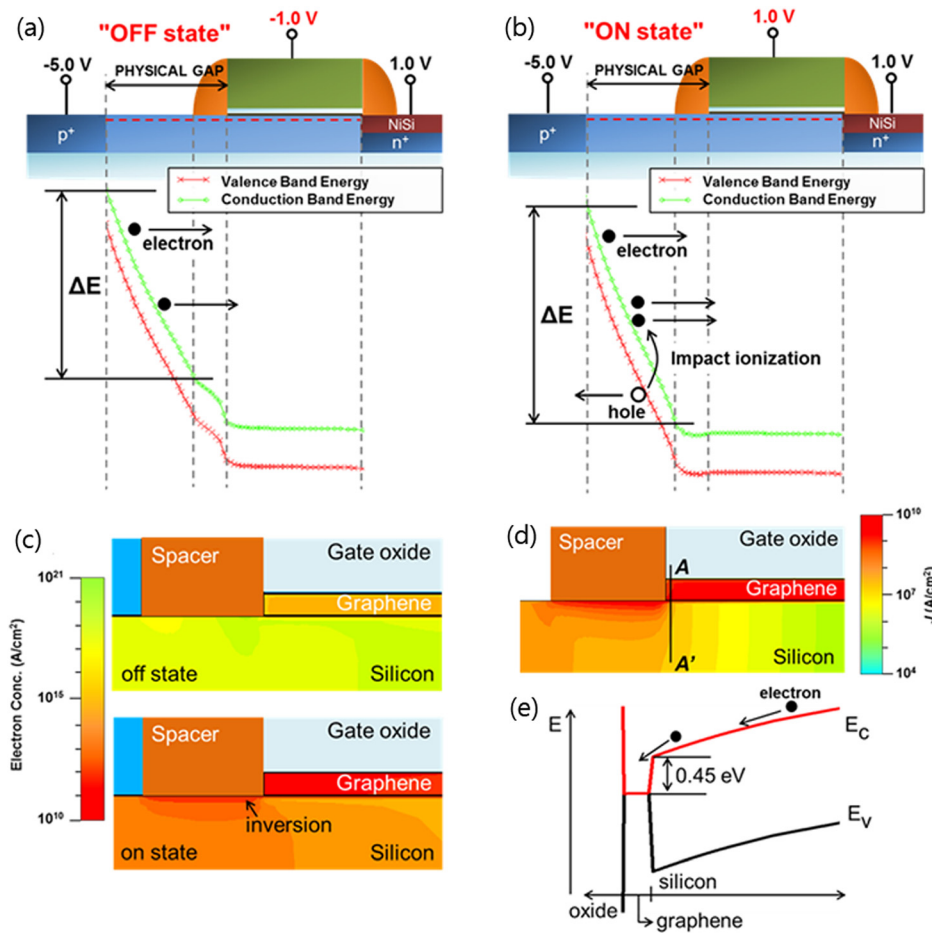
FIG. 3. Operating bias conditions of the proposed device and corresponding energy band diagrams along the channel. (a) Band diagram in off state. $V_{ds} = 6.0$ V and $V_g = -1$ V. The energy band of silicon underneath the high-κ spacer region is pulled up by negative gate bias. (b) In the on state, the energy band of silicon underneath the spacer region is pushed down, resulting in an increase of the lateral electric field in the physical gap region. This causes ignition of impact ionization, causing the device to turn on. (c) Current density distribution in channel area. In the on state ($V_g = 1.0$ V, $V_d = 1.0$ V, and $V_s = -5.0$ V), almost all electrons flow through the graphene rather than through the silicon.

ten times higher on-state current compared to the conventional MOS device (Figs. 4(a) and 4(b)). More importantly, the proposed graphene device shows excellent switching performance with an on/off current ratio of seven orders of magnitude, which is well within the acceptable range for modern digital logic circuits (Fig. 4(b)). In addition, the graphene de-

vice exhibits a subthreshold slope of 2.23 mV/dec, constituting more than a 20-fold reduction from the theoretical limitation of conventional MOS devices (~60 mV/dec). This sudden switching behavior originates from the feature that the conduction is ignited by impact ionization in the physical gap region. However, the V_d-I_d characteristic (Fig. 4(c))
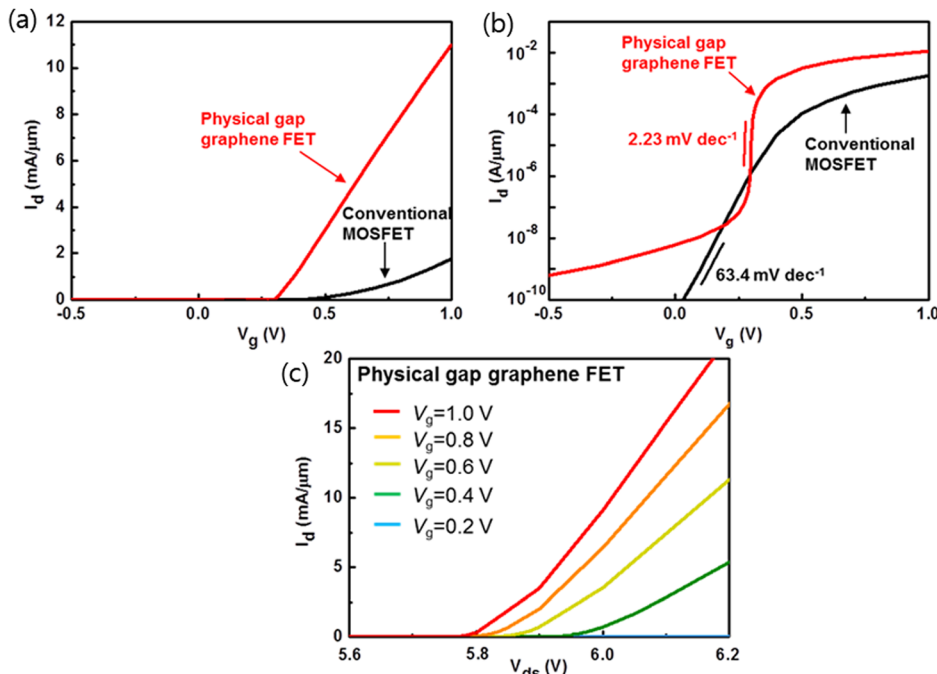

FIG. 4. Transfer characteristics and device performance. (a) Linear-linear plot of I_d-V_g curve. (b) Log-linear plot of I_d-V_g curve. The physical-gap-channel graphene FET shows significantly suppressed off-state current and an ultra-steep subthreshold slope of 2.23 mV/dec. The characteristics of a conventional MOSFET that has the same channel length are plotted together for comparison. (c) The I_d-V_d characteristics of the graphene FET show a narrow operation window and small output resistance.

shows that the physical-gap-channel graphene device has low output resistance and a narrow operation voltage window, thus necessitating further optimization of the device structure in future research. And, it should be noted that the model which we used in this simulation does not include the physical limitation of current capacity of graphene and heating effect. Therefore, the current levels at further higher drain biases may be lower in actual devices.

In conclusion, significant suppression of the off-state current in the physical-gap-channel graphene transistor enables an on/off current ratio of seven orders of magnitude, the highest value that has been achieved to date in a graphene channel transistor. Excellent device performance including an extremely steep subthreshold slope and high on-state current is obtained through the innovative device structure. The proposed device utilizes the conventional CMOS process technology and therefore application of graphene channel FETs to digital logic devices is expected to become more realistic in the near future.

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