A GENERAL CIRCUIT TOPOLOGY OF MULTILEVEL INVERTER

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ABSTRACT

A generalized circuit topology of multilevel voltage source inverter is proposed, which is based on a direct extension of the three-level inverter to higher level, and the circuit topologies up to five-level are presented. The proposed multilevel inverter can realize any multilevel pulsewidth modulation(PWM) scheme which leads to harmonic reduction and provides full utilization of semiconductor devices like GTOs especially in high power range where high voltage could be applied. Capacitor voltage balancing problem is pointed out and a circuit remedy for such a problem is also given.

I. Introduction

In general, increasing the switching frequency in voltage source inverters(VSI) leads to the better output voltage/current waveforms. Harmonic reduction in controlling a VSI with variable amplitude and frequency of the output voltage is of importance and thus the conventional inverters which are referred to as two-level inverters have required increased switching frequency along with various PWM switching strategies. In the case of high power/high voltage applications, however, the two-level inverters have some limitations to operate at high frequency mainly due to switching losses and constraints of device rating itself. Moreover, the semiconductor switching devices should be used in such a manner as problematic series/parallel combinations to obtain capability of handling high power.

Nowadays the use of multilevel approach is believed to be promising alternative in such a very high power conversion processing as pointed out in literatures [1,2]. In addition, some switching strategy has been developed in accordance with the newly emerged circuit topologies, for example, neutral point clamped inverter which is intuitively a three-level inverter [3,4]. Recently, a work to extend such three-level switching strategy to that of higher level above three-level has been reported [5]. The improvement in the harmonic contents owing to the increased number of levels could be followed as expected.

But the actual generalized structure to achieve such features seems to be somewhat questionable especially at the level above three. So far, a few multilevel structures were presented [1,6]. The multilevel structure presented in [6] is made up of series connected full-bridge bipolar inverters and thus it can be seen as a combination of two-level inverters requiring coupling components such as transformer. Thus, it becomes bulky and heavy along with complexity of structure. On the other hand, the generalized topology in [1] exhibits a very simple structure, that is, a direct realization of multilevel concept with bidirectional switches consisting of two thyristors. In such configuration, however, the semiconductor switches may have the different voltage stress with each other and a switch connected to most upper/lower voltage levels should undergo stress of dc-link voltage. Hence, it has limitation in increasing handling power especially when input voltage is very high.

In this paper a general circuit topology of multilevel VSI is proposed which is based on a direct extension of the three-level

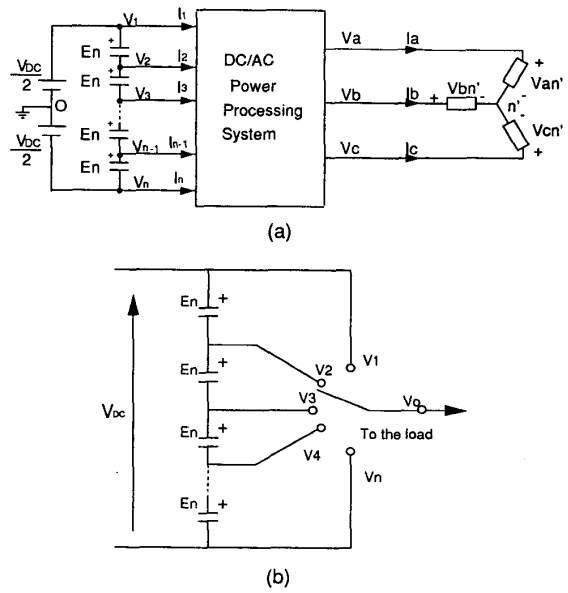

Fig. 1 (a) Three phase multilevel power processing system, (b) Schematic of single pole of multilevel inverter by a switch.

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inverter to higher level and the circuit topologies up to five-level are presented. The circuit topology provides full utilization of semiconductor devices like GTOs where voltage stress of each switch is limited to certain lower value than dc-link voltage whereby increased handling power capability of the inverter. Moreover, the switching configurations related to the inverter result in actually decreased switching frequency at each switching device with the same/better output waveform quality as that of conventional two-level structure. Of course, the proposed multilevel inverter can realize any multilevel PWM scheme which leads to harmonic content reduction.

Primarily, we assume that the dc-link voltages across each series connected capacitor tank would be voltage sources and whereby the basic principle of the inverter is presented. Then, the voltage balancing problem of each capacitor voltage is described and some circuit techniques for solving such a problem are given.

II. General Topology of Multilevel Inverter

A. MULTILEVEL CONCEPT

Fig. 1(a) illustrates a schematic of DC to AC power conversion system employing three-phase multilevel VSI where V_{DC} indicates dc-link voltage obtained from any equipment which can yield stable dc source. Series connected capacitors constitute energy tank for the inverter providing some nodes to which multilevel inverter can be connected. Primarily, the series connected capacitors will be assumed to be any voltage sources of the same value. Each capacitor voltage E_n is given by

$$E_n = \frac{V_{DC}}{n-1} \tag{1}$$

where n denotes the number of levels adopted.

The term so called level in the configuration can be referred to the number of nodes to which the inverter can be accessible as shown in Fig. 1(a).

Output phase voltages will be defined as voltages across output terminals of the inverter and the ground point denoted by o in Fig. 1(a). Moreover, input node voltages and currents will be referred to input terminal voltages of the inverter with reference to ground point and the corresponding currents through branches from each nodes of dc-link capacitors to the inverter, respectively. For example, input node voltages are designated by V_1, V_2 etc and input node currents by I_1, I_2 etc as seen in Fig. 1(a).

Fig. 1(b) shows the schematic of a pole in multilevel VSIs where V_o indicates an output phase voltage. The output phase voltage can assume any voltage level by selection of each node V_1, V_2 etc. Thus, a pole in multilevel VSI could be regarded as a single-pole-multiple-throw switch.

In the context of actual realization, selection of each input node voltage may imply , for example, to be achieved by any bidirectional switching devices. Obviously, such direct realization may result in relatively many semiconductor devices employed as well as excessive switching stress of full dc-link voltage and thus practically of little usefulness. In other words, the topological structure of multilevel inverter suggested must cope with the following points. 1) It should have less switching devices as far as possible. 2) It should be capable of enduring very high input voltage such as HVDC transmission for high power applications. 3) Each switching device should have lower switching frequency owing to multilevel approach.

B. CIRCUIT TOPOLOGY PROPOSED

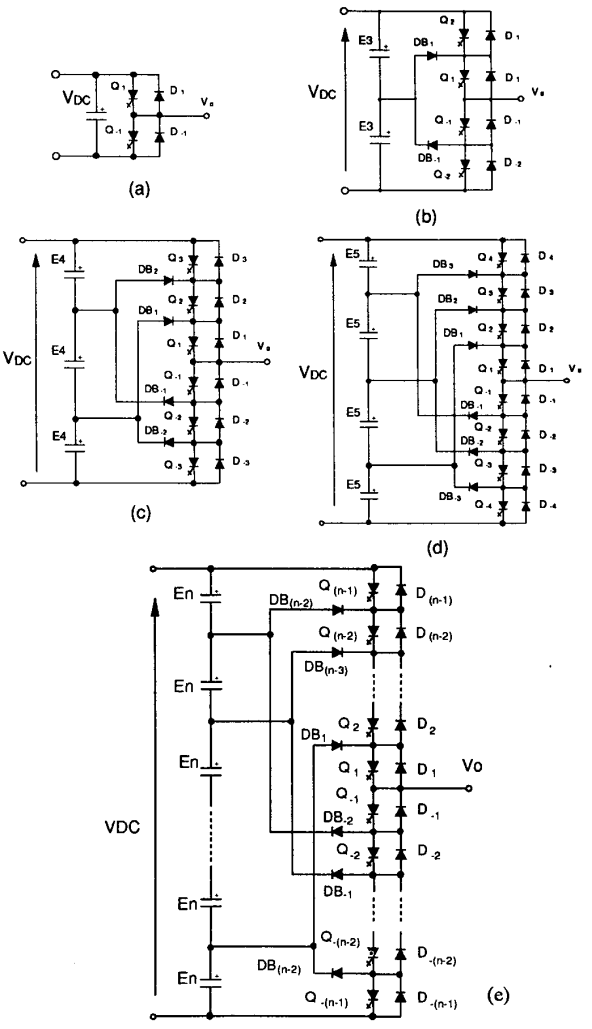

Fig. 2 Proposed general multilevel topology: a pole of (a) two-level, (b) three-level, (c) four-level, (d) five-level, (e) n-level inverter.

V_o	V_1	V_2	V_3	···	$V_{(n-1)}$	V_n
$Q_{(n-1)}$	1	0	0	···	0	0
$Q_{(n-2)}$	1	1	0	···	0	0
$Q_{(n-3)}$	1	1	1	···	0	0
·	·	·	·	·	·	·
Q_2	1	1	1	···	0	0
Q_1	1	1	1	···	1	0
Q_{-1}	0	1	1	···	1	1
Q_{-2}	0	0	1	···	1	1
·	·	·	·	·	·	·
$Q_{-(n-3)}$	0	0	0	···	1	1
$Q_{-(n-2)}$	0	0	0	···	1	1
$Q_{-(n-1)}$	0	0	0	···	0	1

ON = 1, OFF = 0

Table 1 Switching table for n-level VSI stresses of each device.

The actual circuit topologies of multilevel inverters up to arbitrary level are presented in Fig. 2, which shows only a pole construction. As well known, the conventional VSI has adopted a pole of two-level type as seen in Fig. 2(a) and also the neutral point clamped inverter takes that of three-level seen in Fig. 2(b). The bidirectional current flow can be achieved by both a set of series connected semiconductor switches turning on and either diodes parallel with such active switches or two branch diodes which are directly connected to an accessible node of series connected capacitor tank. Such branch diodes are denoted by DB_m, $(m = -(n-2),\cdots,-1,1,\cdots,(n-2))$, and distinguished from main diodes, D_m, $(m = -(n-1),\cdots,-1,1,\cdots,(n-1))$, as seen in Fig. 2(e). In addition, the series connected switches such as Q_m, $(m = -(n-1),\cdots,-1,1,\cdots,(n-1))$ will be referred to as main switches.

Table 1 shows the fundamental switching table for our multilevel inverters where V_o indicates an output phase voltage (See Fig.1(b)). Note that, in Table 1, some series connected $(n-1)$ switches are in on-state and the rest in off-state so that a set of such series connected main switches in on-state and some additional diodes which vary according to voltage level selection play a role of an equivalent bidirectional switch conceptually pictured in Fig. 1(b). Fig. 3 illustrates bidirectional current flow path, for example, of the four-level inverter for each node selection. It should be noted that main diodes conduct only in the case that the most upper/lower voltage level is selected. This implies that main diodes may have much lower rms current rating than that of main switches while having the same voltage rating as that of main switches. In Fig. 3, two branch diodes are related to nodes from which we want to draw output phase voltage, except the most upper/lower node. Moreover, the number of switches turning on for selection of any input node voltage are always equal to $(n-1)$ regardless of switching status except during transient dead time.

It is worthy to note that if the pole of inverters in Fig. 2 is controlled in such a way as to avoid sudden change of $2E_n$ or more, there is no need to turn off two or more switches simultaneously while turning on the other two or more, and vice versa (refer to Table 1). It is pointed out that such switching strategy, in turn, leads to decrease in switching frequency at each switching device with the same output waveform quality as conventional two-level type and it will be investigated with an example in the subsequent section.

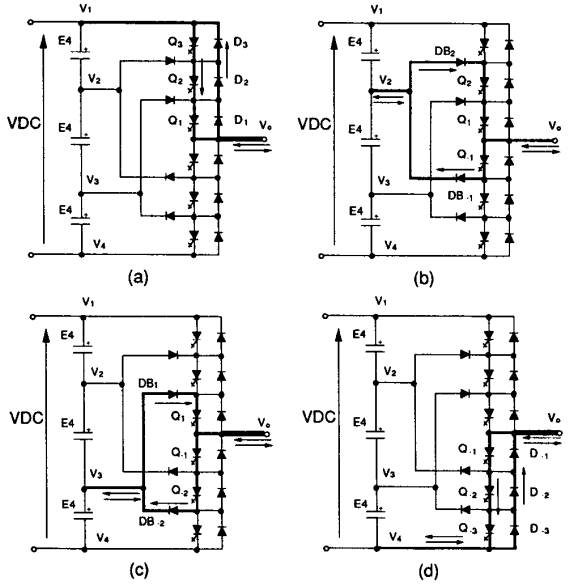

Fig. 3 Bidirectional current flow path of the four-level inverter for each output voltage level: selection of (a) V1, (b) V2, (c) V3, (d) V4.

Of course, it is possible to change output phase voltage by the amount of each values of multiple of E_n. In such case, the number of commutated switches, N_c, will be given by

$$N_c = 2(n_2 - n_1) \tag{2}$$

assuming output phase voltage changing from V_{n_2} to V_{n_1} and vice versa. For instance, confining the only extreme changes of output phase voltage, i.e. selection of V_1 and V_n alternatively, any multilevel inverter of n-level goes to conventional two-level VSI in practice, resulting in $2(n-1)$ commutations whenever switching state transition occurs.

In very high power applications especially with very high input voltage, traditional two-level VSIs could not avoid to use the series connected semiconductor switches so as to cope with limitations of device rating utilized and it may be very cumbersome and even problematic mainly due to the difficulty of device matching deteriorating utilization factor of switching devices. Our multilevel topology, however, suggests a good solution for such a problem. In any possible switching states shown in Table 1, each semiconductor device is to be block at most a voltage equal to E_n so that it may have lower voltage rating with the same power output as that of conventional VSI. Hence, the circuit topologies shown in Fig. 2 might be preferred not only under the aspect of harmonic content reduction due to several level of the output voltage as an essential feature of multilevel scheme, but also under the aspect of full utilization of semiconductor device in case that high voltage of dc-link could be applied.

The multilevel inverter in Fig. 2(e) has very simple commutation sequence which could make it possible to freely change output phase voltages between arbitrary two voltage levels, requiring no additional commutation circuitry. Commutation procedure between some levels should be divided into each one-level commutation of unit change of voltage E_n in order to guarantee voltage stress of both main switches and main diodes within unit level voltage E_n during transient time. One-level commutation can be carried out by first turning off the most upper(lower) main switch in on-state and turning on the opposite lower(upper) main switch in off-state after a required dead time. It should be noted that such commutation sequence facilitates utilization of switching devices even with different turn off times.

III. Control of Multilevel Inverter

Recently, a work to extend what we called subharmonic PWM method in two-level to that of higher level has been reported where the multilevel modulation processes are analyzed and the expressions of the output phase voltages of the inverter are mathematically drawn along with existence of actual structure of the multilevel VSI [5]. In our paper, such a subharmonic PWM in a multilevel inverter is actually applied to our multilevel topology, especially for half-bridge five-level inverter whereby some structural features in our topology such as rms current ratings of each device component and switching frequency at each switching device are investigated varying modulation index and load condition.

A. HALF-BRIDGE FIVE-LEVEL INVERTER

Half-bridge five-level inverter drawn from the general topology in Fig. 2(e) is presented in Fig. 4 where V_o and I_o indicate a load voltage and current respectively. We assume that there is

enough inductance associated with the output load, i.e., perfect filtering at load side to yield a purely sinusoidal output current. Under the assumption, the output current, I_o, with a maximum value of I_{max} can be expressed as

$$I_o = I_{max}\sin(\theta - \beta) \tag{3}$$

where β represent phase lag in radian related to power factor, pf, of the load, i.e., $pf = \cos\beta$. Also, to assure strict five-level operation, it is assumed that each capacitor voltage should be the same and equal to E_5 allowing some additional circuitry or the other technique pertinent to regulate the voltage.

Fig. 5 shows a typical current waveform observed at each main switch when employing simple stepped control of output phase voltage where power factor of 0.8 assumed (see Fig. 5(a)). Note that, in Fig. 6, the most inner switches such as Q_1 and Q_{-1} support more current than the most outer switches such as Q_4 and Q_{-4}.

For the application of fixed frequency and fixed voltage such as utility power processing, higher level inverter above five-level may be adopted because the increased level of the inverter is not only capable of enduring high input voltage but also capable of yielding good waveform quality with lower harmonic contents intuitively.

B. SUBHARMONIC PWM FOR FIVE-LEVEL INVERTER

Fig. 6 illustrates a subharmonic PWM technique for any five-level inverter, which employs four triangular carrier signals and a modulating sinusoidal signal. All of the carriers have the same frequency f_c and the same amplitude of peak-to-peak A_c while the modulating signal is a sinusoid of frequency f_m and amplitude A_m. As seen in Fig. 6(a) the carriers are so deposed that they are contiguous with each other and alternatively in opposition. Some another methods of carrier deposition are presented in [5]. we selectively take one among the methods for simplicity of examination of our inverter topology. It is believed that any multilevel PWM with only minor difference such as carrier phase would to some extend result in similar characteristics.

At every instant each carrier is compared with the modulating signal producing the corresponding decision signals such as S_1, S_2, S_3, and S_4 where the value of $+1(-1)$ represents that the modulating sinusoid is greater(less) than the triangular under comparision. Then all the decision signals are summed up to yield a control signal S_l where the pattern resembles the output phase voltage of the inverter. Strictly speaking, however, the control signal S_l gives only some information to control any five level inverter and thus the actual switch driving signals are completely dependent on the particular structure and can be drawn from the control signal S_l. Thus, the scaling of S_l may be of no importance.

As traditional subharmonic PWM, the subharmonic PWM for the five-level inverter has two parameters related in modulation process: one is frequency ratio M_f which is given by

$$M_f = \frac{f_c}{f_m} \tag{4}$$

and the other modulation index M_i which is defined by

$$M_i = \frac{A_m}{2A_c} \tag{5}$$

for the case of five-level modulation. Varying modulation index with any fixed frequency ratio enables voltage control of the five-level inverter, including the overmodulation which gives fundamental amplitude up to $4/\pi$ p.u. effectively resulting in what so called two-level action of the five-level inverter.

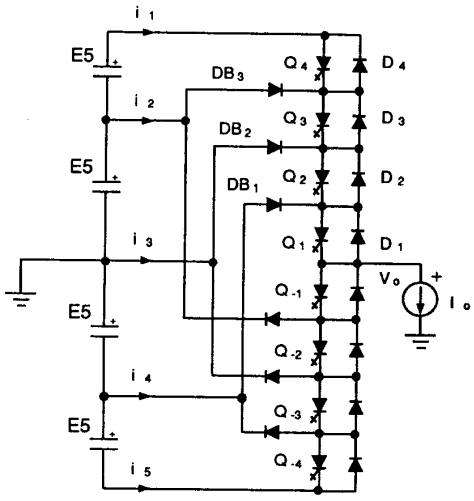

Fig. 4 Half bridge five-level inverter.

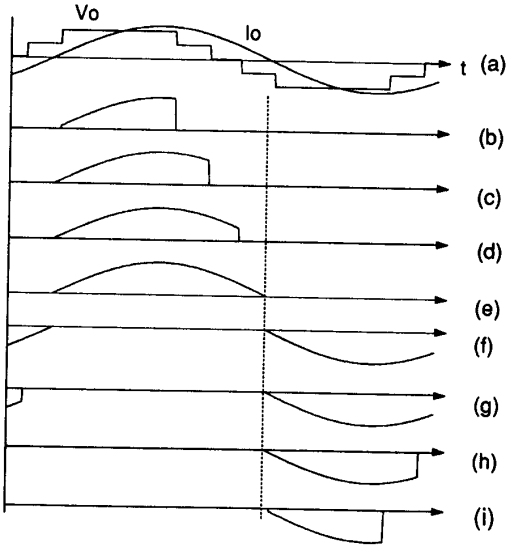

Fig. 5 Simple stepped control of half-bridge 5-level inverter: (a) Vo and Io, (b) i_{Q_4}, (c) i_{Q_3}, (d) i_{Q_2}, (e) i_{Q_1}, (f) $i_{Q_{-1}}$, (g) $i_{Q_{-2}}$, (h) $i_{Q_{-3}}$, (i) $i_{Q_{-4}}$.

IV. Utilization of Semiconductor Device

Multilevel inverters, in general, employ relatively many semiconductor devices due to their distinct structure so that it would be seen at glance to be less attractive. However, it is reasonable that the real evaluation of such an inverter should be primarily in the context of device utilization. In some inverter structures such as direct realization with bidirectional switches, the device utilization may be poor resulting in high voltage and/or current stress at the device. But our multilevel inverters make it possible to utilize their semiconductor devices fully allowing low devices ratings.

In this section, some properties associated with semiconductor devices of use are investigated in order to evaluate our multilevel inverter topology. Starting with the half-bridge five-level inverter

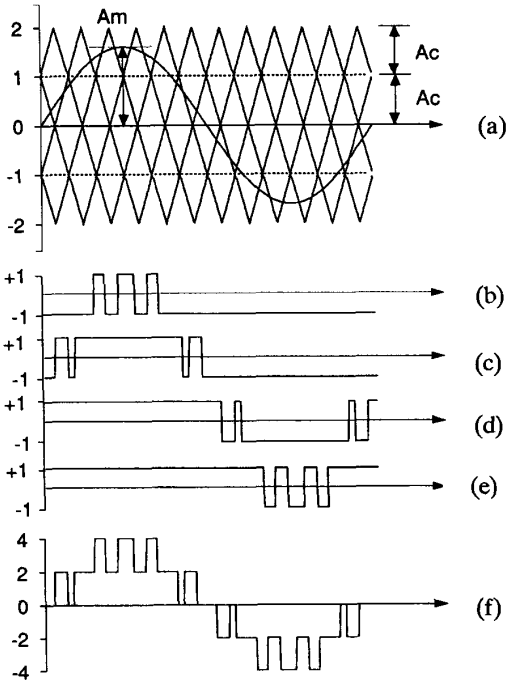

Fig. 6 A subharmonic PWM of a five-level inverter: (a) modulating signal and carriers, (b) S_1, (c) S_2, (d) S_3, (e) S_4, (f) S_I.

(see Fig. 4) with the aforementioned subharmonic PWM control, firstly, rms currents through each semiconductor devices are estimated and plotted by digital simulation which may give some guidelines selecting device ratings. Then switching frequencies at each main switches are considered with the subharmonic PWM control clarifying advantages of our five-level inverter.

A. RMS CURRENT

Each input node current can be expressed with well-known switching function method as follows (refer to Fig. 4):

$$i_n = SF_n \cdot I_o \qquad n = 1,2,\cdots,5 \tag{6}$$

where SF_n indicates switching function associated with selection of the corresponding input node voltage V_n shown in Fig. 1(b). That is,

$$SF_n = \begin{cases} 1 & \text{if } V_o = V_n \\ 0 & \text{if } V_o \neq V_n \end{cases} . \tag{7}$$

Referring to Fig. 1(b), since the single-pole multiple-throw switch as a general model of multilevel inverter is always connected to one and only one input node at every instant, the output load current could be drawn from one and only one input node. Thus,

$$I_o = i_1 + i_2 + i_3 + i_4 + i_5 \tag{8}$$

and the rms value of each current is expressed as follows

$$I_{o\,(rms)}{}^2 = \sum_{n=1}^{5} I_{n\,(rms)}{}^2 \tag{9}$$

where

$$i_{n\,(rms)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} SF_n \cdot I_o{}^2 d\theta} \qquad n = 1,2,\cdots,5 \tag{10}$$

Assuming balanced switching with reference to ground level, we obtain

$$i_{1\,(rms)}{}^2 = i_{5\,(rms)}{}^2, \quad i_{2\,(rms)}{}^2 = i_{4\,(rms)}{}^2 \tag{11}$$

If the five-level inverter have the voltage control by means of subharmonic PWM, rms input node current can be derived from both the corresponding switching function and the output current as given by Eq. (10).

Each rms current through the main switches of the five-level inverter is shown in Fig. 7 as increasing output phase voltage at each specified power factor. Remember that by structural symmetry and balanced control, currents through the opposite switches such as $Q_{-1},..,Q_{-4}$ also have the same rms evaluation as $Q_1,..,Q_4$, respectively.

Note that variations in rms value at each main switch exhibit distinctive features. Until overmodulation occurs, the rms currents through the inner main switches, Q_1, Q_2 are almost the same as 0.707 P.U. and relatively constant with about 10% variations regardless of load condition (see Fig. 7(a),(b)). On the other hand, the rms values of current through the outer main switches, Q_3, Q_4 show lower current sharing than Q_1, Q_2 allowing relatively large variations according to each load condition. If we confine the operating range of the inverter up to M_i of 1, the most outer main switches have lower current rating than the most inner ones which have the same current rating of 0.707 P.U. as that of conventional VSI. We can say that in very high power conversion especially employing the multilevel inverter, it may be preferred to keep the inverter from operating at the condition of such large/full modulation for the purpose of preserving advantages of the multilevel approach such as the utilization of several input node voltages.

Fig. 8 shows the rms current through main diodes. It should be note that all the main diodes have not only the same current rating but also much lower value of the rms current through them than that of any main switches. For example, with the load of 0.25 power factor, relatively worst case, the rms value of a main diode are at least 0.3p.u. at full modulation (see Fig. 8). This is because the main diodes of one side have opportunity to conduct only when the most upper or lower voltage level is selected as seen in Fig. 3.

Fig. 9 shows the rms current through the branch diodes Note that DB_1 may have the rms current rating of one half of that of DB_2 or DB_3. The device stress of each semiconductor device can be summerized for the half-bridge five level inverter as shown in Table 2, where lower voltage stress and lower rms current stress could be observed.

B. SWITCHING FREQUENCY

In this section, the number of commutations at each main switch is considered supposing that the half-bridge five-level inverter is under control of the subharmonic PWM. Obviously the number of total commutations per cycle in the five-level inverter is dependent on the modulation index since overmodulation drops some modulated pulses. One intersection of modulating sinusoidal with any carrier (see Fig. 6) results in two commutations in the inverter : one is on-going while the other is off-going. Thus, the frequency ratio M_f provides $2M_f$ commutations per fundamental cycle unless overmodulation occurs.

Fig. 10 shows the number of commutations per cycle at each switching device varying the modulation index with some frequency ratios of 12 and 36. It should be noted that no commutation in Q_1 and Q_4 (similarly, in Q_{-1} and Q_{-4}) occurs until modulation index reaches 0.5 and thus power processing is covered by switching action of the rest four switches. That is, both the most inner switches and the most outer switches maintain on or off states in

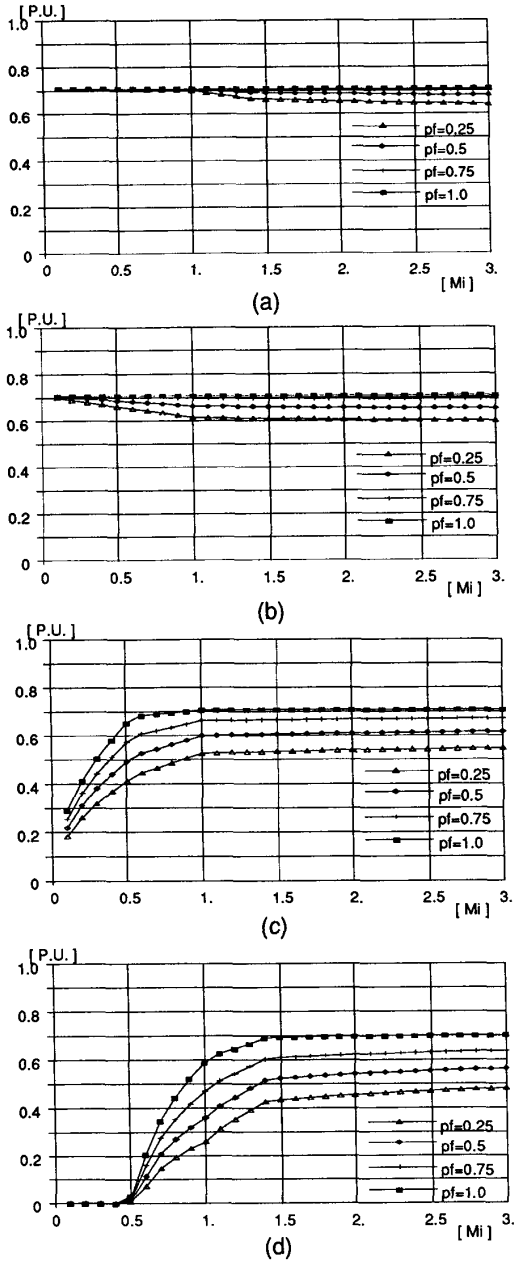

Fig. 7 RMS current variation of main switch: (a) Q_1, (b) Q_2, (c) Q_3, (d) Q_4

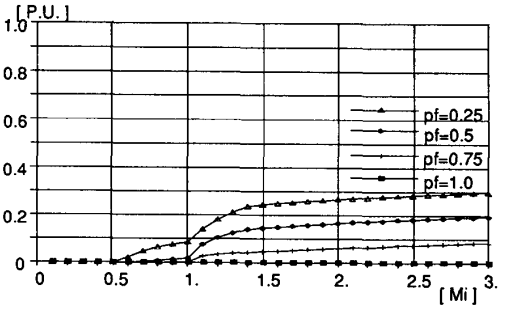

Fig. 8 RMS current variation of main diodes.

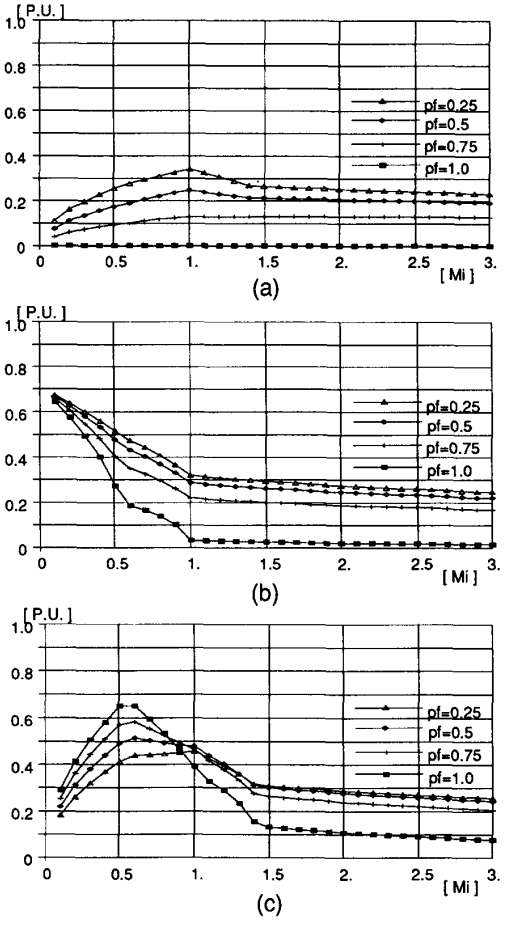

Fig. 9 RMS current variation of branch diode: (a) DB_1, (b) DB_2, (c) DB_3

the case of small modulation. Then, when middle modulation initiates, the switches awake and become active taking over some opportunity of switching action.

It is worthy to note that in any case of modulation index up to 1.0, the number of total commutations per cycle is fixed and the total commutations are distributed at each switching device. Such property allows switching frequency reduction at real switching device maintaining the total number of switchings constant. In addition, when deep modulation occurs to yield maximum power, our multilevel inverter has uniform distribution of commutations to all of the switches, i.e., 2 commutations per switch per cycle.

V. DC-Link Capacitor Voltage Balancing

The voltage balancing of capacitors acting as energy tank is very important in order for the multilevel inverter to work well. The capacitor voltage balancing problem is meant by the fact that

Table 2 Semiconductor device voltage and current stresses of each device.

Device	V_{peak}	I_{peak}	I_{rms}*	I_{rms}**
Q_4	0.25 p.u.	1.0 p.u.	0.707 p.u.	0.589 p.u.
Q_3	0.25 p.u.	1.0 p.u.	0.707 p.u.	0.706 p.u.
Q_2	0.25 p.u.	1.0 p.u.	0.707 p.u.	0.707 p.u.
Q_1	0.25 p.u.	1.0 p.u.	0.707 p.u.	0.707 p.u.
D_1~D_4	0.25 p.u.	1.0 p.u.	0.3 p.u.	0.086 p.u.
DB_3	0.25 p.u.	1.0 p.u.	0.65 p.u.	0.65 p.u.
DB_2	0.5 p.u.	1.0 p.u.	0.67 p.u.	0.67 p.u.
DB_1	0.75 p.u.	1.0 p.u.	0.34 p.u.	0.34 p.u.

(*) ranged to full modulation.
(**) with no overmodulation.

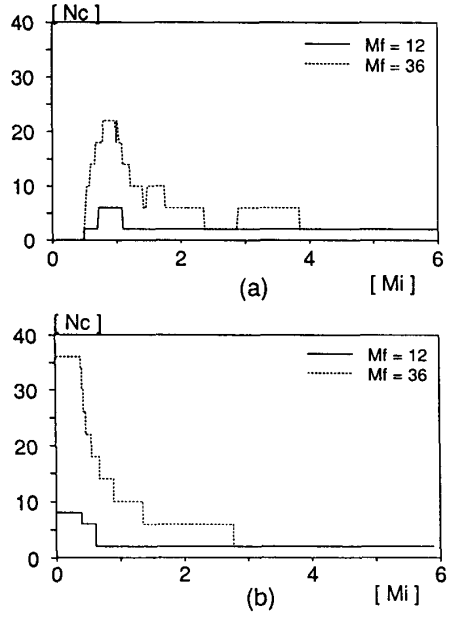

Fig. 10 The number of commutations at each switching device: (a) Q_4, Q_1, Q_{-1}, Q_{-4}, (b) Q_3, Q_2, Q_{-2}, Q_{-3}..

when establishing sinusoidal output waveform, charge of inner capacitors nodes of which are connected to the others can flow out more than that of outer capacitors which are directly connected to dc-link bus.

To describe capacitor charge balancing problem, the half-bridge five-level inverter is again used supposing simple stepped voltage control. In Fig. 11, (a) illustrates schematic of such a five-level inverter and (b) is the resultant stepped output phase voltage and sine output current allowing some power factor pf = cosβ and arbitrary control angles α_1, α_2.

Thus, the average value of input node current i_1, $I_{1(avg)}$, is given by

$$I_{1(avg)} = \frac{1}{2\pi}\int_{\alpha_2}^{\pi-\alpha_2} I_o \, d\theta$$

$$= \frac{1}{2\pi}\int_{\alpha_2}^{\pi-\alpha_2} I_{max}\sin(\theta-\beta)\, d\theta$$

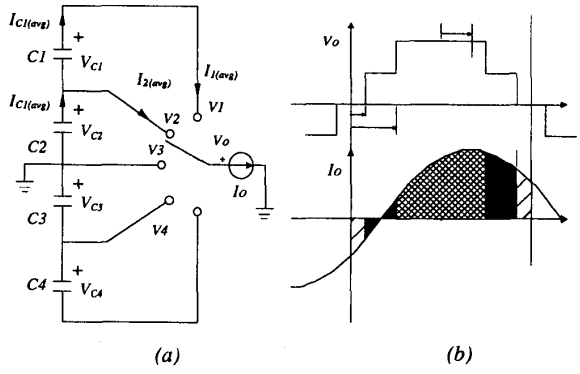

Fig. 11 (a) Schematic of half bridge five-level inverter, (b) distribution of output load currents.

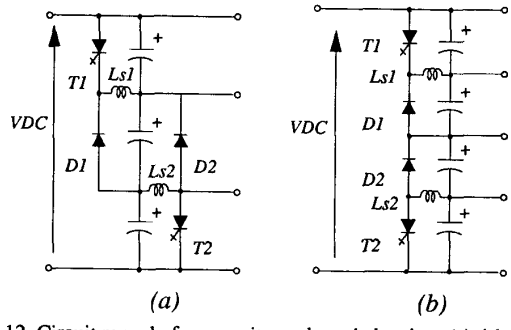

Fig. 12 Circuit remedy for capacitor voltage balancing: (a) 4-level case, (b) 5-level case.

$$= \frac{I_{max}}{\pi}\cos\beta\cos\alpha_2 \quad . \tag{12}$$

Similary, the average value of i_2, $I_{2(avg)}$, is given by

$$I_{2(avg)} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} I_{max}\sin(\theta-\beta)\, d\theta$$

$$= \frac{I_{max}}{\pi}\cos\beta(\cos\alpha_1 - \cos\alpha_2) \quad . \tag{13}$$

By symmetry, $I_{3(avg)} = 0$, $I_{4(avg)} = -I_{2(avg)}$ and $I_{5(avg)} = -I_{1(avg)}$.
Therefore, if each capacitor voltage is to be under regulation, the average currents per cycle which should be supplied from each capacitor are as follows:

$$I_{C1(avg)} = I_{1(avg)} \tag{14}$$

$$I_{C2(avg)} = I_{1(avg)} + I_{2(avg)} \quad . \tag{15}$$

Thus,

$$I_{C1(avg)} = \frac{I_{max}}{\pi}\cos\beta\cos\alpha_2 \tag{16}$$

$$I_{C2(avg)} = \frac{I_{max}}{\pi}\cos\beta\cos\alpha_1 \quad . \tag{17}$$

Obviously, $I_{C1(avg)} < I_{C2(avg)}$ for $\alpha_1 < \alpha_2$. This results in capacitor charge unbalancing. The charge of inner capacitor C_2 (C_3) flows out more than that of outer capacitor C_1 (C_4) and thus V_{C2} (V_{C3}) goes to ground level as time goes. Also, from Eq. (16),(17)

$$\frac{\cos\alpha_1}{\cos\alpha_2} = \frac{I_{C2(avg)}}{I_{C1(avg)}} \quad (18)$$

Eq.(18) means that capacitor charge unbalancing exists regardlessly of load condition and it is only dependent on control strategy (i.e.,α_1, α_2). Though any multilevel PWM is employed, capacitor charge unbalancing is the same as simple control, supposing effective control angles.

Capacitor charge unbalancing problem can be solved simply employing some regulation circuitry which forces energy transfer from outer capacitor to inner capacitor. Fig. 12 shows such circuit remedies where well-known buck-boost converter is used and each converter is composed of T_1 - D_1 - L_{S1} or T_2 - D_2 - L_{S2}.

VI. CONCLUSION

A general circuit topology of multilevel inverters above three level is suggested. When compared with conventional two-level inverters, the multilevel structure allows to raise the power handling capability in the conversion process in a very powerful and systematical way while the level of inverter employed can be determined according to the inverter input voltage, output power, device rating, waveform quality required, etc. The proposed multilevel inverter can realize any multilevel pulsewidth modulation scheme which leads to harmonic content reduction and provides full utilization of semiconductor devices like GTOs especially in high power range where high voltage could be applied. Thus, with our multilevel inverter, 6600V direct conversion could be possible requiring no additional coupling component such as transformer. Moreover, high quality output waveform in higher level inverter can be applicable to, for example, high power uninterrupteble power supply system such as TRIPORT type with low switching frequency and thus high efficiency.

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