A Programmable 3.2-GOPS Merged DRAM Logic for Video Signal Processing

Sunho Chang, Bum-Sik Kim, and Lee-Sup Kim

***Abstract*—This paper proposes a programmable high-performance architecture of datapath in the merged DRAM logic (MDL) for video signal processing. A model of a datapath in the programmable MDL is generated, and two basic parameters, *total required clock cycles (TRCC)* and *DRAM access rate (DAR)*, are defined by analysis of the model. Design guidelines are suggested for the optimized video signal processor based on the modeling and analysis of the MDL. The inverse discrete cosine transform (IDCT) and motion compensation (MC) of the video signal processing are analyzed in the MDL architecture. Two measures, TRCC and DAR, are determined such that the data bandwidth between DRAM and logic is not a bottleneck in the MDL architecture. The efficient datapath is designed based on these design guidelines. The datapath has processing units (ALU, MAC, and Barrel Shifter) with splittabilities of data and multi-port SRAM. The maximum performance of the proposed datapath with 200-MHz clock frequency is 3.2 GOPS for 8-bit video signals, which can deal with decoding high-level (1920×1080) in MPEG. The proposed MDL architecture has 2.1–4.8 times higher performance compared with conventional dedicated hardware chips. It can also be used for other multimedia signal processing due to its programmability.**

***Index Terms*—Merged DRAM logic (MDL), MPEG, programmable architecture, video signal processing, VLSI.**

I. Introduction

MANY popular multimedia applications such as digital TV, 3-D graphics, and MPEG encoding/decoding require high computing power. However, there exists a big performance gap between a processor and DRAM in terms of data throughput. There have been many efforts to modify the architecture of DRAM for the goal of achieving higher bandwidth. One of these trends is a series of synchronous DRAM. Additional circuitry is added in DRAM for synchronization to obtain higher bandwidth. Another is some series of special memories, such as Video DRAM, Window DRAM, and SGRAM. Special logic circuits are added to DRAM to reach the performance level required for video or graphic applications. However, several types of DRAM and various modified DRAM architectures accompany large power dissipation or large latency to obtain high bandwidth [1]. Thus, merging high-density DRAM with high performance logic in a single chip is considered as a feasible solution of obtaining higher bandwidth and lower power dissipation. It also overcomes the performance limitations of previous DRAM architectures [2].

In previous works, there are two approaches in designing merged DRAM logic (MDL). One is to merge a general-purpose processor and DRAM. This approach provides programmability for many applications, but dissipates large power and requires considerable hardware resources [3], [4]. The other approach is to merge a dedicated signal processor and DRAM [5]–[7], which enables an efficient usage of hardware resources and low power dissipation, but it does not have programmability, thus applications are restricted. As yet another approach, the activities to obtain programmable-specific hardware for multimedia applications have been tried in [8] and [9]. Those activities show low power dissipation, but do not meet high enough performance for high-quality video signal processing.

In this paper, we propose a programmable high-performance MDL architecture for video signal processing with an efficient use of hardware resources, low power, and programmability. The applications of video signal processing are analyzed by using the proposed MDL model and the requirements of the performance are examined in the MDL. Total required clock cycles (TRCC) is defined to express the number of required clock cycles for the application and DRAM access rate (DAR) is defined to indicate a synergy effect of merging DRAM with logic circuitry in a single chip. The performance of IDCT and MC in MDL is evaluated and the effective datapath of the MDL architecture is designed. This paper is organized as follows. Presented in Section II are the basic model and analysis of MDL architecture. In Section III, design guidelines and the datapath of the MDL are explained. In Section IV, performance evaluations and experimental comparisons are given, and Section V concludes this paper.

II. Modeling and Analysis

The basic model of MDL architecture consists of processing units (PUs), a merged DRAM, a temporal storage (TS), and some control units. Key parameters are defined to analyze performance of the MDL architecture as follows.

- *Bus width between DRAM and temporal storage unit (WDB)*: this parameter is one of the key parameters in the MDL, which directly indicates improvements of the performance.
- *Number of processing units (NP)*: this parameter affects the number of clock cycles to execute required operations in the MDL system.
- *Size of temporal storage (STS)*: this parameter affects the number of accesses to DRAM. It depends on the size of basic data block in video signal processing.

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- *Latency of DRAM* ($\text{LATENCY}_{\text{DRAM}}$): this parameter can be changed by modifying interconnect bus circuits, which drive load capacitance between DRAM and logic.
- *Latency of temporal storage unit* ($\text{LATENCY}_{\text{TS}}$): this parameter is the number of clock cycles between address-inputs and data-outputs in temporal storage unit.
- *Latency of processing unit* (LATENCY_{PU}): the effect of this parameter decreases as the amount of data to be dealt with increases.

A. A Qualitative Analysis

The proposed programmable MDL architecture executes required operations according to the sequence of instructions for video signal processing. The instructions can be categorized as three stages:

1) *data transfer from DRAM to DSP core* [Read];
2) *data processing in the DSP core* [Compute];
3) *data transfer from DSP core to DRAM* [Write].

Execution time of the required operations for a basic block can be represented as

$$\text{Execution Time} = \text{Data Read} + \text{Data Processing} + \text{Data Write}. \quad (1)$$

The number of required clock cycles for each item can be formularized by using the defined parameters. At first, if STS is greater than *size of basic data block* (SBD), the number of *clock cycles for Data Read* (CC_{READ}) can be expressed as

$$\text{CC}_{\text{READ}} = \left[\frac{\text{SBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}} \quad (2)$$

where $[f]$ means the minimum integer number above a fractional number f, SBD is *size of basic data block* for video signal processing. If STS is less than SBD, the size of data to be dealt with should be reduced to smaller SBD, which is defined as RSBD, to meet the condition of data correlation: STS $>$RSBD + STCR, i.e., all data in the same flow of data processing should be stored in a temporal storage unit where STCR means *size of temporal computation result*. Then (2) should be modified as

$$\text{CC}_{\text{READ}} = \left(\left[\frac{\text{RSBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right) \cdot \left[\frac{\text{SBD}}{\text{RSBD}}\right] \quad (3)$$

where [SBD/RSBD] is defined as *multiplication factor* in the case of STS $<$ SBD. This indicates that small size of temporal storage in the DSP core increases the number of clock cycles to transfer data between DRAM and DSP core. Secondly, number of *clock cycles for Data Processing* ($\text{CC}_{\text{Compute}}$) can be calculated as

$$\text{CC}_{\text{Compute}} = \frac{\text{CA}}{\text{NP}} + \text{LATENCY}_{\text{PU}}, \quad \text{for STS} > \text{SBD} \quad (4)$$

$$\text{CC}_{\text{Compute}} = \left(\frac{\text{RCA}}{\text{NP}} + \text{LATENCY}_{\text{PU}}\right) \cdot \left[\frac{\text{SBD}}{\text{RSBD}}\right], \quad \text{for STS} < \text{SBD} \quad (5)$$

where we have *computation amounts* (CA) and *reduced computation amounts* (RCA). Next, *TRCC*, as the sum of clock cycles for *Data Read, Data Processing, and Data Write* is defined to calculate required clock cycles for video signal processing in MDL architecture. The TRCC for a basic data block is represented as

$$\begin{aligned}\text{TRCC} &= 2 \times \text{CC}_{\text{READ}} + \text{CC}_{\text{Compute}} \\ &= 2\left(\left[\frac{\text{SBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right) + \frac{\text{CA}}{\text{NP}} + \text{LATENCY}_{\text{PU}}, \quad \text{for STS} > \text{SBD}\end{aligned} \quad (6)$$

$$\begin{aligned}\text{TRCC} &= 2\left(\left[\frac{\text{RSBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right) \times \left[\frac{\text{SBD}}{\text{RSBD}}\right] + \left(\frac{\text{RCA}}{\text{NP}} + \text{LATENCY}_{\text{PU}}\right) \times \left[\frac{\text{SBD}}{\text{RSBD}}\right], \quad \text{for STS} < \text{SBD}\end{aligned} \quad (7)$$

on the assumption that CC_{WRITE} is the same as CC_{READ}. In addition, DAR is defined as *ratio of clock cycles for data transfer to clock cycles for computation* to show the effect of merging DRAM and logic, which is given in (8) and (9). This value indicates how much the performance is improved after merging DRAM and logic as a single chip

$$\text{DAR} = \frac{\text{Clock Cycles for Data Transfer}}{\text{Clock Cycles for Computation}} = \frac{2\left(\left[\frac{\text{SBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right)}{\frac{\text{CA}}{\text{NP}} + \text{LATENCY}_{\text{PU}}}, \quad \text{for STS} > \text{SBD} \quad (8)$$

$$\text{DAR} = \frac{2\left(\left[\frac{\text{RSBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right) \cdot \left[\frac{\text{SBD}}{\text{RSBD}}\right]}{\left(\frac{\text{RCA}}{\text{NP}} + \text{LATENCY}_{\text{PU}}\right) \cdot \left[\frac{\text{SBD}}{\text{RSBD}}\right]}, \quad \text{for STS} < \text{SBD}. \quad (9)$$

TRCC and DAR are used to provide design guidelines for the MDL system.

B. A Quantitative Analysis of Applications

The decoding algorithm in MPEG is analyzed to design the datapath in MDL, which consists of variable length decoding (VLD), inverse quantization (IQ), inverse discrete cosine transform (IDCT), and motion compensation (MC) [10]. The VLD is not a data-intensive function compared to IDCT or MC, thus it is neglected in designing datapath. The required clock cycles in MDL architecture is calculated for video signal processing. Assuming that resolution of the video frame is $\text{NP}_H \times \text{NP}_V$ and the size of a basic data block for computation is $\text{NB}_H \times \text{NB}_V$, a performance metric to execute required video signal processing for one frame can be written as

$$\text{clock cycles to process basic data block} \times \frac{\text{NP}_H}{\text{NB}_H} \times \frac{\text{NP}_V}{\text{NB}_V}. \quad (10)$$

TABLE I
TRCC FOR 8 × 8 IDCT IN THE MDL

WDB	L_{DRAM}	NP = 1		NP = 4		NP = 8		NP = 16	
[bits]	[clks]	L_{PU}=1	L_{PU}=2	L_{PU}=1	L_{PU}=2	L_{PU}=1	L_{PU}=2	L_{PU}=1	L_{PU}= 2
64	3	1020	1048	248	280	136	152	80	88
	6	1026	1054	254	286	142	158	86	84
256	3	1008	1036	236	268	124	140	68	76
	6	1014	1042	242	274	130	146	74	82
512	3	1004	1032	232	264	120	136	64	72
	6	1010	1038	238	270	126	142	70	78
1024	3	1004	1032	232	264	120	136	64	72
	6	1010	1038	238	270	126	142	70	78

A performance metric for video signal frames can be estimated after calculating TRCC for two main functions IDCT and MC in MDL.

IDCT: The IDCT operation is applied to full frame (or field) of digital video signal, thus it requires a high computing power and frequent memory accesses in general DSP architecture. The 8×8 block IDCT operation consists of two 8-line, 8-point IDCT, i.e., 8-line horizontal and 8-line vertical operations [11]. The minimum size of temporal storage for a 8×8 block IDCT operation is $8 \times 8 + 8$ (to store results of ALU operations) to prevent additional DRAM accesses. The computation amount CA can be calculated from the rank-4 matrix as

$$\begin{aligned}\text{CA} &= \text{Addtion (or subtraction)} + \text{Division (by 2)} \\ &\quad + \text{Matrix calculation} \\ &= 4\text{ADDs(or 4SUBs)} + 4\text{DIVs}(by\ 2) + 16\text{MACs} \\ &= 4 \times (\text{ADD(or SUB)} + \text{DIV(by 2)} + 4c\text{MAC}) \end{aligned} \quad (11)$$

where $4c$MAC indicates four continuous-MAC operations.

The required total clock cycles can be obtained from (6) for an 8×8 block IDCT operation as

$$\begin{aligned}\text{TRCC}_{\text{IDCT}} = 2\left(\left[\frac{\text{SBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right) \\ + \frac{128}{\text{NP}} \times (\text{ADD(or SUB)} + \text{DIV(by 2)} \\ + 4c\text{MAC}) + \text{LATENCY}_{\text{PU}}\end{aligned} \quad (12)$$

where DIV means division by two. From (12), it can be easily predicted that the number of PUs dominates $\text{TRCC}_{\text{IDCT}}$ to execute 8×8 block IDCT if WDB is larger than SBD. The $\text{TRCC}_{\text{IDCT}}$ for a basic block is summarized in Table I.

Table I shows that $\text{TRCC}_{\text{IDCT}}$ has strong dependency on the number of PUs. From (8), DAR_{IDCT} can be written as in (13), shown at the bottom of the page, where DAR_{IDCT} decreases rapidly as the PU and WDB increase.

MC: The operation of MC is applied to full frame (or field) of digital video signal. The MC of the MPEG decoding is formulated as linear matrix with rank 4. Since there is no data correlation between pixels of the same frame in the MC, size of temporal storage does not affect the sequence of the MC. If we assume that N_B is *number of 4-pixel* (2×2) *block* and N_D is *number of bits for a pixel*, the maximum amount of data to be transferred in field mode is $4\text{MV}+4N_BN_D$ [bits] where MV indicates a *motion vector*, N_BN_D means number of bits for a data block. *Four* motion vectors and *four* data blocks are required to calculate a pixel in the field mode. The $4 \times 4c$MAC of computation amounts are necessary for an N_D. From (6), the required total clock cycles to execute the MC of a basic block data can be written as

$$\begin{aligned}\text{TRCC}_{\text{MC}} = 2\left(\left[\frac{\frac{4}{2}\text{MV}+4N_BN_D}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right) \\ + \frac{N_B}{\text{NP}} \times 4 \times 4c\text{MAC} + \text{LATENCY}_{\text{PU}}\end{aligned} \quad (14)$$

where the Write operation of *four* motion vectors is not necessary, hence 4MV is divided by two. The TRCC_{MC} for a basic block is summarized in Table II. The number of clock cycles of the $4c$MAC is *five* for one clock latency, and *six* for two clock latency. The DAR_{MC} is affected by the number of PUs, but the

$$\text{DAR}_{\text{IDCT}} = \frac{2\left(\left[\frac{\text{SBD}}{\text{WDB}}\right] + 1 + \text{LATENCY}_{\text{DRAM}}\right)}{\frac{128}{\text{NP}} \times (\text{ADD(or SUB)} + \text{DIV(by 2)} + 4c\text{MAC}) + \text{LATENCY}_{\text{PU}}} \quad (13)$$

TABLE II
TRCC FOR MC IN THE MDL

WDB	L_{DRAM}	NP = 1		NP = 4		NP = 8		NP = 16	
[bits]	[clks]	L_{PU}=1	L_{PU}=2	L_{PU}=1	L_{PU}=2	L_{PU}=1	L_{PU}=2	L_{PU}=1	L_{PU}= 2
64	3	336	400	96	112	66	78	36	46
	6	342	406	102	118	72	84	42	52
256	3	332	396	92	108	62	74	32	42
	6	338	402	98	114	68	80	38	48
512	3	330	394	90	106	60	72	30	40
	6	336	400	96	112	66	78	36	46
1024	3	328	392	88	104	58	70	28	38
	6	334	398	94	110	64	76	34	44

$L_{DRAM} = LATENCY_{DRAM}$, $L_{PU} = LATENCY_{PU}$

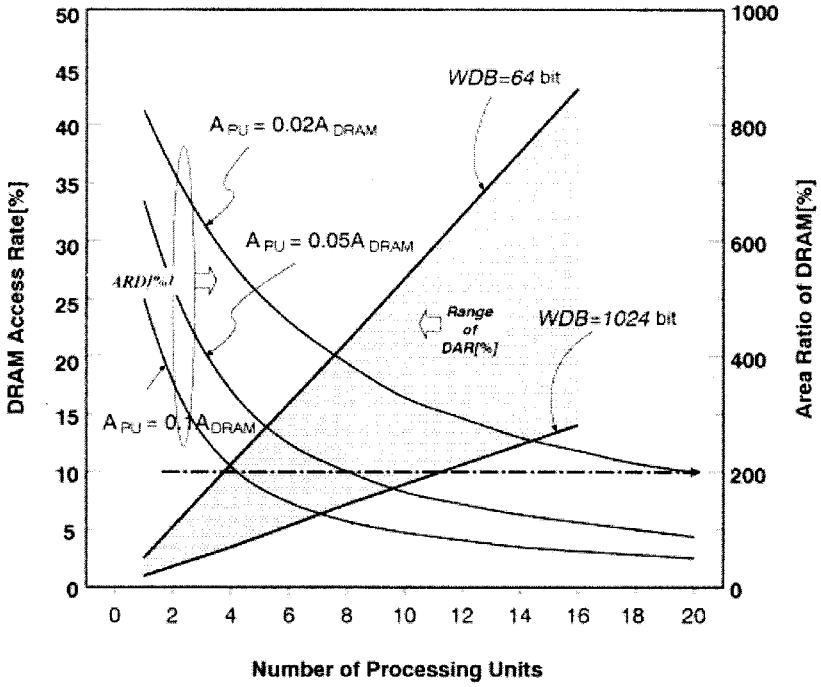

Fig. 1. DAR and ARD versus number of PUs.

effect is small compared to that of IDCT. From (8), $\mathrm{DAR_{MC}}$ is represented as

$$\mathrm{DAR_{MC}} = \frac{2\left(\left[\dfrac{2\mathrm{MV}+4N_BN_D}{\mathrm{WDB}}\right]+1+\mathrm{LATENCY_{DRAM}}\right)}{\dfrac{N_B}{\mathrm{NP}}\times 4\times 4c\mathrm{MAC}+\mathrm{LATENCY_{PU}}}. \tag{15}$$

III. DESIGN OF DATAPATH IN MDL

A. Design Guidelines for MDL

Design guidelines for the datapath of the MDL are suggested from TRCC and DAR, and from the analysis of the MPEG2 decoding algorithm. Two major considerations are:

1) TRCC *should be kept minimized to reduce power dissipation*;
2) DAR *should be kept minimized to maximize synergy effect of the* MDL.

Then, design guidelines for the datapath are suggested as follows.

1) *An optimized bus width between DRAM and DSP core is necessary for a low power dissipation and an efficient usage of silicon area*.
2) *A wide data bus architecture is necessary in the DSP core*: all PUs should be operated at the same time to reduce clock frequency. Then, inputs and outputs of PUs can be manipulated without a bottleneck.

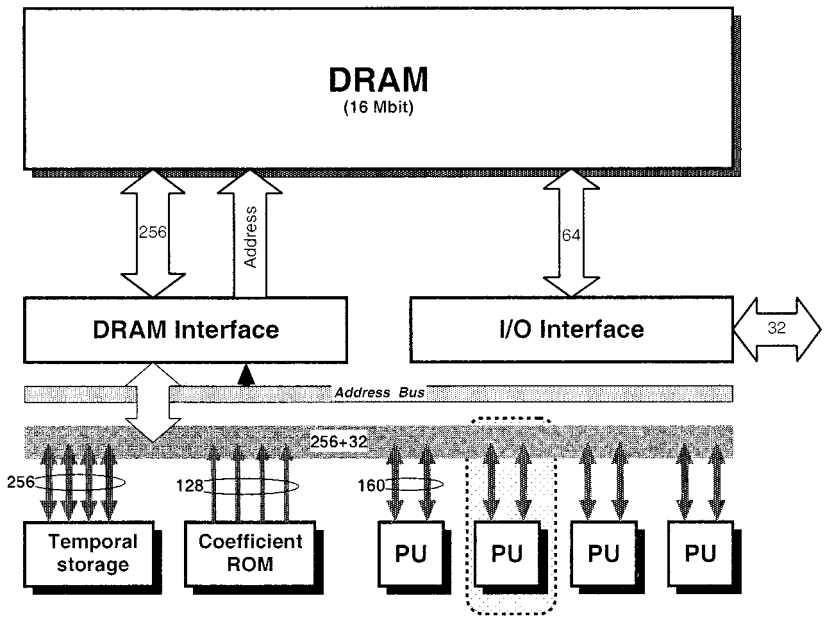

Fig. 2. Datapath in the MDL for video signal processing.

TABLE III
CLOCK FREQUENCY FOR MPEG2 DECODING (EXCEPT VLD) VERSUS RESOLUTION

Level	Resolution(H×V)	CF_{DECODE} [MHz]
Low	352 × 288	6
Main	720 × 480	20
High-1440	1440 × 1080	88
High	1920 × 1080	116

CF_{DECODE} = clock frequency to decode MPEG2

3) *Number of PUs should be maximized*: the DAR decreases rapidly in MDL architecture with many PUs, which can reduce clock frequency.
4) *A large and fast temporal storage should support multiple PUs and data manipulations for several video formats.*

The other design constraint in MDL architecture, i.e., area of the VLSI chip, should be also investigated in designing MDL. The area of MDL architecture can be represented as

$$A_{\mathrm{MDL}} = A_{\mathrm{DRAM}} + A_{\mathrm{TS}} + A_{\mathrm{CROM}} + A_{\mathrm{MISC}} + \mathrm{NP} \times A_{\mathrm{PU}} \quad (16)$$

where A_{DRAM}, A_{TS}, A_{CROM}, A_{MISC}, and A_{PU} mean the area of DRAM, temporal storage, coefficient ROM, miscellaneous blocks, and a PU. ARD, *area ratio of DRAM*, can be defined as

$$\mathrm{ARD} = \frac{\text{Area of DRAM}}{\text{Area of Logic}} = \frac{A_{\mathrm{DRAM}}}{\mathrm{NP} \times A_{\mathrm{PU}} + A_{\mathrm{TS}} + A_{\mathrm{CROM}} + A_{\mathrm{MISC}}}. \quad (17)$$

The total area of a VLSI chip for an application is limited by three major factors: *yield, cost, and power dissipation*. Fig. 1 shows the range of DAR and ARD versus the number of PUs in the MDL chip. The number of PUs should be carefully determined. The $A_{\mathrm{others}} (= A_{\mathrm{TS}} + A_{\mathrm{CROM}} + A_{\mathrm{MISC}})$ is assumed as $0.1 \cdot A_{\mathrm{DRAM}}$ and an area of a PU (A_{PU}) is assumed as three kinds, $0.02 \cdot A_{\mathrm{DRAM}}$, $0.05 \cdot A_{\mathrm{DRAM}}$, and $0.1 \cdot A_{\mathrm{DRAM}}$. If A_{PU} and ARD is selected as $0.1 \cdot A_{\mathrm{DRAM}}$ and 200%, respectively, then the number of PUs is determined as *four* (32-bit format). However, the effect of merging DRAM and logic is small when WDB is expanded from 64-bits to 1024-bits. In other words, Δ DAR (about 7%: from 10% to 3%) is small when NP = 4. As the number of PUs increases, Δ DAR becomes larger when WDB is widened in Fig. 1. Therefore, it is important to increase the effective number of PUs without increment of chip area to obtain a large Δ DAR when WDB is widened.

B. Design of Datapath

The MDL architecture is designed based on the previous design guidelines. The design targets are implementing a high performance MDL system, and limiting the maximum clock frequency of DSP core to 200 MHz for low power dissipation in decoding MP@HL(1920×1080) in MPEG2. The area of theVLSI chip is also limited for high yield. Considering constant hardware resources, three prerequisite conditions are assumed, which are extracted from the previous analysis and design guidelines.

1) *There are four 32-bit PUs in the DSP core*: this constraint comes from the limitation of chip area as exhibited in Section III-A.
2) *Width of data bus in the DSP core is sufficiently large to support parallel processing capabilities of four 32-bit PUs*: since one 32-bit PUs require two operands, 256-bits are required for *four* 32-bit PUs in the DSP core.
3) *Size of temporal storage is larger than size of block data for the application*: the minimum 72 bytes are necessary for the 8×8 block IDCT. This condition removes additional DRAM accesses, so that TRCC is reduced.

The proposed datapath in MDL architecture for video signal processing is shown in Fig. 2. The MAC, ALU, and barrel shifter

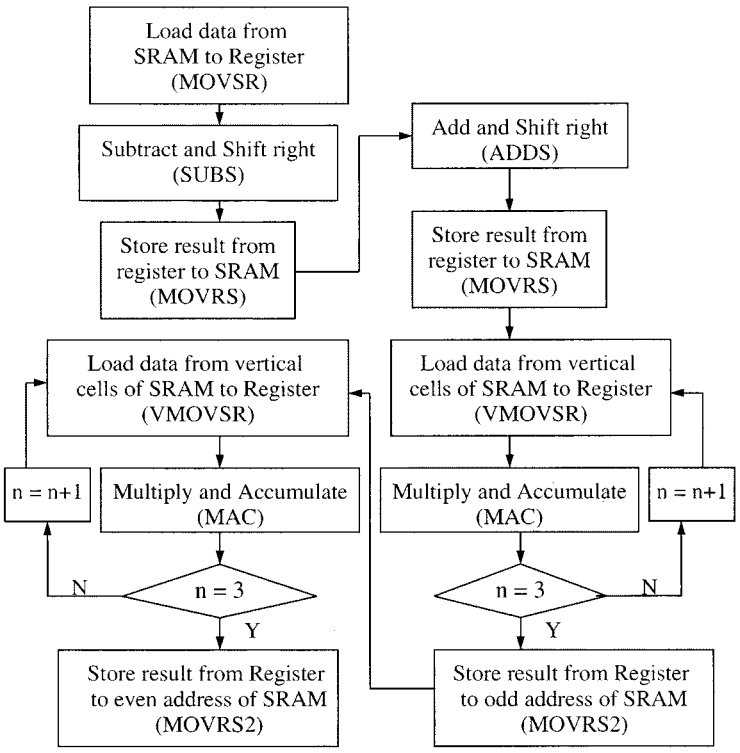

Fig. 3. Instruction sequence of the IDCT in MDL.

that have bit-splittable capabilities and multi-port SRAM that has 256-bit simultaneous data accessibility are designed to increase effectiveness in processing video signals. That enables clock frequency of the proposed MDL to be less than 200 MHz for decoding of MP@HL in MPEG2.

IV. Performance of the Proposed MDL

The performance of the MDL is evaluated for MPEG2 decoding based on the TRCC. The simulation results of datapath are compared to other dedicated hardware chips.

A. Performance Evaluation

CF_{DECODE}, the *clock frequency to decode MPEG2* in MDL, can be calculated as (except VLD)

$$\begin{aligned} CF_{DECODE} = &(TRCC_{IDCT} + TRCC_{MC} + TRCC_{IQ}) \\ &\times (\text{number of pixels per basic block: } 8 \times 8) \\ &\times (\text{number of basic block per second}) \end{aligned} \tag{18}$$

where $TRCC_{IQ}$ is the number of TRCC for IQ, which requires one multiplication per one pixel. The required clock frequencies for decoding of MPEG2 in *four* kinds of levels are shown in Table III. The computational results for the clock frequencies show that the proposed MDL architecture can execute a high level of MPEG2 decoding with a 120-MHz clock. Since there is a color signal in digital video signals, a 200-MHz MDL architecture is required. The maximum data bandwidth between DRAM and logic is 6.4 Gbytes/s and the maximum processing capabilities for 8-bit video signal is 3.2-GOPS with a 200-MHz clock. The relative performance of the proposed MDL is compared to industrial standards [12]. The proposed MDL can decode MPEG2 signal in MP@ML with the same clock frequency of the hardwired logic. Therefore, the proposed MDL has higher computing capabilities over general types of processors and also versatile programmability for video signal processing.

B. Simulation Results

The performance of the proposed architecture is verified by an architecture simulator for the integrated *four* PUs and a coefficient ROM through the *eight* 32-bit data bus. *Single instruction multiple data* (SIMD) type 4-depth vector instructions are generated for a simulation of programmable environments targeting IDCT operation as a benchmark to verify the performance of the MDL. The instruction sequences for the IDCT are shown in Fig. 3. The words in parentheses in Fig. 3 are SIMD type instructions, which are generated for the DSP core. The *clock cycles for read and write* ($CC_{READ,\,WRITE}$) and the *clock cycles for data processing* ($CC_{COMPUTE}$) can be obtained from the simulation. The TRCC for 32 pixels (half of 8×8 block) of the 1-D IDCT is obtained to be 24, as follows:

$$\begin{aligned} CC_{READ,\,WRITE} = &\,1(\text{MOVSR}) + 2(\text{MOVRS}) \\ &+ 1(\text{VMOVSR}) \times 4(\text{columns}) \\ &\times 2(\text{SUBS and ADDS}) + 1(\text{MOVRS2}) \\ &\times 2(\text{SUBS and ADDS}) = 13 \\ CC_{COMPUTE} = &\,4(\text{SUBS}) + 1(\text{ADDS}) \\ &+ 3(\text{LDI}) \times 2(\text{columns}) = 11 \end{aligned} \tag{19}$$

where instruction LDI stands for *load data immediately*. The proposed datapath is compared with conventional dedicated

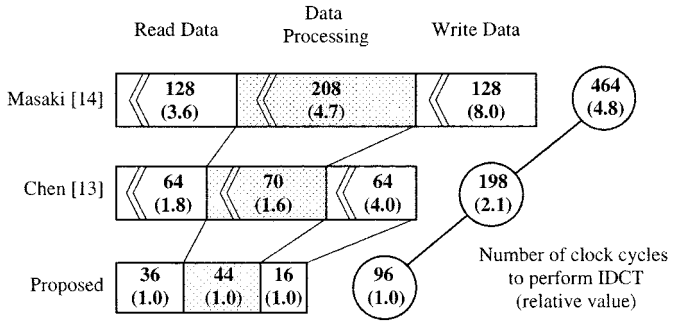

Fig. 4. Performance comparison with conventional structures.

architectures [13], [14] to perform the IDCT. A performance comparison is shown in Fig. 4. The number in the figure shows required clock cycles to perform the IDCT for the 8×8 basic block, the numbers in parentheses are relative clock cycles when the required clock cycles in MDL is regarded as number *one* (1.0). The proposed MDL architecture shows 2.1–4.8 times higher performance compared to conventional architectures.

V. Conclusion

A programmable architecture of MDL is proposed for video signal processing. The proposed MDL can decode a high level (1920×1080) of MPEG2, and also achieve a 3.2 GOPS processing power for 8-bit video signal processing in a 200-MHz clock. It has 2.1–4.8 times higher performance for the IDCT compared to the previous two conventional architectures, which do not have programmability. The optimization of various datapaths is executed according to the proposed model and design guidelines in MDL. Two measures, TRCC and DAR, are defined such that they take into account effect of various parameters on the performance of MDL architecture. The methodology of MDL modeling and analysis can also be used to implement high-performance merged DRAM logic for other multimedia applications such as digital-TV, 3-D graphics, and MPEG2 encoding.

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