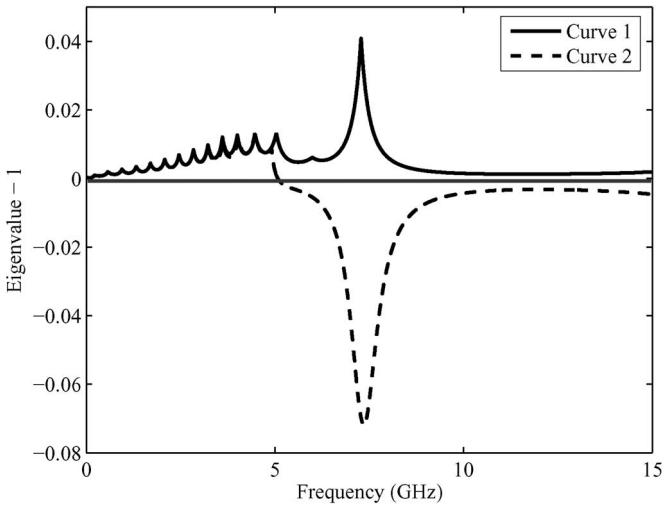

Fig. 3. Eigenvalue plot of real part of admittance matrix.

VI. Conclusion

In this paper, a novel formulation of TE is presented, which enables the inclusion of PR matrix rational approximation of FD-PUL parameters directly in the TEs and does not require the explicit lumped-circuit realization in terms of positive elements. The resulting reduced model of the TEs using the ICT technique is guaranteed to be passive.

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A Delay Line Circuit Design for Crosstalk Minimization Using Genetic Algorithm

Chaeho Chung, Soobum Lee, Byung Man Kwak, Gawon Kim, and Joungho Kim

***Abstract*—Most signals between chips or packages in an electric circuit board require certain delays in order to achieve good timing. An extension of the circuit line that is proportional to the designated time delay has been a usual practice due to cost effectiveness. However, the layout of the line becomes dense due to the small size of packages or circuit boards, and this generates crosstalk, causing signal detection errors. In this paper, a design methodology of delay line layout for crosstalk minimization is developed using the genetic algorithm (GA). The GA requires a large number of function evaluations, and efficient calculation of crosstalk is proposed together with a new technique of generating random line, making offsprings, and mutation. Different optimum results have been obtained for different objectives and compared. Some of the designs were actually manufactured and experimentally tested, showing the validity of the optimum results.**

***Index Terms*—Crosstalk minimization, genetic algorithm (GA), optimum delay line layout.**

I. Introduction

With the competition for cheaper and smaller products, the need for low-cost and high-density circuit board increases. One of the important tasks encountered in the development of such a circuit board is to design delay line paths according to a designated signal delay. A widely accepted practice is to extend the circuit line in proportion to the desired time delay. However, the layout tends to become dense and twisted due to size limitation. These lines can cause a crosstalk which deteriorates the signal quality such as voltage drop, or jitter should be minimized.

For analyses of crosstalk, Wu and Chao [1] suggested a wave-tracing technique and a quantitative analysis with the help of connection matrix. A laddering crosstalk analysis [2] and a method of moments are also proposed [3]. With the help of these or other analysis techniques, much endeavor to reduce crosstalk has been performed, for example, for wires in a VLSI chip [4]–[6], or by adjusting the line spacing [7]. A framework for fast multilevel routing, considering crosstalk and timing, has been proposed [8], and a similar routing problem has been solved using the genetic algorithm (GA) to minimize the crosstalk [9]; both of them optimize a chip-level routing. However, little study on layout changes in a PCB board has been reported even though much larger effect is expected.

Currently, the meander (or serpentine) line shape is mainly used in the industry due to its simple shape. However, the detail dimensions, such as the gaps between any two line and the line lengths, still need to be modified by trial and error [1], [2], [10], [11] in order to

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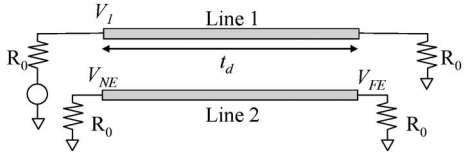

Fig. 1. Parallel transmission lines with matched transmission [11]. A pulse transmitted on the upper line generates crosstalk on the lower line.

reduce the high peak value of the crosstalk, which is known as the disadvantage of the meander line. The spiral line layout is suggested for this reason, whereas it produces a widely and asynchronously accumulated crosstalk [1], [10]. Although the concentric Cs delay has been proposed so as to keep the crosstalk closer to the input signal [11], it did not reduce the crosstalk compared with the spiral line. Existing delay lines show different shortcomings. Therefore, a systematic procedure is required to select among existing delay lines or to design a delay line following specific design requirements.

With this motivation, a procedure of simulation is first developed, and a general delay line design method is proposed in this paper.

II. Crosstalk Calculation

A single delay line case, rather than differential signaling, is mainly considered in this paper. Let us explain the crosstalk calculation by taking two adjacent parallel sections, as shown in Fig. 1. We assume that the crosstalk is generated only in the adjacent parallel line. The crosstalk decreases exponentially with the distance, and the effect from the next adjacent parallel lines is negligible.

If a ramped step pulse (the amplitude is $V_{\rm in}$, and the rising time is T_r) is introduced from the starting point at t_0 and travels along the active line (line 1 or the aggressor), the capacitive and inductive couplings occur between two lines, and they cause the near-end (NE) and far-end (FE) crosstalk on the adjacent parallel line (line 2 or the victim) [12], [13]. The NE and FE crosstalk are proportional to $V_{\rm in}$, and the proportional constants for each crosstalk are expressed as follows [14]:

$$k_{\rm NEXT} = \frac{1}{4}\left(\frac{C_m}{C_{11}} + \frac{L_m}{L_{11}}\right)$$
$$k_{\rm FEXT} = \frac{1}{2}\left(\frac{C_m}{C_{11}} - \frac{L_m}{L_{11}}\right) \quad (1)$$

where C_m and C_{11} are the mutual capacitance and the self-capacitance, respectively, and L_m and L_{11} are the mutual inductance and the self-inductance, respectively. These capacitance and inductance are the functions of the distance between line 1 and line 2 (s_l) [15], and other parameters (the width of the delay line, the height of PCB board, impedance, and so on) are assumed to be fixed. The NE crosstalk has positive voltage and moves leftward, whereas the FE crosstalk has negative voltage and moves rightward in line 2.

We predict the total crosstalk in a delay line by the superposition [15] upon the time domain from each line segment. The time delay of each segment is denoted as $\rm TD_s$. This numerical superposition procedure is summarized in Fig. 2 with a simple example. For the segmented line layout in Fig. 2 (the number of line segments is $n-1$, and $n=12$ in this example), we visit each line segment (l) in order and find a victim segment (a_l). After measuring the gap (s_l) between l and a_l, the NE/FE crosstalk, proportional to $k_{\rm NEXT}$ and $k_{\rm FEXT}$, respectively, is calculated and superposed on the original time-domain reflectometry (TDR) and time-domain transmit (TDT) waveforms, as shown in Fig. 2. In this figure, the original waveform (W_i) and the crosstalk (W_c) are indicated by solid and dotted lines, respectively. For NE crosstalk in a_l, a $2\times \rm TD_s$ wide, $k_{\rm NEXT}\times V_{\rm in}$ high, and rectangular wave is superposed. For FE crosstalk in a_l, on the other hand, a T_r wide, $k_{\rm FEXT}\times V_{\rm in}$ deep, and triangular wave is superposed. In either case, the crosstalk is superposed at $t_0+(l+a_l-1)\times \rm TD_s$ if it is toward TDR, or at $t_0+(n+l-a_l-1)\times \rm TD_s$ if it is toward TDT. a_l can be plural if there is any $a_6=2$ and 10, for example. The procedure is repeated until l reaches $n-1$.

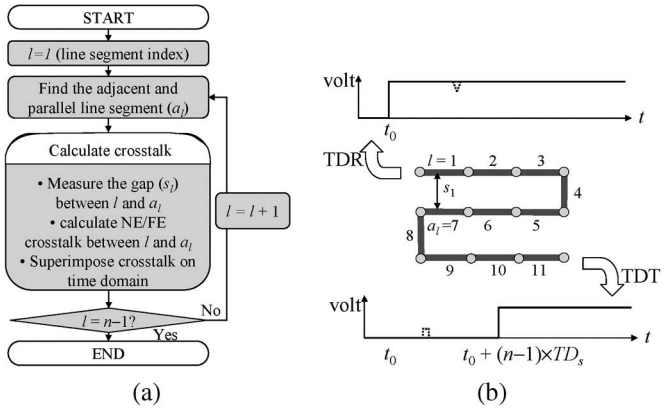

Fig. 2. Procedure of crosstalk calculation. (a) Flow chart. (b) Case study.

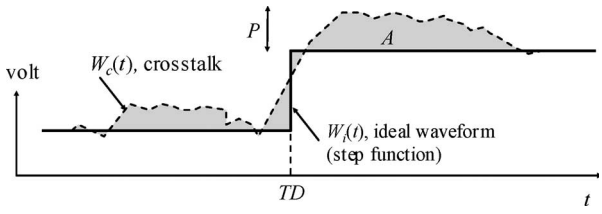

Fig. 3. Characteristics of crosstalk in TDT waveform.

III. Optimization Strategy Using GA

In this section, we present the design method of delay line circuits to minimize crosstalk using GA. The general GA is tailored for the line layout design; the ways of creating the initial pool, making offspring, and mutation are suggested.

A. Optimization Formulation

In order to minimize the detection error caused by the distorted waveform with the crosstalk, harmful features of the crosstalk are chosen as objective functions to be minimized: the peak value (P), the total area of the unadulterated waveform (A), or the variance (V), as shown in Fig. 3 and in the following equations:

$$P = \max_t\{W_c - W_i\}$$
$$A = \int_0^{2\rm TD_l} |W_c - W_i|dt$$
$$M = \int_0^{2\rm TD_l} \frac{t|W_c - W_i|}{A}dt$$
$$V = \int_0^{2\rm TD_l} \frac{(M-t)^2|W_c - W_i|}{A}dt \quad (2)$$

where $\rm TD_l(=(n-1)\times TD_s)$ is the time delay from the starting to the ending points.

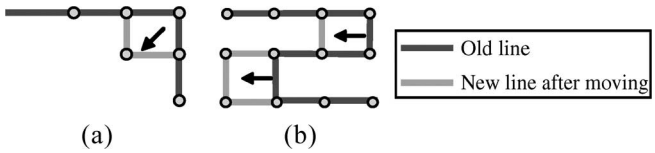

Fig. 4. Two ways of line modification without length change. (a) Point moving. (b) Conjugate moving.

A board that is defined as a rectangle is meshed, and a line is drawn by filling cells from the fixed starting point to the ending point. The design variable set $\mathbf{X}$ consists of the x and y coordinates of the cells in the filling order, and its component is a natural number. The optimization formulation is expressed as follows:

$$\text{Minimize } f = P(\mathbf{X}), A(\mathbf{X}), \text{or } V(\mathbf{X}) \tag{3}$$

$$\text{Subject to} \tag{4}$$

$$|x_j - x_{j+1}| + |y_j - y_{j+1}| = 1, \quad j = 1, \ldots, n-1 \tag{5}$$

$$|x_i - x_j| + |y_i - y_j| > 0,\ i = 1, \ldots, n, \quad j = 1, \ldots, i-1, i+1, \ldots, n \tag{6}$$

$$1 \le x_j \le C_{\text{width}}, 1 \le y_j \le C_{\text{width}}, \quad j = 1, \ldots, n, (x_j, y_j) \notin \mathrm{R} \tag{7}$$

where

$$\mathbf{X} = \begin{bmatrix} x_1 & x_2 & \ldots & x_n \\ y_1 & y_2 & \ldots & y_n \end{bmatrix}. \tag{8}$$

(x_1, y_1) and (x_n, y_n) are given when the starting and the ending points are fixed.

The objective function is defined to be one of the features in the crosstalk, as shown in (3). C_{width} and C_{height} are the total number of the columns and the rows in the meshed rectangle. $\mathbf{R}$ is the set of points within an obstacle area where no line should pass. The constraints denote the following conditions: (5) line connectivity condition (any two consecutive locations should have a distance of 1), (6) the condition to prevent line overlapping, and (7) the upper limits and obstacles in the circuit where the line should not pass.

B. Modified GA for Line Layout Design

An optimization method for line layouts is proposed using GA. First, we generate a number of lines to make the first pool (Section III-B1). Second, parent lines from the generated pool are selected. The third step is to make offspring to substitute worse lines in the pool. Finally, a new mutation scheme is performed, as explained in Section III-B3. These steps are repeated until the number of iteration reaches a predefined maximum iteration number [16].

1) Random Line Generation: For using GA, random chromosomes must be generated considering the constraints in (4)–(7). Each cell of a chromosome is represented by 3 bits: 1 bit for existence(1)/nonexistence(0) of line and 2 bits for the line extending direction [rightward(00), leftward(01), upward(10), and downward(11)]. The set of chromosomes uniquely defines $\mathbf{X}$. The proposed random line generation technique is composed of the following three steps: path finding from the starting point to the ending point, line length matching, and line moving. The shortest and nonintersecting connected line is first found from the starting point to the ending point, not overlapping the obstacle. Next, the line length is randomly extended until it reaches the designated length $(n-1)$. Finally, the line layout is modified while keeping the line length and the constraints in (4)–(7) using two ways shown in Fig. 4: a "point moving" [Fig. 4(a)] or a "conjugated moving" [Fig. 4(b)]. We visit every single cell where a corner is made, and we change the shape if the objective function is improved by "point moving," as shown in Fig. 4(a). "Conjugate moving" in Fig. 4(b) is tried afterward for all possible pairs. A pool (the first generation) is created by performing these three steps repeatedly z times (the size of the population).

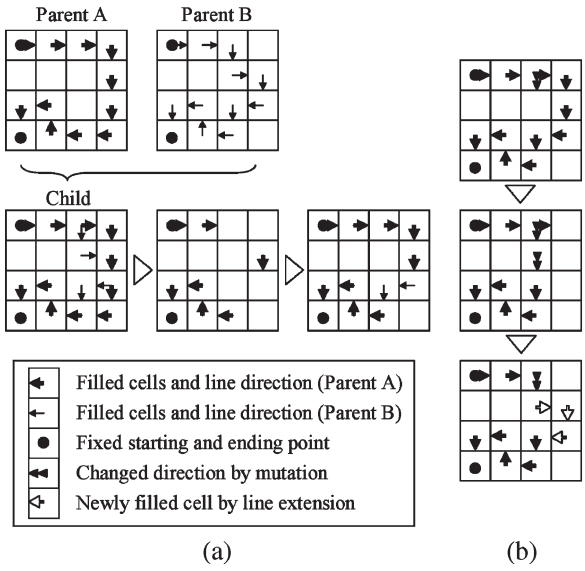

Fig. 5. Operations in the modified GA. (a) Making offspring. (b) Mutation.

TABLE I
EXPERIMENT CONDITIONS FOR CROSSTALK MEASUREMENT

Item	Quantity
Input voltage (V_{in})	250 mV
Impedance	50 Ω
Rising time of step function (T_r)	70×10^{-12}s

2) Selecting Parents and Making Offspring: We select parents from the pool made in the previous section. The lower the objective function value, the higher probability to be chosen as a parent is assigned. The probability for each line (p_{G}) varies from 0.05 (for the worst) to 0.55 (for the best). A random number in (0,1) is generated for each line in the pool, and the line is chosen as a member of the parent pool if the random number is less than p_{G}.

The line layouts of worse objective functions in a generation are erased. The probability to be erased (p_{B}) varies from 0.5005 (for the worst) to 0.0005 (for the best). A random number in (0,1) is again generated for each line, and the line is erased once it is less than p_{B}.

The newly born offsprings by the crossover substitute the erased ones to maintain the total number of lines in a generation. The crossover operation for delay lines is suggested, as shown in Fig. 5(a). The chosen two parents A and B are overlapped [the first step at "Child" procedure in Fig. 5(a)], and the overlapped cells of the same direction remain (the second). Next, following the path from the starting point along the remaining line, when we meet a cut, we select the direction of Parent A or Parent B randomly until we reach the ending point. Finally, we adjust the line length using the method in Section III-B1 if the length is changed.

3) Mutation: A geometric mutation method for the line layout, as described in Fig. 5(b), is considered as follows: We generate a random real number in (0, 1) at every cell along the line from the starting point and perform mutation if the number is under a mutation probability p_M (0.005 is chosen). When a mutation is determined, the

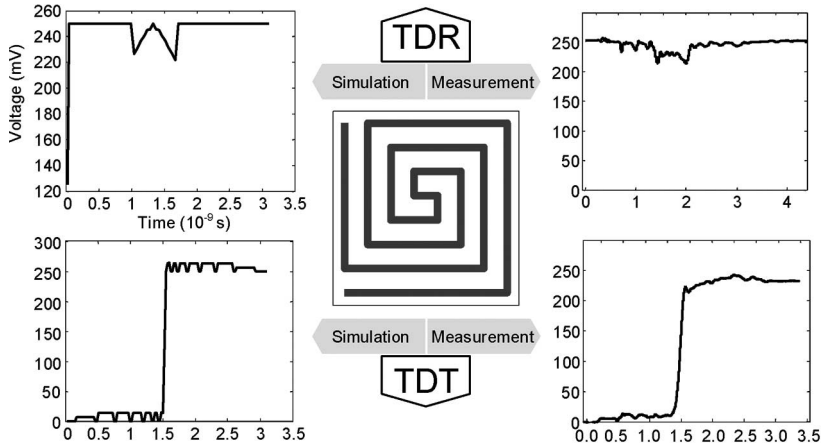

Fig. 6. Waveform of spiral delay line (P_t and V_r are minimized).

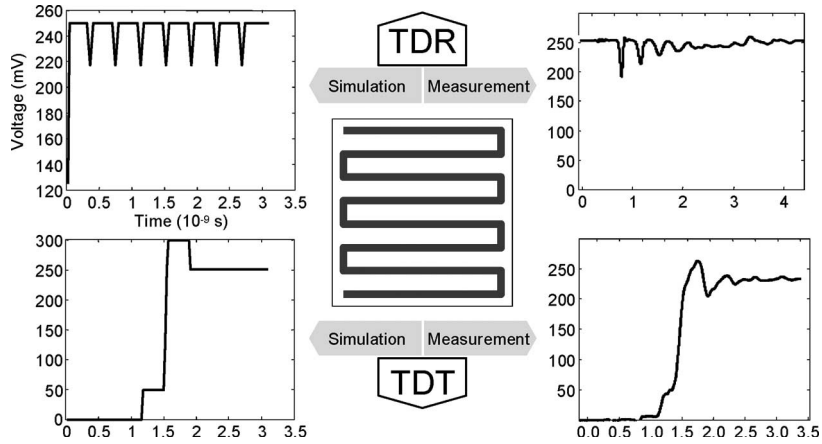

Fig. 7. Waveform of meander delay line (V_t is minimized).

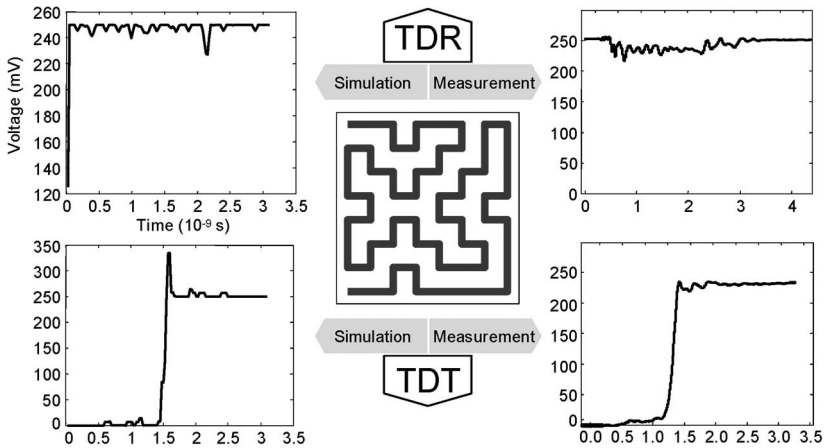

Fig. 8. Waveform of Dz delay line (A_t and A_r are minimized).

TABLE II
CHARACTERISTICS OF CROSSTALK FOR EACH LAYOUT BY SIMULATION

Line layout	Characteristic of crosstalk [a] (objective function highlighted)					
	P_t	V_t	A_t	P_r	V_r	A_r
Spiral	14.44	1014.1	1064.0	28.19	100.03	364.63
Meander	48.91	80.250	1369.6	32.90	1024.5	460.51
Dz	84.78	238.29	577.66	22.82	929.87	247.94
Pattern IV	126.93	149.72	847.94	6.04	1128.9	314.20

[a]Unit for Peak is mV, Variance (20 ps)^2, and Area mV×(20 ps).

direction changes randomly, and it is extended until the line joins the thread of the existing layout. Any disconnected lines from the mutation operation are removed. After the mutation, we again adjust the line length as explained in Section III-B1.

IV. OPTIMIZATION RESULTS

The proposed method has been applied to design a delay line with the following conditions: The cell size is 4 mm, line width is 1.92 mm, both C_{width} and C_{height} are 8, and z (the size of the population) is 100. The procedure in Section III-B is repeated 500 times. The conditions

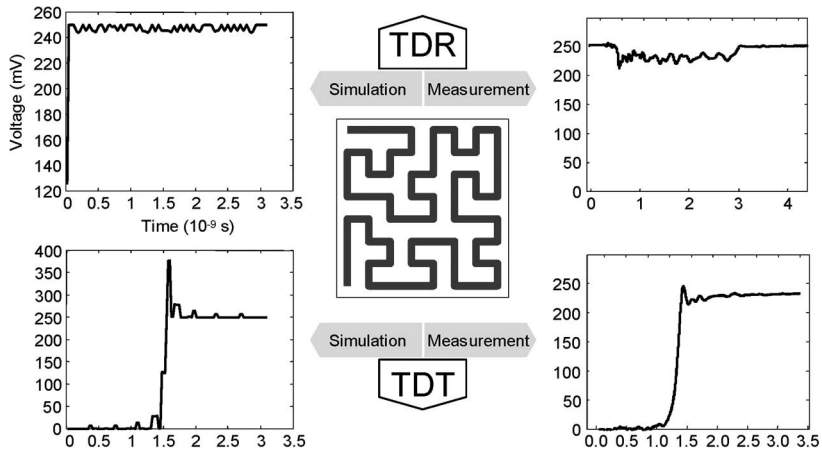

Fig. 9. Waveform of "Pattern IV" delay line (P_r is minimized).

TABLE III
MEASUREMENT OF PEAK VALUE FOR EACH LAYOUT

Line layout	P_t	P_r (mV)
Spiral	14.86	37.84
Meander	52.70	59.46
Dz	16.22	36.49
Pattern IV	9.46	32.43

for the crosstalk estimation and experimental measurement are listed in Table I. Three kinds of objective functions in (3) from TDT and TDR waveforms are chosen, and the results are explained in the following sections.

A. Crosstalk in TDT Waveform

P_t, A_t, and V_t of TDT waveform (the subscript t refers to the characteristic from TDT waveform) are chosen as the objective functions, and three different types of line layouts are obtained. Note that the lower left waveforms in Figs. 6–8 are discussed in this section. In minimizing P_t, a spiral delay line is obtained (Fig. 6), which is also suggested in [1] and [10]. The TDT waveform of the spiral line (the lower left one in Fig. 6) is interpreted as follows: As the line travels from the starting point and winds to the center, the parallel victim line sections are getting shorter, and this contributes to the shortening of widths of the rectangular type crosstalk as approaching the rising edge. When V_t is chosen to be minimized, the modified GA yields a meander line (Fig. 7), which is widely used in industries [1], [2], [10], [11]. The two rectangular waves before and after the rising edge in the TDT waveform in Fig. 7 denote an accumulation of the NE crosstalk at the preceding and the following victims, respectively.

In the case of minimizing A_t, on the other hand, we obtain a new layout not found in the literature; the line is zigzagging in a diagonal direction, as shown in Fig. 8. This new layout is therefore named as the "Dz delay line." The sharp peak in the TDT waveform in Fig. 8 is the result from the "U-turn" sections where the NE crosstalk is generated right after the step pulse (a total of 12 U-turn sections are found).

The simulation results for values of P_t, V_t, and A_t of the TDT waveform for each line layout are shown from the second to the fourth columns in Table II. For each characteristic, the optimal solution is highlighted, and the corresponding optimal layout is found from the first column. For example, for P_t, "14.44" is highlighted, and the optimal layout for minimizing P_t is "Spiral."

B. Crosstalk in TDR Waveform

The crosstalk at the starting point is calculated, and similar objective functions, P_r, V_r, and A_r, are considered for the TDR waveform (the subscript r refers to the characteristics from TDR waveform). In this section, the upper left waveforms in Figs. 6, 8, and 9 are discussed. For the layout where P_r is minimized, it is difficult to describe theline pattern (Fig. 9, named as "pattern IV" tentatively); the scattered U-turn sections contribute to the asynchronous accumulation of the crosstalk on the TDR waveform in Fig. 9. However, for either case where V_r or A_r is minimized, we obtain the same result as the case where P_t or A_t is minimized, respectively. When V_r is chosen as the objective function, the same spiral delay line is obtained with the opposite wound direction. The two valleys from TDR waveform in Fig. 6 come from the first half travel to the center and the second half travel to the ending point. We can conclude that P_t and V_r can be minimized simultaneously. For the minimization of A, the Dz delay line (Fig. 8) is obtained, showing that minimizing A at either TDT or TDR waveform is the same optimization task. The simulation results for P_r, V_r, and A_r of TDR waveform for the optimum layouts are shown in the last three columns in Table II.

V. MANUFACTURE OF CIRCUITS AND EXPERIMENTATION

The four types of line layouts, the meander line, the spiral line, the Dz line, and pattern IV, are manufactured, and the measured waveforms are compared with the simulation results in Section IV. A step function ($T_r = 70$ ps; $V_{\text{in}} = 250$ mV) is introduced from the starting point, and the TDT/TDR waveform is captured using an oscilloscope. The measured waveforms are shown in the right side of Figs. 6–9.

For the spiral line, the TDT/TDR waveform captured by the oscilloscope, which is shown in Fig. 6, proves that it is an optimal layout for the minimum P_t and V_r. The meander line shown in Fig. 7, which is obtained to provide the minimum V_t, reveals a similar waveform to the simulation. However, the triangular wave in the measured TDR waveform is getting lower and wider because of increasing T_r, which is not considered in the estimation. The newly found Dz line, corresponding to the minimum A_t and A_r, shows agreements between the simulation and the measurement, as shown in Fig. 8, except the sharp rise in the simulated TDT waveform, which is not observed in the measurement because of the low resolution of the oscilloscope. However, in the real measurement, the Dz line shows its excellence in conveying a step function to the ending point with

minimum crosstalk, which is the best TDT waveform among the four types of layouts. Pattern IV in Fig. 9 shows similar waves as the Dz line. A higher peak in the TDT waveform than the one from the Dz line is observed, although TDR waveforms are very similar to each other.

The measured peak values are listed in Table III for comparison with the simulations.

VI. Conclusion

The modified version of GA for the design of a delay line is introduced, and the optimal designs are verified by measuring crosstalk with manufactured PCB boards. Because GA requires a large number of function evaluations, a fast and efficient way of crosstalk calculation is proposed by discretizing the line into segments and superposing the crosstalk from each line segment. The methodology of making offsprings and mutation for the discretized line layout chromosome is suggested. The proposed GA has shown the excellence; we obtained the well-known layouts: the spiral and the meander layouts. In addition, a new layout named Dz layout was found for the minimum disturbance area of the unadulterated waveform. The optimum layouts are manufactured, and the measured waveforms were compared with the simulation results.

In calculating crosstalk, we have made simplifying assumptions, although a more elaborate model may be adopted: 1) The crosstalk is generated only at the parallel adjacent line, and 2) the rising time of the step function (T_r) is consistent until it travels to the ending point. The current version of the modified GA has an exponentially increasing time complexity as the PCB board size (C_{width} and C_{height}) increases. To alleviate this problem, a better scheme for the definition of chromosome (currently composed of 3 bits), as well as a fast-converging algorithm, is necessary.

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On Complete Functional Broadside Tests for Transition Faults

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***Abstract*—It was shown before that tests applied under nonfunctional operation conditions, which are made possible by scanning in an unreachable state, may lead to unnecessary yield loss. To address this issue, functional broadside tests were defined as broadside tests that use only reachable states of the circuit as scan-in states. Earlier procedures for generating functional broadside tests were not complete, i.e., they did not always detect all the detectable faults or prove that all the undetectable faults are undetectable. In this paper, we address the completeness of the functional broadside tests for transition faults. We describe the implementation of a test-generation procedure that can, for every transition fault, either find a functional broadside test or prove that the fault is undetectable under the functional broadside tests. We present experimental results where complete results are achieved for almost all the benchmark circuits considered.**

***Index Terms*—Functional broadside tests, overtesting, reachable state, scan, test generation.**

I. Introduction

The rapid increase in clock frequency of integrated circuits necessitates the detection of defects that affect the timing behavior of the circuit. Timing defects are typically modeled by delay faults. Transition faults are widely used as a delay-fault model. Test application methodologies for the delay faults in scan designs can be categorized into enhanced scan testing [1], skewed-load testing [2], and broadside testing [3]. All the techniques may suffer from unnecessary yield loss due to overtesting. Even broadside tests, which apply the second vector of every test in functional mode, may result in overtesting [4]. Overtesting for delay faults can be viewed in two ways. Under the first view, overtesting is due to the fact that redundant faults in the original circuit before scan insertion become detectable after scan insertion. It has been observed in [4] that detecting the redundant faults may lead to unnecessary yield loss, i.e., good chips may be discarded as faulty or placed in a lower performance bin due to the detection of a redundant fault. Under the second view, overtesting is caused by

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