On the Functional Failure and Switching Time Analysis of the MOBILE Circuit

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***Abstract*— Despite RTD-based MOBILE gates have been widely used in numerous relatively small high-performance digital circuits with a view to demonstrating their compact functionality and high speed of operational ability, MOBILE gates in general suffer from limited fan-out and driving capability. Therefore, in a large network of MOBILE gates the operating frequency and noise margins are severely impaired, resulting in an overall poor performance as well as reliability. This paper discusses the failure mode and the switching time of a MOBILE circuit through analysis of circuit operation by representing the electrical characteristics of the RTD with a simplified piecewise linear model. The paper also verifies the analytical results through circuit simulation performed with the University of Michigan Quantum Spice simulator. This augmented Spice incorporates the quantum physics based RTD model and appropriate convergence routines to overcome the non-monotonic nonlinearity of MOBILE circuits. The paper has also shown how to derive the optimal rising time of the clocked supply in a given MOBILE circuit. In order to guarantee the logic function of a MOBILE circuit, its device sizes must be made smaller than the critical values that primarily depend on the fabrication technology and the MOBILE circuit configuration.**

I. Introduction

Resonant tunneling diodes (RTD's) have been identified as promising nano-scale devices for high speed and compact circuit implementation due to their pico-second switching speed and unique negative differential resistance (NDR) characteristics [1]. The monostable-bistable logic element (MOBILE) [2] gates, consisting of a pair of series connected RTD's and transistors, are special logic gates which have found wide applications in compact logic families as well as high-speed circuits. However, the operating speed of MOBILE's is not as fast as the switching time of RTD's since it is limited by a critical rising time of the clocked supply due to currents flowing through RTD's capacitance [3]. Several researchers have attempted to estimate the switching speed of the MOBILE gate with simplified I-V characteristics of RTD's by means of numerical and analytic methods [4]-[7]. However, few efforts have been made to investigate the impact of real-world parasitic components such as parasitic contact resistance of RTD's and the parasitic capacitance of embedded transistors. Moreover, no systematic research has been done to study the relationship between the functional failure of MOBILE gates and the dimensions of RTD's, area ratio of the RTD-pair, contact resistance, loading capacitance and the rising time of the clocked supply. In this paper, we investigate the afore-mentioned issues through simulation. The functional failure modes and the switching time of the MOBILE circuitry are then modeled to provide circuit designers with some useful design strategies.

II. Operation Principle of an Ideal RTD-Pair

A pair of series connected RTD's constitute basic component in MOBILE gates. If the RTD-pair is driven by a clocked supply, its output state, determined by the sizing of two RTD's, is evaluated at the rising edge of the clock pulse and it is latched while the clock is active high. Understanding the function of an ideal RTD-pair is the first step to investigate the principle of operation of more complex MOBILE structures that contain parasitic contact resistors of RTD's, parallel connected transistors and the load capacitor.

A. Proposed Model for an Ideal RTD-Pair

The circuit model of an ideal RTD-pair is shown in Fig. 1(a), where each RTD is modeled by its intrinsic capacitor and a parallel-connected voltage controlled current source representing the I-V characteristics of RTD's. To simplify the analysis, the RTD's I-V curve is modeled with a piecewise linear function, assuming that RTD acts as a normal resistor in the first and second positive differential resistance (PDR) regions and a resistor with a negative value in the negative differential resistance (NDR) region. It is observed that at the onset of the rising edge of the clock pulse, both drive and load RTD's (referred as bottom and top RTD's in the following text) are biased in the first PDR region; the output state is then determined once one of them is biased into the NDR region. While both RTD's are biased in the first PDR region, the ideal RTD-pair can be modeled by using simple RC circuits as shown in Fig. 1(b). It is known that the intrinsic capacitance of the RTD is proportional to the area of the RTD while the resistance is inversely proportional to the area since the peak current, I_P, scales linearly with the RTD's area and the peak voltage, V_P, remains the same for a certain fabrication process. Now, let the area of the bottom and the top RTD be A and KA, where K is the area ratio of the top RTD to the bottom RTD. The capacitance and resistance for the bottom and the top branch, thus, are denoted as AC_{RTD-U}, R_{P1-U}/A, and KAC_{RTD-U}, $R_{P1-U}/(KA)$, respectively, where C_{RTD-U} and

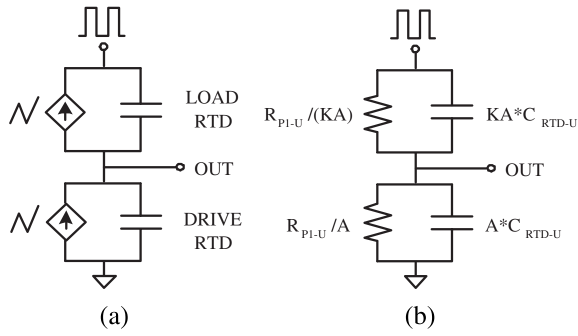

Fig. 1. Circuit model of an ideal RTD-pair under (a) any biasing condition and (b) the first PDR region biasing condition.

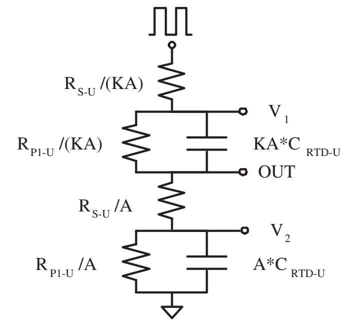

Fig. 2. Circuit model of an RTD-pair with parasitic contact resistance biased in the first PDR region.

R_{P1-U} are the capacitance and resistance of an RTD with unit area biased in the first PDR region.

B. Analysis for Operation Principle

At the beginning of the rising of the clock, the circuit behavior can be derived by solving the following ordinary differential equation,

$$KA * C_{RTD-U} * \frac{d(V_{CLK}(t)-V_{OUT}(t))}{dt} + \frac{V_{CLK}(t)-V_{OUT}(t)}{R_{P1-U}/(KA)}$$
$$= A * C_{RTD-U} * \frac{dV_{OUT}(t)}{dt} + \frac{V_{OUT}(t)}{R_{P1-U}/A}$$

Let the high level, rising time, and slew rate of the clock supply be V_{DD}, T_{RS}, and S. Thus, $S = V_{DD}/T_{RS}$ and $V_{CLK}(t) = S * t$. Thus, this ODE simplifies to:

$$\frac{dV_{OUT}}{dt} + \frac{V_{OUT}}{C_{RTD-U}R_{P1-U}} = \frac{K}{K+1}S\left(1 + \frac{t}{C_{RTD-U}R_{P1-U}}\right)$$

Its solution is $V_{OUT}(t) = \frac{K}{K+1}St$. The voltage drops on the bottom and the top RTD biased in the first PDR region are $\frac{K}{K+1}St$ and $\frac{1}{K+1}St$, respectively. As long as both RTD's are biased in the first PDR region, the current flowing through the bottom RTD's capacitor is equal to that in the top RTD's capacitor; current in the bottom RTD's resistor is equal to that in the top RTD's resistor since

$$AC_{RTD-U} * d \quad \frac{K}{K+1}St \quad /dt = KAC_{RTD-U} * d \quad \frac{1}{K+1}St \quad /dt$$
$$\frac{K}{K+1}St \quad \frac{R_{P1_U}}{A} = \frac{1}{K+1}St \quad \frac{R_{P1_U}}{KA}$$

If the top RTD is larger than the bottom RTD, i.e., K>1, the bottom RTD enters the NDR region earlier than the top RTD, thereby making the current flowing through the bottom RTD's resistor (now R_{N-U}/A) decrease and that in the top RTD's resistor keep increasing. The difference current resulting from the current mismatch in two resistors is then pushed into two capacitors at the output node according to the current dividing principle. Hence, the charging speed of the bottom RTD's capacitor is increased while that of the top RTD's is reduced, resulting in high state at the output node. The difference current exists until currents in both resistors are matched, which occurs once clock becomes high or at a later time. We define the period from the onset of the rising edge of the clock to the disappearance of the difference current as the switching time of MOBILE, T_{SW}.

Whether T_{SW} is equal to or larger than T_{RS} depends on the relationship between the original capacitor's displacement current level and the difference current level. If the slew rate is so large (e.g., very small T_{RS}) such that the displacement current is much larger than the difference current, the top and the bottom RTD's capacitors have similar charging speed throughout the rising phase of the clock, resulting in the output voltage being equal to $\frac{K}{K+1}V_{DD}$ at t=T_{RS}. After the rising of the clock, the displacement current disappears while the difference current keeps charging and discharging the capacitors. The steady output state, then, is obtained after this difference current vanishes. On the other hand, if the displacement current is comparable to the difference current, the final output voltage is obtained at t=T_{RS}.

III. Functional Failure of MOBILE Circuitry

The output state of the MOBILE gate may be incorrect if several non-ideal effects are not considered. We will investigate the afore-mentioned issues in this section.

A. Impact of Parasitic Contact Resistance

The parasitic contact resistance is represented by a series connected resistor, R_S, in the model as shown in Fig. 2. With R_S, the charging speed now is governed by the RC time constant on the charging path while it is unlimited when R_S=0. The maximum displacement current is $V_{CLK}/(R_{S-top} + R_{S-bottom})$, which no longer depends on the slew rate. However, R_S not only degrades the switching speed but also causes a functional failure if its value is too large. In such case, the voltage drop on R_S may be larger than that on the capacitor given a certain displacement current. Hence, the output voltage is around $\frac{K}{K+1}V_{CLK}$ due to the voltage division of two R_S, $R_{S-U}/(KA)$ (top) and R_{S-U}/A (bottom), where R_{P1} can be ignored.

1) Transient behavior at clock's rising edge: Transient response of the RTD-pair with R_S can be found by solving the following ODE's,

$$KA * C_{RTD-U} * \frac{d(V_1 - V_{OUT})}{dt} + \frac{V_1 - V_{OUT}}{R_{P1-U}/(KA)}$$
$$= A * C_{RTD-U} * \frac{dV_2}{dt} + \frac{V_2}{R_{P1-U}/A} = \frac{V_{CLK}-V_1}{R_{S-U}/(KA)} = \frac{V_{OUT}-V_2}{R_{S-U}/A}$$

Due to $i_{C-bottom} = i_{C-top}$ and $i_{R-bottom} = i_{R-top}$ with the same reason in the ideal RTD-pair, $(V_1 - V_{OUT})/V_2 = 1/K$,

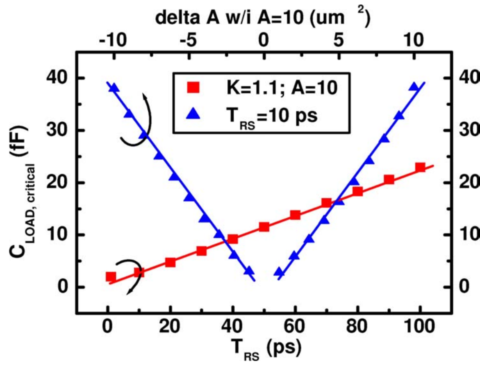

Fig. 3. Dependence of CLOAD,critical on TRS and delta A.

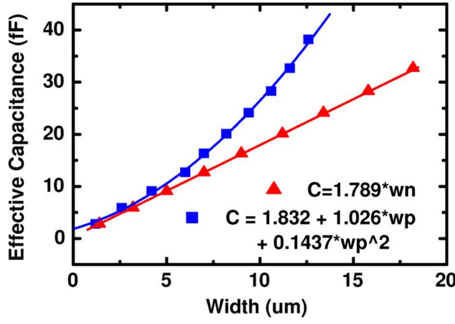

Fig. 4. Extracted output-node-to-ground parasitic resistance of N-type and P-type FET's in the bottom branch as a function of transistor width.

i.e., $V_1 = (K/(K+1)) * V_{CLK} + 1/K * V_2$. These ODE's then become:

$$\frac{dV_2}{dt} + \frac{1}{C_{RTD-U}}\left[\frac{1}{R_{P1-U}} + \frac{1}{R_{S-U}}\right]V_2 = \frac{K}{K+1}\frac{St}{R_{S-U}}$$

The solution V2 is given below:

$$V_2 = \frac{KS}{K+1}\frac{C^2_{RTD_U}R^2_{P1_U}R_{S_U}}{(R_{P1_U}+R_{S_U})^2} \quad e^{-\frac{R_{P1_U}+R_{S_U}}{C_{RTD_U}R_{P1_U}R_{S_U}}t} - 1$$

$$+\frac{KS}{K+1}\frac{C_{RTD_U}R_{P1_U}}{R_{P1_U}+R_{S_U}}t$$

2) Failure Criteria: The MOBILE gate functionality fails when the voltage drops on both RTD's capacitors are smaller than V_P at $t = T_{RS}$, resulting in output voltage being equal to $\frac{K}{K+1}V_{DD}$. Hence, the failure criteria can be found by replacing t with T_{RS} into the previously derived formula and making it equal to or less than V_P. Another approach is to solve the following equation:

$$\frac{I_{C,RTD} * T_{RS}}{C_{RTD}} < V_P$$

,which can be approximated by the following equation:

$$\frac{V_{DD}}{(1+\frac{1}{K})(1+R_{S_U}(\frac{C_{RTD_U}}{T_{RS}}+\frac{1}{R_{P1_U}}))} < V_P$$

It is observed that if T_{RS} is longer than 1 ps, $C_{RTD-U}/T_{RS} \ll 1/R_{P1-U}$ due to $C_{RTD-U} \simeq 0.75$ fF and $R_{P1-U} \simeq 1.4$ kΩ. Hence,

$$R_{S_U,critical} \approx R_{P1_U} \quad \frac{V_{DD}}{(1+\frac{1}{K})V_P} - 1$$

Under the normal bias condition, V_{DD} ranges from 1V to 2V and 1/K<1. With R_{P1-U} 1.4 kΩ in our model, $R_{S-U,critical}$ is around 4 kΩ, which is much larger than the value the fabrication technology can achieve. Hence, the impact of the contact resistance on the functionality of MOBILE circuitry can be ignored when T_{RS} is longer than 1 ps. However, if T_{RS} is much smaller than 1 ps, $R_{S-U,critical}$ is derived as,

$$R_{S-U,critical} \approx \frac{T_{RS}}{C_{RTD_U}} \quad \frac{V_{DD}}{(1+\frac{1}{K})V_P} - 1$$

B. Impact of Loading Effect Capacitance

MOBILE circuits experience serious loading effects due to their operation of charging and discharging the small intrinsic capacitors of RTD's. Loading effects result from the gate capacitance in the following stage and the drain to body or source to body junction capacitance of parallel-connected transistors. With the loading effect capacitance, C_{LOAD}, connected between the output node and ground, the output of MOBILE goes to low more easily since the displacement current in the top RTD's intrinsic capacitor must increase to compensate the additional displacement current for C_{LOAD}. Therefore, the charging speed of the top RTD's capacitor is increased, forcing the top RTD to enter NDR region first, thus generating low output state even if K>1. On the contrary, if K<1 and C_{LOAD} is parallel-connected with the top RTD, the output goes to high state more easily.

1) Failure Criteria: C_{LOAD} should be smaller than a certain value, $C_{LOAD,critical}$, to ensure correct output state. Fig. 3 shows the simulation results of $C_{LOAD,critical}$ depending on T_{RS} and the area difference of two RTD's, delta A (i.e., $|K-1|A$). As can be seen, as T_{RS} increases, $C_{LOAD,critical}$ increases almost linearly due to the decreased displacement current in C_{LOAD}. On the other hand, given fixed T_{RS}, $C_{LOAD,critical}$ is proportional to delta A. Based on the simulation results, $C_{LOAD,critical}$ can be modeled as,

$$C_{LOAD,critical} = 0.218A|K-1| * T_{RS} \quad (fF)$$

2) Parasitic capacitance extraction of parallel connected transistors (CMOSFET's used here) : The procedure for extracting the equivalent C_{LOAD} of FET's is to search the critical width of FET's that causes a functional failure when the FET's are off, i.e., the input signal is low. For a certain design of RTD-pair (fixed K, A and T_{RS}), the FET with the critical width has parasitic capacitance equal to its corresponding $C_{LOAD,critical}$, which has been found in the last section. Observed from the simulation results, FET's in the top and the bottom branch generate parasitic capacitance between the output node and the supply node and the output node and the ground accordingly. Fig. 4 shows the extracted effective capacitance as a function of FET's width when only one FET is connected in the bottom branch. As can be seen, the relationship between the effective capacitance and FET's width is linear in N-FET's while is quadratic in P-FET's. This may be due to the asymmetric fabrication process and the biasing condition of P-type and N-type FET's. Note that the capacitance is independent on FET's length since it does not relate to junction capacitors. The maximum width for FET's at the bottom branch is modeled as,

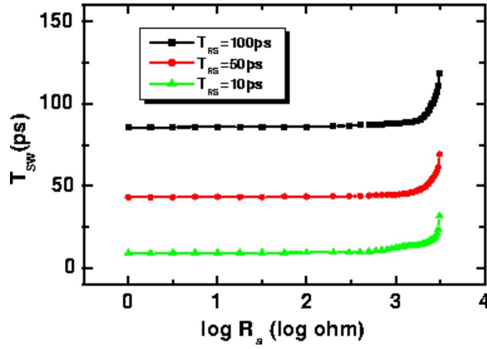

Fig. 5. Dependence of the switching time on RS with three different TRS for the RTD-pair with K=1.1 and A=10.

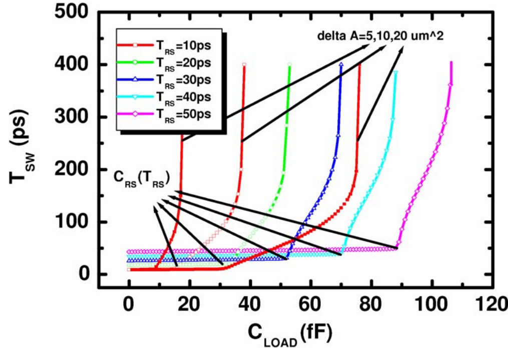

Fig. 6. Dependence of TSW on CLOAD for five different TRS with K=2 and A=10 (colorful lines) and for three delta A design with TRS=10ps (red lines).

$$wn_{max} = \frac{0.81A(K-1)}{1.798} * \frac{T_{RS}}{10p}\ (um)$$

$$wp_{max} = 3.57\left[\left(1 - \frac{0.81A(K-1)}{1.798} * \frac{T_{RS}}{10p}\right)^{0.5} - 1\right]\ (um)$$

Similar approach can be applied to derive the maximum width for FET's at the top branch.

IV. Switching Time Estimation

Switching time, T_{SW}, of MOBILE usually consists of two parts: the rising time of the clock, T_{RS}, and the settling time, T_{ST}, defined as the extra time for achieving the steady output state after clock remains active high. In some cases, output state is obtained at the end of T_{RS}, thus T_{SW}=T_{RS} and T_{ST}=0.

A. Impact of Parasitic Contact Resistance

Since R_S may cause functional failures, it affects T_{SW}. The simulation results in Fig. 5 demonstrate the relationship of T_{SW} and R_S for three T_{RS} values. Note that T_{SW} is measured when the output voltage is 90% of its final value. As can be seen, the rising trend of T_{SW} for different T_{RS} is similar but shifted whenever $T_{SW} > 1ps$. Thus, the dependence of T_{SW} on R_S can be modeled as:

$$T_{SW} = 0.9T_{RS} + 0.017 * \exp\ \frac{\log R_{S-U} + \log(K+1/1.91K) - 2.637}{0.12}$$

B. Impact of Load Capacitance

Fig. 6 shows the simulated T_{SW} for various A and K design, delta A equal to 5, 10, 20 μm^2 (Red Lines), and for different T_{RS} (Color Lines). An interesting observation is that given the same T_{RS}, the curves have the same waveform, but expanded in the x-axis with a factor proportional to delta A. However, waveforms are different for the same RTD-pair with different T_{RS}, but the onset of the rapid growth of T_{SW} for different T_{RS} is roughly proportional to T_{RS}. We call the onset point C_{RS}, which plays a very important role in choosing the optimal T_{RS} for MOBILE circuitry. For example, the MOBILE with K=2, A=10, and C_{LOAD} =40 fF has its optimal T_{RS} around 22 ps rather than any value smaller than 22 ps since T_{ST} grows rapidly for the latter choice. The dependence of T_{RS} on C_{LOAD} can be modeled as following:

$$T_{SW} = 0.9T_{RS} \quad if\ C_{LOAD} < C_{RS}$$

$$T_{SW} = 0.9T_{RS} + f(T_{RS}, C_{LOAD}/\delta)\ if\ C_{RS} < C_{LOAD} < C_{LOAD,critical}$$

, where $C_{RS} = 18.4\delta\alpha\ (fF)$, $\delta = |K-1|A/10$, $\alpha = T_{RS}/10p$ and f(.) is a monotonically increasing exponential-like function.

V. Conclusion

This paper investigates the operation principle of a RTD-pair using a simplified circuit model. The switching time of the MOBILE circuit as well its functional failure mode has been derived by a new analytical method and the analytical results have been verified by performing Quantum-SPICE simulation with physics-based model of the RTD. It has been found that the impact of contact resistance can be ignored in the present fabrication technology. Loading effects of the MOBILE gate can be well controlled by appropriately sizing the RTD, selecting the area ratio of the RTD-pair, choosing the width of parallel-connected FET's, and adjusting the rise time of the clock pulses. Therefore, given a certain application that requires a specific MOBILE design, there will be an optimal rise time of the clock pulses. Derivation of these parameters is the main contribution of this paper.

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