A 20 Gb/s 1:4 DEMUX Without Inductors and Low-Power Divide-by-2 Circuit in 0.13 μm CMOS Technology

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Abstract—In this paper, a 20 Gb/s 1:4 DEMUX without inductors is presented. A coupled latch with shared current source and buffer insertion scheme improves the signal bandwidth. A divide-by-2 circuit with a static frequency divider and a delay-locked loop achieves low power consumption and enhanced timing margin without the degradation of the divider sensitivity. A horizontal eye opening is 71.3%, and a vertical eye opening is 52%. The test chip fabricated in a 0.13 μm process consumes 210 mW from 1.2 V logic supply.

Index Terms—CMOS, DEMUX, delay-locked loop (DLL), latch, static frequency divider.

I. INTRODUCTION

In recent years, high-speed communications systems beyond 10 Gb/s have been realized in CMOS technology. The MUX and DEMUX ICs are challenging building blocks for high-bandwidth systems. Synchronous Optical NETwork (SONET) standard and Ethernet standard for 10 Gb/s and above serial links have promoted developments of the CMOS transmitter and receiver including a CDR and MUX/DEMUX [1]–[3]. Several works have reported 10 Gb/s inductorless DEMUX ICs in 0.18 μm CMOS process [4], [5]. In this paper, a 20 Gb/s 1:4 DEMUX in 0.13 μm CMOS is presented. This design uses no inductive peaking, which reduces area, and a 1.2 V logic supply, which reduces power consumption. A coupled latch and buffer insertion scheme increases the signal bandwidth at the 20 Gb/s data rate [6]. A divide-by-2 circuit uses a delay-locked loop (DLL) to align the clock output of the frequency divider with the data center of the 1:2 DEMUX output. This design reduces the power consumption of the power-hungry divider and improves the timing margin.

Fig. 1 shows structures of a conventional 1:4 DEMUX. Cascaded buffers can be inserted in the divided-clock path to reduce the loading capacitance on the divider output as shown in Fig. 1(b). The divider can operate at higher frequencies while avoiding large sizing. The cascaded buffers should be added in the Even and Odd paths to align with the divide-by-2 clock. However, when the data and the clock pass through several buffers, the timing margin between them is degraded.

Fig. 1. Conventional structures of 1:4 DEMUX. (a) Basic DEMUX. (b) DEMUX with cascaded buffers.

Fig. 2. Proposed 1:4 DEMUX.

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II. ARCHITECTURE DESIGN

A. 1:4 Demux Design

Fig. 2 shows the proposed 1:4 DEMUX. Since the 1:4 DEMUX operates with a half rate clock, it needs a 10 GHz input clock for the 20 Gb/s data rate. The divide-by-2 circuit includes a frequency divider and DLL. The sensitivity of the divider is improved because of small capacitive load on the divider output. The DLL synchronizes the negative edges of \( CLK_{in} \) (10 GHz) with the positive edges of \( CLK_{fb} \) (5 GHz). The DLL output signal needs buffers to have a large enough driving capability to drive many latches in the 2:4 DEMUX. To align the \( CLK_{out} \) with the center of \( D_{even} \) and \( D_{odd} \), a buffer whose delay corresponds to the \( C-Q \) (clock-to-out) delay of the 1:2 DEMUX is added in front of the clock input of the 2:4 DEMUX. The \( C-Q \) delay buffer in Fig. 3 is the replica circuit of the coupled latch and inserted buffer. The transistor size of \( M1-M5 \) is proportional to the size of nMOS in the read part. \( M6-M9 \) exhibit the drain and gate capacitances of the cross-coupled nMOS pair in the hold part. The drain and source of \( M8 \) and \( M9 \) are tied to \( (V_A + V_B)/2 \) to provide more accurate gate capacitance. \( R1 \) and \( R2 \) have large resistance to minimize the interaction between \( V_A \) and \( V_B \). The replica for the coupled latch may have a slight different output common mode voltage from the coupled latch because it replicates the operation in the read mode. However, the delay of the \( C-Q \) delay buffer is almost the same as the \( C-Q \) delay of the 1:2 DEMUX because a little variation of the output common mode exhibits a minor effect on the \( C-Q \) delay. The 1:2 DEMUX improves the operation speed with the proposed coupled latch and buffer insertion scheme, and the 2:4 DEMUX uses a conventional latch for low power because it is fast enough for the 10 Gb/s data rate.

Fig. 4 depicts the timing diagram of the 1:4 DEMUX. The \( D_{even} \) and \( D_{odd} \) are 1:2 demultiplexed outputs of \( D_{in} \). They are delayed from \( CLK_{in} \) by \( C-Q \) delay. The DLL output \( CLK_{fb} \) is synchronized with the negative edge of \( CLK_{in} \). The \( CLK_{fb} \) should be delayed by \( C-Q \) delay to generate the divide-by-2 clock \( (CLK_{out}) \) aligned with the center of \( D_{even} \) and \( D_{odd} \).

The 2:4 DEMUX generates 5 Gb/s D0 to D3 with better timing margin.

B. DLL Design

The DLL architecture is shown in Fig. 5(a). The output clock of the DLL is controlled by analog phase interpolation using four phases (\( Q, I, Q, I \)) based on the divider outputs [7]. The D-flip-flop type phase detector in Fig. 5(b) is used to operate at high frequency. The 5 GHz \( CLK_{fb} \) samples the 10 GHz \( /CLK_{in} \) to indicate “early” or “late”. To achieve an unlimited phase shift of \( 2\pi \) in the phase interpolator, the phase selector monitors the boundary of \( V_C \) and controls the MUX output and the current direction of the charge pump through the polarity checker. Fig. 5(d) shows the phase selector. The latch is used as the comparator. The buffer is inserted in front of the latch to minimize the kick-back effect, and it provides the amplification of the voltage difference between \( V_C \) and \( V_{pf} \). Comparators need the high-frequency input clock (\( I \) and \( Q \) signals) for fast operation speed. Dividers triggered by the output signal of the comparator generate the \( sel_I \) and \( sel_Q \) signals. The polarity checker outputs the polarity signal which controls the charging and discharging path of UP and DN currents in the charge pump. Fig. 6 shows the timing diagram of the DLL. The DLL uses small transistors to minimize its power consumption.
As implemented, the DLL draws a total current of 2 mA excluding cascaded buffers.

\[ \text{C. Coupled Latch and Buffer Insertion Scheme} \]

Fig. 7 describes the structure of the proposed 1:2 DEMUX. The 1:2 DEMUX is located in front of the 2:4 DEMUX. It has three stages. In one stage, two latches are coupled with shared current sources. The \( I_{\text{read}} \) and \( I_{\text{hold}} \) of the coupled latch (CL) are equal to \( I_{\text{up}} + \alpha \) and \( I_{\text{up}} - \alpha \), respectively. This design is similar to the asymmetrical latch in [8]. However, in the proposed coupled latch the read and hold parts have different current sources to fully steer the current in each mode. The sizing of transistors in the read and hold parts is simple because they can have the size proportional to the amount of the current source. The different allocation of \( I_{\text{read}} \) and \( I_{\text{hold}} \) improves the operation speed in read mode, and the latch has less delay. However, the reduced output swing in hold mode may degrade the operating speed of the latch in the next stage. The buffer is inserted to enhance the transition of the output signal. The third stage includes a dummy latch for the coupled latch structure.

Fig. 8 shows four types of the latch structure and their frequency responses of \( D_{\text{in-to-out}} \). In this design, the \( I_{\text{read}} \).
The simulation result of frequency responses in Fig. 8(e) demonstrates the effectiveness of the coupled latch structure and the buffer insertion scheme. While the latch and the CL have a slope of $-20$ dB/decade, the latch + buffer and the CL + buffer have a slope of $-40$ dB/decade due to an additional pole of the buffer. The buffer insertion scheme increases the DC gain of output signal by 4.13 dB on the average. The coupled latch structure enhances it by 1.62 dB on the average. The CL buffer structure increases the gain at DC by 5.75 dB and the gain at 10 GHz by 3.8 dB. It is effective to extend the gain in the target bandwidth without inductors.

When the 1:2 DEMUX uses the conventional latch whose current source draws $I_o$, its current consumption is $5I_o$ because it uses five latches. In the 1:2 DEMUX with the CL + buffer, a stage draws $4I_o$ because it has four current sources of $I_{\text{read}}$, $I_{\text{hold}}$, and $2I_o$. The total current consumption of 1:2 DEMUX with the CL + buffer is equal to $11I_o$ ($=12I_o-I_o$, the dummy CL does not have the buffer). The proposed 1:2 DEMUX draws 2.2 times larger current than the conventional 1:2 DEMUX does. The increased power consumption of the proposed 1:2 DEMUX comes from inserted buffers.

Fig. 9 describes the timing diagram of the CL + buffer. When the CL + buffer is in the read mode, the latch can change its output promptly because of the large $I_{\text{read}}$ and less loading capacitance of small transistors in hold part. The latch holds the output weakly with a reduced swing in the hold mode. The reduced swing allows the fast transition of the latch output when the latch is entering the read mode. The output of the buffer has a sharper rising and falling time. The $C\cdot Q$ delay of CL + buffer is similar to that of a conventional latch because the coupled latch has lower delay than the conventional latch does. Although the $C\cdot Q$ delay of the CL + buffer is similar to that of a conventional latch, it can operate at a higher bit rate due to the decreased transition time of the buffer output. Since the output edge of the CL + buffer is fast enough, the maximum operating data rate is mainly limited by the $C\cdot Q$ delay. The $C\cdot Q$ delay of the stage must be less than 50 ps for correct operation at 20 Gb/s.
D. Divide-by-2 Circuit Design

Fig. 10(a) shows the static frequency divider in the conventional DEMUX. The latch of the divider ($I_{\text{div}}$) has large size to drive 10 latches in the 2:4 DEMUX. Latches in the 2:4 DEMUX use the current of $I \times I_{\text{min}}$ where $I$ is the normalized latch size and $I_{\text{min}}$ is the minimum amount of the current source in the current-mode logic (CML). In this design, the $I_{\text{min}}$ is 150 $\mu$A. To prevent the degradation of the divider sensitivity due to many latches of 2:4 DEMUX, the current of the $I_{\text{div}}$ is larger than the total current used in 2:4 DEMUX. When the ratio of the $I_{\text{div}}$ current to its load current is $K$, the $I_{\text{div}}$ uses the current of $K \times 10 \times I \times I_{\text{min}}$ because its load corresponds to 10 latches of 2:4 DEMUX. The total current of the divider is given by

$$2 \times I_{\text{div}} = 2 \times K \times 10 \times I \times I_{\text{min}} = 2 \times K \times 150 \mu A = 3 \times K \times L \text{ (mA)}.$$  

(1)

In Fig. 10(b), the divider drives small clock buffers to reduce its current consumption. The divide-by-2 clock signal needs cascaded buffers to have more driving power. Cascaded buffers are also inserted in the $D_{\text{even}}$ path and $D_{\text{odd}}$ path to remove the delay difference between the data and the clock. In the cascaded buffers, the current ratio between adjacent buffers is 2 for adequate transition time of each buffer. For proper timing margin with fast slope of the divided clock, the buffer of the final stage is sized to have larger current than the total current of 2:4 DEMUX. The first buffer in cascaded buffers uses the current
of $I_{\text{min}}$. In the divided clock path, $D_{\text{even}}$ path, and $D_{\text{odd}}$ path, the total current of cascaded buffers is as follows:

$$3 \times I_{\text{min}} \times (1 + 2 + \cdots + 2^{n-1}) = 3 \times I_{\text{min}} \times (2^n - 1)$$

(2)

where $n$ is the number of buffers. Since the current used in the final buffer should exceed the total current of 2:4 DEMUX, the number of buffers is defined by following inequality:

$$I_{\text{min}} \times 2^{n-1} \geq 10 \times L \times I_{\text{min}}$$

$$n \geq \log_2 10L + 1.$$  

(3)

Since the divider drives the small buffer of the minimum size, the $I_{\text{SY}}$ has the current of $K \times I_{\text{min}}$. The total current of the divider and cascaded buffers is given by

$$I_{\text{total}} = I_{\text{min}} \times (2 \times K + 3(2^n - 1))$$

$$I_{\text{total}} \geq I_{\text{min}} \times (2K - 3 + 3 \times 2 \log_2 10L + 1)$$

$$I_{\text{total}} \geq 150 \mu\text{A} \times (2K - 3 + 60L)$$

$$I_{\text{total}} \geq 0.45 + 0.3K + 9L \text{ (mA)}.$$  

(4)

In the proposed structure in Fig. 10(c), the divider drives two small buffers with the current of $I_{\text{min}}$. Two small buffers may generate offsets due to the device mismatch. However, their effect on the divider sensitivity is negligible because of large divider size ($L_{\text{clk}}$). Although the $I/Q$ mismatch due to the offsets of two buffers may deteriorate the linearity of the phase interpolator, the DLL at lock can resolve the static $I/Q$ mismatch and provide the well-aligned output clock. The final stage in the cascaded buffers is the $C\cdot Q$ delay buffer. Since the $C\cdot Q$ delay buffer in Fig. 3 has two current sources, the total current of cascaded buffers including the $C\cdot Q$ delay buffer is as follows:

$$I_{\text{min}} \times (1 + 2 + \cdots + 2^{n-1} + 2^{n-1})$$

$$= I_{\text{min}} \times (2^n - 1 + 2^{n-1})$$

$$= I_{\text{min}} \times (3 \times 2^{n-1} - 1).$$  

(5)

If the 1:2 DEMUX uses the conventional buffer but not the $C\cdot Q$ delay buffer has one current source and the total current of cascaded buffers becomes $I_{\text{min}}(2^n - 1)$. The implemented DLL draws 2 mA. The total current of the divider, two small buffers, cascaded buffers, and DLL is given by

$$I_{\text{total}} = I_{\text{min}} \times (2 \times K + 2 \times 1 + 3 \times 2^{n-1} - 1) + I_{\text{DLL}}$$

$$I_{\text{total}} \geq 150 \mu\text{A} \times (2K + 1 + 3 \times 2 \log_2 10L) + 2 \text{ mA}$$

$$I_{\text{total}} \geq 150 \mu\text{A} \times (2K + 1 + 30L) + 2 \text{ mA}$$

$$I_{\text{total}} \geq 2.15 + 0.3K + 4.5L \text{ (mA)}.$$  

(6)

Fig. 11 shows the graph of the current consumptions of (1), (4), and (6) as a function of the normalized latch size ($L$) and the ratio of the $I_{\text{clk}}$ current to its load current ($K$). When three dividers have the same divider sensitivity, the proposed structure is the most efficient for low power consumption.

Fig. 12 shows the static frequency divider, which consists of coupled latches and buffers. The graph in Fig. 13(a) shows the simulated sensitivity curves of three static dividers. Although the divider using only the CL can operate at higher frequencies, it needs a larger input swing for correct operation. It loses
As the supply voltage is generated by a voltage divider consisting of a series set 2. Although and the bias voltage rise. The CML circuits increases, the degradation of the sensitivity is 1 PRBS signals. The pulse pattern generator (PPG) generates of 16 for more robust current to its load current. Dashed lines indicate the buffer allows a larger output swing due to its larger buffer does. However, the divider with self-resonance can be occurred with a sufficient small-signal gain for oscillation build-up. Although the divider based on CL self-resonance can be avoided due to additional phase shift and increased gain by inserted buffers. Its sensitivity is shifted to a slightly lower frequency than that of the conventional latch, because the conventional latch has a little lower input-to-output latency than the CL + buffer does. However, the divider with the CL + buffer allows a larger output swing due to its larger gain. Fig. 13(b) shows the output voltage swing as a function of the input frequency. Output voltage swings are simulated with the input clock of 0.4 Vpp (single-ended). To ensure that the divider in the chip will operate at 10 GHz, its sensitivity and output swing must be optimized in the range from 8 GHz to 15 GHz. In this frequency range, the divider based on the CL + buffer has the best simulation results. Since the divider only drives a small capacitive load as shown in Fig. 10(c), it almost achieves the sensitivity shown in Fig. 13(a). As a result, it is possible to avoid large power consumption in the divider at clock frequencies above 10 GHz. Fig. 14 shows the self-oscillation frequency of the divider output according to the ratio (K) of the Ldiv, current to its load current. Dashed lines indicate the self-oscillation frequencies when the divider output has no load. As the ratio (K) increases, the degradation of the sensitivity is reduced. The self-oscillation frequency should be over 5 GHz because the input frequency of the divider is 10 GHz. The ratio (K) above 8 is recommended for correct operation of the divider under environmental and parasitic variations. Fig. 11(d) shows current consumptions of three divide-by-2 circuits at K = 8. The implemented divider has the ratio (K) of 16 for more robust operation, and the normalized latch size (L) is set 2. Although the DLL and cascaded buffers consume some power, the total power consumption of the proposed divide-by-2 circuit is remarkably reduced compared to a conventional design.

III. RESULTS

The 1:4 DEMUX IC is fabricated in 0.13 μm CMOS and placed in a micro-lead-frame (MLF) package, the printed circuit board (PCB) is made with Rogers 4350B material, whose signal loss at high frequency is less than that of FR4. The prototype chip could not operate with a 1.2 V supply at 20 Gb/s because of the reduced bandwidth of the input buffer. It could achieve 20 Gb/s operation from a 1.5 V supply because of the increase of bias voltage dependent on the supply. To provide the constant swing in the CML circuits under process and temperature variations, the bias voltage is adjusted by the replica-biasing circuit with a Vref which defines the low level of swing. The Vref is generated by a voltage divider consisting of a series of resistors and has the value of 3VDD/4. As the supply voltage increases, the Vref and the bias voltage rise. The CML circuits draw more current, and thus the chip achieves higher data rate. Consequently, we present the results from a 1.2 V supply at 19 Gb/s for low power consumption. A 19 Gb/s input data and 9.5 GHz input clock are applied for DEMUX measurement. The 19 Gb/s data is generated by multiplexing four 9.5 Gb/s 215−1 PRBS signals. The pulse pattern generator (PPG) generates two 9.5 Gb/s data signals and a 9.5 GHz clock signal. To generate 19 Gb/s signal, the 4:1 MUX module needs four 9.5 Gb/s input signals and a 38 GHz clock signal. Power dividers are used to split two 9.5 Gb/s signals into four signals. The 4x frequency multiplier module outputs the 38 GHz clock signal from the 9.5 GHz input clock. Since two signals in four 9.5 Gb/s signals are duplicated by the power dividers, the MUX module can output the 19 Gb/s signal. To test the DEMUX chip with single-ended input signals, one pin of the differential pair in the test chip is terminated with ground. The input data and clock have the amplitude of 0.5 Vpp (single-ended). We could not measure the bit error rate (BER) due to limited instruments for adequate measurement setup under the condition that the 1:4 DEMUX outputs 4.75 Gb/s signals and the PPG generates 9.5 Gb/s signals. The eye diagram of the output data and the waveform of the output clock are shown in Fig. 15. The horizontal eye opening is 150.1 ps, and the vertical eye opening is 62.1 mV (single-ended). A die micrograph is shown in Fig. 16.
IV. CONCLUSION

A 20 Gb/s 1:4 DEMUX in a 0.13 μm CMOS has been presented. A coupled latch and buffer insertion technique enhances the signal bandwidth without inductive peaking effect. A divide-by-2 circuit has the structure using a static divider of small size and a DLL to achieve low power and improved timing margin. A static frequency divider based on the coupled latch and buffer insertion has an increased output swing without the degradation of the sensitivity. The proposed 1:4 DEMUX provides effective techniques for high data rate with low power dissipation.

REFERENCES


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Dr. Yu was a co-recipient of the Best Paper Award at the 2002 SoC Design Conference and received the Technology Outstanding Achievement Award and Distinguished Medal for his contribution to the RF CMOS Technologies from IEEEK in 1999 and 2003, respectively. He founded and has served as Chairman of RF Integrated Circuit Technology Society in Korea since 2000. From September 2002 to August 2003, he was a Visiting Professor at the University of Florida, where he studied programmable RFIC for the future reconfigurable RF transceiver. He is the author or co-author of over 110 technical papers and 70 patents in the RF devices and integrated circuits design areas. He is listed in Marquis Who’s Who in the World.